Research Needs for
Memory Technologies

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Background, Trend, and Challenges

Not only memories are intricate part of most, if not all, integrated circuits, the popular consumer products in the mass storage space put memory devices as the most common transistors in the market today. Also, flash memory currently serves as the technology driver for most of the critical processing steps. To continue this pace is getting increasingly more challenging but is important to the whole industry. This document identifies industry-driven research needs for a variety of embedded and stand-alone memory devices. It is intended to research novel materials, device concepts, and architectural aspects of memory devices addressing continuation of scaling and new applications.

This document is prepared for the purpose of generation and reference of the Call-for-White-Papers in the Device Sciences Memory Technologies thrust. Within the program structure of SRC GRC, this thrust deals specifically with technology-related research. Other memory-related work but focusing on circuit design or compact modeling is dealt with in its respective thrust and excluded from this call.

The general technology requirements of memories are; compatibility and integration with CMOS, high functional bit density, high speed, low power dissipation, and low cost. The major technology barriers are stability, reliability, data retention, disturb, on-off ratio, and endurance. There is a significant interplay between requirements and barriers, and optimized trade-offs between them are expected.

The requirements and challenges specific to memory types are listed below [1]:

- Nonvolatile Memory: Common to all charge-storage type of transistors is the limit of scaling the tunnel oxide while facing the problem of retention for the same required lifetime. In order to maintain the retention time of several years, the tunnel oxide between the channel and the charge storage node is limited to EOT of roughly 4 nm. Considering the additional top dielectric blocking layer, the finite total gate dielectric thickness of the transistor limits the channel length to a minimum of 20–30 nm. In order to continue to scale the area per bit, the channel length has to be directed vertically. Additionally, the number of bit per cell is another important means to improve the effective area efficiency. The ITRS forecasts that 4 bits per cell will be in the market in about 10 years. Embedding flash nonvolatile memory into CMOS process flows is always a common goal in the industry. Embedded flash faces different and much tougher scaling challenges than those for the stand-alone counterpart. For example, the current memory array area is occupied substantially by the high-voltage peripheral devices required to write and erase the bit cells, typically +/- 9V. For embedded flash applications, it is critical to find technologies that allow scaling of voltage required to operate the memory array. In general for nonvolatile memory, the industry trend is switching from the current floating-gate transistor to the charge-

trapping transistor. Eventually they will be replaced by 2-terminal non-transistor type of cells for the aforementioned reason of scaling. The latter has a vast range of options and the eventual winner is still unknown, although it is likely that there will be a few variations coexisting in the market. The different nonvolatile memory forms and their challenges are described below:

o Floating-gate transistor—Pertinent to the floating-gate structures is the requirement for high coupling ratio. This is achieved typically by wrapping around the floating gate by the control gate. Processing for such severe topography gets harder with scaling.

o Charge-trapping transistor—The industry trend is moving from the floating-gate type of transistor cell to the charge-trapping type. The SONOS device uses a thinner non-conducting layer Si_3N_4 to trap charges. They are more planar than the floating-gate type and are easier to scale. Since charges in Si_3N_4 are not mobile, they can be located either near the source or drain, and such information is counted as two bits. The challenges are in general reliability and endurance. Also trapped electron charges are difficult to detrap, and injection of holes needed to neutralize them are more difficult due to higher hole barrier.

o Non-charge-storage type—This group of newer options require new materials and physics that have not been part of traditional Si processes. There are many options that are being pursued and the specific types will be described. [2] Several new materials and mechanisms are currently being investigated to develop the next-generation memory devices. Most of these approaches rely on non-Si or non-SiO_2 based elements and open up the possibility of stacking several layers of memory arrays on top of the CMOS support circuitry. Furthermore, the commonality among them is that they are all two-terminal non-transistor type of cells which makes them more area efficient. But multi-level programming with them are generally more difficult. Another penalty of these two-terminal devices is that in the cross-point arrays, a selection device is needed for every cell in order to prevent parallel leakage paths through unselected cells in reading, and disturb of unselected cells in writing.

• SRAM—Because this memory is typically constructed from core CMOS technology, all issues associated with MOSFET scaling apply to scaling of SRAM. Additionally, there is a desire to find a dense SRAM replacement that can substantially reduce the area occupied by the traditional 6T SRAM bit cell. Discovery of such a bit cell would have profound implications on the die cost of integrated circuits given the ever-increasing area ratio occupied by this type of memory. In addition to area scaling, there is also a need to develop alternate architecture that maintains stability while operating at lower voltages, thus, allowing the industry to substantially reduce standby power consumption in the memory arrays.

• DRAM—The one-transistor/one-capacitor cell, which can be trench or stack capacitor (latter is more common), requires photoresist and etch processes of very high aspect ratio. To minimize the capacitor area, higher-K dielectrics are a natural path, to go beyond that of high-performance logic devices. This is especially challenging for the extra requirement of non-planar surface for the capacitor in order to get adequate capacitance with minimal layout area. To meet retention and refresh requirements, the transistor has to control

both subthreshold leakage and junction leakage. The transistor structure is becoming non-planar such as recessed channel and FinFET. Embedding DRAM into a CMOS process flow has become more popular over the last decade.

Research Topics

To better identify more specifically the topics of research needs for our member companies, we have listed the topics into finer details as shown in the table below. Furthermore, we will indicate the level of priority for each topic to provide a general feeling of what our members consider most beneficial to their needs.

Floating-Gate Transistor

We anticipate that research in the following areas could extend the life of conventional flash devices: tunnel dielectrics, new material for storage layer, nano-particle storage layer, multi-bit, writing and reading speed, retention, low-power writing, endurance, and 3-D stacking of multiple layers.

Charge-Trapping Transistor

This type of transistor cell is more scalable than the floating-gate type. One research focus is the challenge of endurance and improvement of the charge-trapping layer. Other areas of interest are tunnel dielectric, 3-D vertical string, multi-bit, etc.

PCRAM (Phase-Change RAM)

The PCRAM is already in the market for medium size (total bit count). The current required for writing is a big limitation for power. For this reason, continuation to scale the critical dimension could help, or/and with new materials which have lower phase-change temperature or lower heat conductivity. Other challenges are endurance, drifting, and the difficulty to achieve multi bits.

STTRAM (Spin-Torque-Transfer RAM)

The STTRAM has high potential of being the main-stream technology due to low power in writing. Nevertheless, continue to scale the device cross-section is required to realize that potential. The current structures require 10–12 different layers, some of which are quite thin. This is a factor for reproducibility and cost. Other challenges of this technology include speed, on/off resistance ratio, narrow coercivity window, endurance, and multi-bit capability.

MRAM (Magnetoresistive RAM)

The drawback of this older technology is the requirement of an external magnetic field outside the device for writing and erase such that interference of cells at close proximity prevents high-density scaling. This is the exact problem STTRAM tries to solve by passing an internal current through its own cell to switch the magnetic polarization.

FeRAM (Ferroelectric RAM)

FeRAM can be in the form of a 2-terminal capacitor or 3-terminal transistor (FeFET) which incorporates the ferroelectrics as the gate dielectrics. The attractiveness is low-voltage operation. The main hurdle is the drift which severely limits the retention time and application as nonvolatile memory, especially at elevated temperatures. Endurance is another challenge. There have been studies to use FeFET as a DRAM replacement.

RRAM (Resistive RAM)

Without debating on the suitability of devices under the category RRAM, we refer here to the 2-terminal memory cells based on resistance change due to movement, from diffusion or drift process, of ions or/and reactions such as oxidation/reduction. Included are also switching mechanisms due to charge injection and trapping. For many device types the exact mechanisms that cause the change in resistance state is not well known, but they are known to occur in the bulk of the insulator layer, along some conducting filaments, or at the insulator-metal interface. Depending on the material system, the set/reset processes can be carried out in bipolar or unipolar voltage polarity.

Other Novel Non-Charge-Storage Memories

We include in this category all other non-charge-storage types some of which can be explored for special applications. These include Mott-transition memory, molecular memory, nanoelectromechanical RAM, etc. [2]

Selection Device

Much of the literature on these 2-terminal cells envisages a cross-point memory architecture - each memory storage cell is sandwiched between a word line and an orthogonal bit line. However, due to this array architecture, there are leakage paths through unselected cells during a read operation, and during programming many other unselected cells are being disturbed. This is in part due to cells with two terminals, unlike a transistor cell which can be turned off with a third terminal. An optimally designed addressable/readable memory array implementation thus requires the insertion of a selection device for each memory cell. To realize the small size of these novel options, this calls for the ability to fabricate stackable selection devices over or under each cell. The attributes required in this device include low thermal budget for fabrication and dopant activation, small geometry, small on-resistance, low leakage current and, for bipolar types of memory cells, bi-directional operation. A common approach to a selection device is simply a diode but other similar options are to be explored for improvement. A transistor selection device dominates the area and does not provide an optimized solution.

SRAM: Innovative Technologies

SRAM is by far the most common embedded memory technology because of the common features with the core technology. The 6-T layout is much larger than other memories (DRAM and nonvolatile memories) and SRAM typically dominates the die size for many systems. Innovation in integration and structure leading to smaller foot-print would be of great value. Other challenges include worsening noise margin and stability due to voltage scaling approaching 0.5 V.

SRAM: Revolutionary Solution for Replacement

Because of the large area demanded by the 6-T layout, an invention of a single device or dual-device combination to replace the current SRAM architecture would be a tremendous benefit to the industry. This would be a high-risk and high-pay-off type of research.

DRAM: Innovative Technologies

The challenges to continue to scale DRAM include the difficulty in scaling the capacitor. Traditionally they are in the forms of trench and stack structures, but these are getting more difficult to maintain sufficient capacitance to hold certain required amount of charge. Higher-K, larger than 50, dielectrics can be beneficial. Other improvements needed include low leakage which is getting increasingly difficult with transistor scaling.

DRAM: Revolutionary Solution for Replacement

As a result of the difficulty associated with scaling DRAM, there is a need to develop alternative cell structure that can maintain the read/write/refresh performance but with much smaller area. Ideally the new option should be a single device in place of the 1T-1C combination. This research also falls into the category of high risk and high pay-off.

Research Priorities

Member company representatives were asked to vote on the topics of their preference, with high priority (H) or medium priority (M). Consensus is built on the average of inputs. This methodology yields a total of 3 topics of high priority (highlighted in yellow), and 6 of medium priority (highlighted in blue), as shown in the table below. It is with these guidelines that we will call for and select proposals in this new cycle of research. It should be mentioned that the prioritization is to encourage submissions in certain areas, and it is possible that some important areas are missed, so all papers will be considered for special quality and insight.

References

[1] International Technology Roadmap for Semiconductors (ITRS) 2010 Edition. "*Process Integration, Devices, and Structures*". (http://www.itrs.net/Links/2010ITRS/Home2010.htm)

[2] ITRS ERD/ERM 2010 Future Memory Devices Workshop Summary. (http://www.itrs.net/Links/2010ITRS/Home2010.htm)

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Memory Technologies: Topics and Priority

Nonvolatile memory

Charge-storage type	1a	Floating-gate transistor	M
	1b	Charge-trapping transistor (SONOS)	M
Non-charge-storage type	2a	PCRAM (phase-change)	M
	2b	STTRAM (spin-torque-transfer)	H
	2c	MRAM (magnetic)	
	2d	FeRAM (ferroelectric)	
	2e	RRAM (metallic oxide, ionic)	H
	2f	Other novel non-charge-storage memory cells	
Selection device	3	Efficient selection device for cross-point arrays	M

Embedded memory

SRAM	4a	Innovative technologies to improve SRAM scaling	M
	4b	Revolutionary solution for SRAM replacement	H
DRAM	5a	Innovative technologies to improve DRAM scaling	
	5b	Revolutionary solution for DRAM replacement	M