Research Needs for Compact Modeling

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Device Sciences Compact Modeling TAB

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Introduction

Compact Modeling refers to the development of models for integrated semiconductor devices for use in circuit simulations. The models are used to reproduce device terminal behaviors with accuracy, computational efficiency, ease of parameter extraction, and relative model simplicity for a circuit or system-level simulation, for future technology nodes. The users of the models are the IC designers, and the model interface is considered part of the model development. Physics-based models are often preferred, particularly when concerned with statistical or predictive simulation. The industry's dependence on accurate and time-efficient compact models continues to grow as circuit operating frequencies increase and device tolerances scale down with concomitant increases in chip device count, and analog content in mixed-signal circuits. Compact modeling is a critical step in the design cycle of modern IC products. It is certainly the most important vehicle for information transfer from technology fabrication to circuit and product design.

Semiconductor companies, Semiconductor Research Corporation (SRC), and the Compact Modeling Council have made significant efforts during recent years to secure future availability of high-quality compact models through proprietary in-house company developments and university research. The current university program for Compact Modeling funded by SRC started in Jan. 2010 and will be concluding in early 2013. SRC plans to initiate a new three-year research program starting Sept. 2013 to support university research addressing the most important needs identified in this report.

In contrast, device modeling is concerned with the understanding and nature of detailed physical representations of device operation, and is not the topic of this call or document. Device modeling is usually carried out under the umbrella of TCAD (Technology Computer Aided Design) in support of device and process modeling, and views its audience to be principally device physicists and technologists rather than designers. It seeks to be predictive rather than completely parameterize-able from terminal electrical measurements.

Environment and Trend

As device scaling continues, potential solutions are sought after which are based on new MOSFET channel materials. These include III-V compound semiconductors, carbon nanotubes (CNTs), semiconductor nanowires (NWs), and graphene nano-ribbons. Apart from the new material properties, their nano-size features result in quantum effects that must be accounted for.

As device size becomes smaller, device reliability due to degradation with operation time, as well as device variability due to process variations, are both becoming increasingly severe. While reliability has been an on-going topic, variability is relatively new which requires new insight.

Besides scaling, the industry trend is functional diversification, i.e., increasing integration of functions and technologies onto the same chips. This naturally calls for wider coverage of device types. In particular, increase of analog contents in mixed-signal circuits is of special interest. This fact, along with the aforementioned increased variety of device options, requires a much larger range of areas to be covered as well as improved model accuracy.

Research Needs Topics

To start to generate the research needs, each member company was asked to suggest topics to be included, as well as how to organize them into categories. The results are shown below. The topics of research needs are organized into four categories: (1) Digital Devices, (2) Analog Devices, (3) Reliability-Related, and (4) Tools and Methodologies.

1. Digital (Logic) Devices
   - 1a. Advanced Si CMOS structures and phenomena (FinFET, SOI, bulk, nanowire, gate leakage, tunneling, GIDL…)
   - 1b. Layout dependent (non-local) effects
   - 1c. Ge and III-V channel FETs (degeneracy effects)
   - 1d. Novel devices (CNT, NW, graphene, photonic…)
   - 1e. Memories
2. Analog Devices
   - 2a. Advanced Si CMOS structures for analog applications and phenomena (FinFET, SOI, bulk, nanowire, subthreshold leakage, gate tunneling, GIDL, intrinsic bipolar action…)
   - 2b. Power MOS transistors (Si, III-V, GaN, SiC, recovery diode…)
   - 2c. Bipolar transistors
   - 2d. Other active components (varactor, diode, sensors [optical, magnetic, thermal, mechanical]...)
   - 2e. Passives (resonator, inductor…)
   - 2f. Novel devices for analog applications (III-V, carbon nanotube, graphene, MEMS…)
3. Reliability-Related
   - 3a. Reliability/aging
   - 3b. Noises and variability (random telegraph noise, 1/f noise, thermal noise, layout-dependent effects, processing variability)
   - 3c. ESD devices (includes I/O devices)
4. Tools and Methodologies
   - 4a. Run-time improvement
   - 4b. Fast full-chip verification
   - 4c. Custom device model interface
   - 4d. Chip-level topography prediction
   - 4e. Automated generation of block-level models
   - 4f. Interconnect (parasitics, optical interconnect and components)

In Analog devices, even the structures can be similar to those of Digital devices (comparing 2a to 1a, and 2f to 1d), here the focus is on analog metrics such as cut-off frequency, noise, matching, linearity, etc. Power MOS transistors (2b) refers to power devices based on MOS technologies (both Si and III-V based) with focus on asymmetric source/drain doping profiles and advanced drain architectures. The model should be physics-based, predictive for DC/AC characteristics of scaling effects, and include parasitic effects such as self-heating and bipolar.

Research Priorities

Next, each member company was asked to identify topics of high priority (H) and that of medium priority (M). The rest of topics will be automatically designated as low priority. The overall net results are shown in the last column of the table, which is consisted of 7 overall high priority (green) and 8 overall medium priority (yellow).

University researchers are advised to write their proposals with knowledge of the needs and priority. However, all proposals, including those outside the topics in this table, will be considered. Also within each topic, researchers are encouraged to propose research targeting longer-term products.

Table 1. Topics of research needs and their priorities from member companies. Highlighted in green are of high priority (H), and that in yellow are of medium priority (M).

		Priority
1. Digital Devices		
1a	Advanced Si CMOS structures (FinFET, SOI, bulk, nanowire…)	H
1b	Layout dependent (non-local) effects	H
1c	Ge and III-V channel FETs	M
1d	Novel devices (CNT, NW, graphene, photonic…)	M
1e	Memories	
2. Analog Devices		
2a	Advanced Si CMOS structures for analog applications (FinFET, SOI, bulk, nanowire…)	H
2b	Power MOS transistors (Si, III-V, GaN, SiC, recovery diode…)	M
2c	Bipolar transistors	
2d	Other active components (varactor, diode, sensors [optical, magnetic, thermal, mechanical]...)	M
2e	Passives (resonator, inductor…)	
2f	Novel devices for analog applications (III-V, carbon nanotube, graphene, MEMS…)	H
3. Reliability-Related		
3a	Reliability/aging	H
3b	Noises and variability	H
3c	ESD devices	H
4. Tools and Methodologies		
4a	Run-time improvement	M
4b	Fast full-chip verification	M
4c	Custom device model interface	
4d	Chip-level topography prediction	M
4e	Automated generation of block-level models	
4f	Interconnect (including optical)	M

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