Semiconductor Research Corporation

Because the future can't wait, we bring the best minds together to achieve the unimaginable

AIHW / CADT Research Program Joint Annual Review

May 22-26, 2023

IBM Almaden, San Jose, CA

John Oakley, Science Director
Marcus Pan, Science Director
LaTanya Holmes, Research Program Coordinator
LaDonya Dooley, Research Program Coordinator

https://www.src.org/calendar/e007736/

Thank you!

On Behalf of the SRC,

Thank You!

- To all the industry members for their sponsorship and mentorship
- To all the Principal Investigators & their Students for the great research effort
- To LaTanya Holmes and LaDonya Dooley at SRC for the logistical support
- To all of you for being in-person with us!

e-kickoff Reminders

Everyone will be participating in-person

Presenters should remember to speak clearly and keep within the allotted time.

Timing:
30 min (presentations, 25 min talks)
20 mins (kickoffs, 15 min talks)

Presentations and Q&A will be live. Please be mindful, so watch the time to leave 5 minutes for Q&A!!!

Informal Presentations

Please indicate if you want the audience to interrupt with questions. Q/A will occur at the end.

SRC

Reminder: Invoicing and Deliverables

Regular invoicing

Invoice on regular basis: monthly is preferred
Excess money (calendar year) is considered profit and taxable!
Spending must occur within contract period
Invoicing expected to be at or above 90% invoiced at end of each contract period
Final invoice within 60 days after project ends

Submit deliverables on time: even 1 day is too late!

System will flag delinquencies
Late deliverables will stop invoices being paid and can jeopardize future funding
Contact SRC if there are issues with getting deliverables on time
All submissions will be done in Pillar Science

Pre-publication drafts must be deposited at SRC > 60 days before published

Best practice: deposit draft to SRC website when submitting to journal/conference (also thesis)
Update the draft on the SRC website with final paper after acceptance (select submit a new version)
Acknowledgement of SRC funding must be added to all publications
At minimum, the acknowledgement should read: "This work was supported in part by Semiconductor Research Corporation (SRC)."

Reminder: Send News Items to SRC

- Send noteworthy events and announcements that you and your team are involved in to SRC

- Send this information on a monthly basis. We use what we can in our SRC newsletter and monthly emails to the Advisory Board and liaisons
  - Best Paper Awards (who, award, title of piece, where, when and photos of students/faculty)
  - Papers, posters presentations, and/or conference talks
  - Professional Recognition Awards: IEEE, teaching awards, etc.
  - Professional activities such as workshops, tutorials, and invited talks

More Than 17,000 subscribers!!

- All submissions must have a web link (URL) to the award, paper, etc.
  - If you have your own website that contains information pertaining to your research, share the link with SRC as well

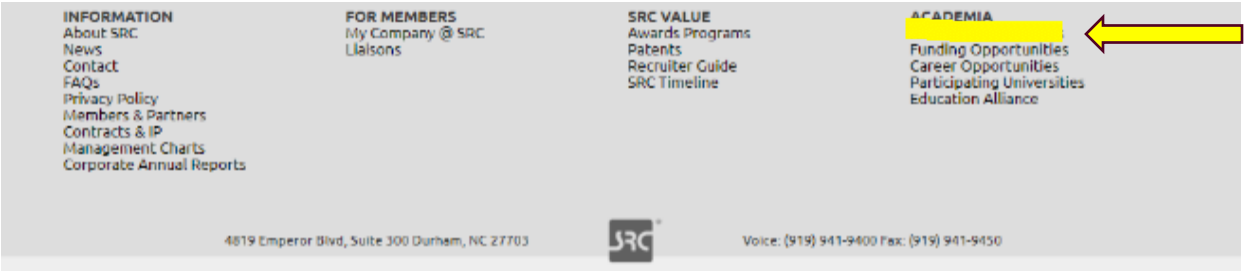
SRC

https://www.src.org/newsroom/newsletter/

Resources that Help Academics Evaluate, Adopt, and Amplify Emerging Member Solutions

Member Resources

- SRC has collected information members provide for the academic community, including education, design, and prototyping
- SRC researchers and students are encouraged to take advantage of these resources in their research and education activities



Member Resources

SRC has collected information members provide for the academic community, including education, design, and prototyping. SRC researchers and students are encouraged to take advantage of these resources in their research and education activities

Intel

- Intel Open Data Center Diagnostic Project
- Intel Academic Compute Resource Environment (ACE)
- Intel Academic Program for oneAPI

Analog Devices

- Active Learning Program
- ADALM-SR1 Hardware
- ADALM-SR1 Switching Regulator Active Learning Module

ARM

ARM Academic Access
ARM Education

- ARM University Program Education Kits
- ARM Education Online Courses
- ARM Education Textbooks and Reference Books

Texas Instruments
Specific tutorial and curriculum for universities include:

- Texas Instruments University Program
- TI Robotics System Learning Kit
- TI Power Management Lab Kit
- TI Experimental Power Electronics Reference and Curriculum
- TI Precision Labs

IBM

- IBM tutorial and curriculum for universities
- IBM Skills Academy
- IBM + Coursera
- IBM PhD Fellowship Program
- IBM Quantum Computing - student opportunities
- IBM AI Hardware

NXP

- Rapid IoT Prototyping Kit

Siemens

- EDA Academic Products

Qualcomm

- University Relations Program

SRC

https://www.src.org/program/grc/guide/researcher/guidelines/

SRC Student Platform on LinkedIn

- What is the **SRC Research Scholars Program?**
  - SRC provides undergrads, graduate students, and postdoctoral researchers with a unique education consisting of traditional course work, cutting-edge research, and direct interaction with the semiconductor industry
  - These Research Scholars work on industry-relevant research with SRC-funded faculty who are recognized experts in their fields
  - Through our extensive community of academics and industry personnel, we nurture the evaluation of the talent pipeline for our industry and beyond
  - Our alumni have become industry leaders and renowned faculty researchers, creating a virtuous cycle where mojo begets mojo

Join Now! And add them to Pillar Science

Get LinkedIn with SRC

SRC uses a special LinkedIn Affiliate page for the SRC Research Scholars Program. Undergrad, graduate students, and postdoctoral researchers participating on SRC research add their SRC Research Scholars experience to their LinkedIn profile. This allows Scholars a way to professionally showcase their talent and experience. It also simplifies how recruiters, engineers, and even other Scholars can find SRC Research Scholars, using either the LinkedIn Search* or LinkedIn Recruiter*.

SRC Research Scholars Program*

By being part of our community, Research Scholars will have a unique opportunity to get to know professionals with careers in the semiconductor industry or government, top researchers in their fields, and other students with similar interests.

SRC encourages all undergrads, graduate students, and postdoctoral researchers to join this program!!!

https://www.src.org/student-center/handbook/linkedin/

Pillar Science Common Issues & Links for Academics

- There are lots of help articles in Pillar Science which can help answer these questions.

- Here's an article about logging into Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/11198322803099-How-To-Login-to-Pillar-with-SRC-org-Credentials
- Here's an article about update your profile in Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10330492961563-How-to-Edit-Your-Profile
- Here's an article about adding students, administrators, or other academics to your project
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10330872380187-How-to-add-Students-Admins-or-other-Academics-to-Your-Project
- Here's an article about submitting projects results and deliverables
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/11213311626139-How-to-Submit-Project-Results-previously-known-as-publications-
- SRC hosted a live demonstration for academics on January 31, 2023, and the recording is available
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/12543067480091-Pillar-Science-Demonstration-for-Academics-Video-Recording-

SRC

https://semiconductorresearchcorporation.zendesk.com/hc/en-us/sections/11359770755483-How-Tos-for-Academics

Guidance for Depositing Supporting Code and Data with Pre-Publications

As part of our move to Pillar Science, there is the ability to collect not just the pre-publications PDF's but also arbitrary file formats (.mp4, .ppt, etc.) as well. This new capability enables a new way for SRC programs to facilitate technology transfer to our sponsors.

Going forward, we will be requiring that all code and supporting data below a certain size threshold to reproduce a pre-publication also be uploaded to Pillar Science.

- SRC's reasons for doing this are:
1. **To more fully document the research output of our programs to demonstrate to our sponsors the breadth and depth of the funded work**
2. The full value of code and data is not often found with its original author but when used across a wider scientific community like our sponsors
3. By having better data and code visibility in our programs, our sponsors will have a better understanding how to connect with researchers

Historically, there has been concern amongst researchers that the code and the data are not "camera ready" for distribution at the pre-publication state. **While these concerns are valid, perfect is the *enemy* of accomplishment.**

- SRC seeks to obtain a snapshot of your code at the state it was in when you submitted your publication to the SRC repository.
- If your code and data are not in a state that you would want to post on an open code repository like GitHub, that is acceptable. Our sponsors employ trained professionals who have the experience to handle and interpret idiosyncratic legacy code and documentation.
- SRC would also like the data collected and used to generate publications to be submitted to Pillar Science as well.
- **Preferably in a single compressed file in an open format marked with the publication's name followed by data so that it read like this, "[Publication Name]_data.ZIP".**

The submission of data to SRC is a direct ask, although it is a right granted by terms of the sponsored research agreement.

- **Contained within that compressed file should be the data used to generate figures, any code developed for that publication as well as any experimental data acquired if the file size is below 10 Mb.**
- If the data file is in a proprietary file format as often happens with analytical instruments, please convert it to an open format before uploading
- If you are not able to convert from proprietary file format to an open file format, please include it in the compressed data file anyway.
- If the data was acquired from an open depository like the UCI Machine Learning Repository, a notification of that along with a dated weblink in a .txt file should be included.

https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/14019093083163-Guidance-for-Submitting-Supporting-Code-and-Data-

Key Performance Indicators (KPI) Process Changes

SRC has moved the KPI forms into Pillar Science and pre-upload the XLSX files
PI will update throughout the year, and Liaisons will be ahead to review at anytime

KPIs sent to the PIs + **Instructions***

PI fills out the KPI

SRC Quality Control

TTs + Vetting presentation** sent to members

Verified TTs reported to the master count

End of the year

Year-end report sent to SRC Members

- KPI instruction video is available: https://www.src.org/src/guide/kpi/

KPIs/TTs are part of annual review process

*TT = "meaningful" Technology Transfers

Because of well-defined KPI process flow, SRC members can maximize their research experiences with meaningful Technology Transfers.

https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/15056064943771-How-to-edit-and-manage-your-Key-Performancer-Indicators-KPI-card-

Pillar Science Common Issues & Links for Industry

- There are lots of help articles in Pillar Science which can help answer these questions.

- Here's an article about logging into Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/11198322803099-How-To-Login-to-Pillar-with-SRC-org-Credentials
- Here's an article about update your profile in Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10330492961563-How-to-Edit-Your-Profile
- Here's an article about adding yourself as a liaison
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10092535189403-How-To-Add-Yourself-As-A-Liaison
- Here's an article about how to find research projects of interest
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/9194403647131-Using-Projects-Page
- There was 2 industry demonstrations for industry on February 14 and 21
  - The recordings can be found on the SRC.org website at : https://www.src.org/pillar/

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https://semiconductorresearchcorporation.zendesk.com/hc/en-us/sections/11366772078235-How-Tos-for-Industry

Intellectual Property Statement

- The information provided by researchers during this annual review
  - Is the property of the university and of the researchers presenting this information
  - May include research results sponsored by and provided to the funding members
  - May include intellectual property rights belonging to the university and SRC, to which sponsors may have license rights

- By attending or viewing this review, you are agreeing
  - Not to use this information for purposes unrelated to the review unless and until approved by SRC
  - To keep this information in confidence until the university and SRC have evaluated and secured any applicable intellectual property rights

- After any intellectual property rights have been secured, the SRC encourages the University and researchers to publish and freely disseminate this information and results of the sponsored research program.
  - Worldwide patent rights are waived if publication or public dissemination occurs prior to filing a corresponding U.S. provisional or utility patent application

SRC

https://www.src.org/about/contracts-ip/#ip

General Data Protection Regulation

- Applies to SRC
- Personal data regulations
- Involves privacy notices, consent, and security
- SRC Privacy Policy

https://www.src.org/app/account/guide/privacy-policy/

Agenda – Day 1

- Presentations (30 minutes)
  - 25-minute presentations with 5-minute Q&A (live)
- Kick-offs (20 minutes)
  - 15-minute presentations with 5-minute Q&A (live)

All Times in PT

SRC

https://www.src.org/calendar/e007736/

Monday, May 22nd

9:00 – 9:15 am	Welcome / Introduction	Pan Marcus & John Oakley / SRC
e-Kickoff of New Starts All Day		
9:15 – 9:35 am	3150.001: MetaPerf: Multi-Model-Multi-Task (M3T) Real-time Machine Learning for the Metaverse	Vijay Janapa Reddi Harvard University
9:35 – 9:55 am	3151.001: Simulating and Modeling Hardware for Machine Learning Workloads at Scale	Matthew Sinclair University of Wisconsin
9:55 – 10:15 am	3152.001: Efficient Hardware Software Co-design of Compute-In-Memory Accelerators for Edge Application	❖Utkarsh Saxena / 💻Kaushik Roy Purdue University
10:15 – 10:35 am	3153.001: Scaling Probabilistic Computers for Sustainable Computing	💻Kerem Camsari University of California – Santa Barbara
10:35 – 10:55 am	3155.001: Automated Data Augmentation for Deflating Data Bias	Prabhat Mishra University of Florida
10:55 – 11:15 am	3156.001: Reconfigurable Floating-Point/Integer Digital Compute-In-Memory Processor for Edge/Cloud Deep Learning Acceleration	Bonglin Kim University of California – Santa Barbara
11:15 – 11:25 am	Break	
11:25 – 11:45 am	3157.001: Memory System Design for AI/ML & ML/AI for Memory System Design	💻Onur Mutlu ETH Zurich
11:45 – 12:05 pm	3154.001: Explainable and Agile AI Hardware/Software Optimization with AI	Aviral Shrivastava Arizona State University
12:05 – 12:35 pm	3014.001: A Novel Imitation Learning Framework for Self-Optimizing Systems	Jana Doppa Washington State University
12:35 – 1:35 pm	Lunch	
1:35 – 2:05 pm	**Industry Talk:** The Mega-Trends Driving Semiconductor Growth	Neil Hand / Siemens EDA
2:05 – 2:25 pm	3160.007: AI-Assisted and Layout-Aware Analog Synthesis and Optimization with Design Intent	David Pan University of Texas at Austin
2:25 – 2:45 pm	3173.001: Standardizing Boolean Transforms to Improve Quality and Runtime of CAD Tools	Alan Mishchenko University of California - Berkeley
2:45 – 3:05 pm	3174.001: High-Throughput Monitors for Pre- and Post-Silicon Verification	Kevin Skadron University of Virginia - Charlottesville
3:05 – 3:25 pm	3175.001: vHLS: Verifiable High-level Synthesis	❖Hanchen Ye / 💻Deming Chen University of Illinois at Urbana-Champaign
3:25 – 3:45 pm	3176.001: Functional Safety over Lifetimes of CMOS Chips: Models, Test Methods, and Aging-resilient Design	Sandeep Gupta University of Southern California
3:45 – 3:55 pm	Break	
3:05 – 3:25 pm	3175.001: vHLS: Verifiable High-level Synthesis	❖Hanchen Ye / 💻Deming Chen University of Illinois at Urbana-Champaign
3:25 – 3:45 pm	3176.001: Functional Safety over Lifetimes of CMOS Chips: Models, Test Methods, and Aging-resilient Design	Sandeep Gupta University of Southern California
3:45 – 3:55 pm	Break	
3:55 – 4:15 pm	3192.001: Improving Fault Injection-based Functional Safety Evaluation using Machine Learning	Kanad Basu University of Texas at Dallas
4:15 – 4:35 pm	3160.003: Techniques for Online Ageing Detection and In-field Characterization of Aging Phenomena	❖Matthew Strong / 💻Degang Chen Iowa State University
4:35 – 6:00 pm	TAB Caucus (Industry Members Only)	
6:00 pm	End of Day 1	

❖ Student Presenter 💻 Remote Presenter

Agenda – Day 2

- Presentations (30 minutes)
  - 25-minute presentations with 5-minute Q&A (live)
- Kick-offs (20 minutes)
  - 15-minute presentations with 5-minute Q&A (live)

All Times in PT

Tuesday, May 23rd		
9:00 – 9:10 am	Welcome / Introduction	Pan Marcus & John Oakley / SRC
e-Kickoff of New Starts from 9:10 – 12:20 pm		
9:10 – 9:30 am	3177.001: Test Generation and Data Analytics for Functional Safety Assessment and Failure Prediction	❖Sai Manish / 💻Krishnendu Chakrabarty Arizona State University
9:30 – 9:50 am	3160.006: Machine-Learning Based Analog Mixed-signal Design Tool	Shuo-Wei Chen University of Southern California
9:50 – 10:10 am	3160.005: ML-Assisted Scalable DfT and BIST of AMS Systems	❖Suhasini Komarraju / 💻Abhijit Chatterjee Georgia Institute of Technology
10:10 – 10:30 am	3149.001: Efficient and Interpretable Symbolic AI for Intelligent Reasoning and Decision Making	Mohsen Imani University of California - Irvine
10:30 – 10:50 am	3159.001: Enabling Simulation and Design of Distributed Heterogeneous AI Accelerator Platforms	Tushar Krishna Georgia Institute of Technology
10:50 – 11:10 am	3191.001: Exploring Extreme Sparsity in Training and Inference for Graph Neural Networks to Achieve High Performance Scaling on Large Core Count Machines	Caiwen Ding / ❖Shaoyi Huang University of Connecticut
11:10 – 11:20 am	Break	
11:20 – 11:40 am	3189.001: Compiling Embeddings-Based AI Models for Near-Data Accelerators	Mattan Erez University of Texas at Austin
11:40 – 12:00 pm	3148.001: Ultra Low-Energy Ultra Low-Latency Machine Learning using Weightless Neural Networks	Zachary Susskind student of Lizy John University of Texas at Austin
12:00 – 12:20 pm	3160.002: tinyASR: Self-Supervised, Sub-10μW Automatic Speech Recognition Hardware for IoT Devices	Dewei Wang student of Mingoo Seok Columbia University
12:20 – 1:20 pm	Lunch	
1:20 – 1:50 pm	2986.001: MLPerf 2.0: Benchmarking End-to-End (E2E) AI Inference Application Performance	Vijay Janapa Reddi Harvard University
1:50 – 2:20 pm	2810.078: Programmable Mixed-Signal Accelerator for DNNs with Depthwise Separable Convolution Layers	Rohan Doshi student of Boris Murmann Stanford University
2:20 – 2:50 pm	3015.001 / 3016.001: Machine Learning Workload Analysis and Characterization	❖Cory Davis working with Lizy John & Eugene John University of Texas Austin
3:30 – 4:30 pm	Poster Session	
4:30 – 6:00 pm	TAB Caucus (Industry Members Only)	
6:00 pm	End of Day 2	

❖ Student Presenter 💻 Remote Presenter

https://www.src.org/calendar/e007736/

Agenda – Day 3

- Presentations (30 minutes)
  - 25-minute presentations with 5-minute Q&A (live)
- Kick-offs (20 minutes)
  - 15-minute presentations with 5-minute Q&A (live)

All Times in PT

Wednesday, May 24th

9:00 – 9:10 am	Welcome / Introduction	Pan Marcus & John Oakley / SRC
9:10 – 10:10 am	3116.001: Strategies for Minimizing Trim Test Cost for Temperature Sensitive Circuits	Randall Geiger/ ❖Byrce Gadogbe / 💻Degang Chen Iowa State University
	2810.084: Soft and Hard Analog Fault Detection, Injection, Coverage, Diagnosis, and Localization Strategies Suitable for Production Test and In-field Test	❖Matthew Strong / 💻Degang Chen Iowa State University
10:10 – 10:40 am	3102.001: Quick and Thorough Design Verification of Hardware Accelerators	Subhasish Mitra / ❖Saranyu Chattopadhyay Stanford University
10:40 – 11:10 am	3197.001: Machine Learning for Testing Machine-Learning Hardware: A Virtuous Cycle	❖💻Jonah Chen / 💻Krishnendu Chakrabarty Arizona State University
11:10 – 11:25 am	Break	
11:25 – 11:55 am	2810.086: Machine Learning-based Functional Safety Improvement of AMS Components in Automotive SoCs	Kanad Basu University of Texas at Dallas
11:55 – 12:25 pm	3103.001 / 3104.001: Machine Learning for Cross-Level, Cross-Domain and Multi-Objective Optimizations	Jiang Hu Texas A&M University – College Station Yiran Chen Duke University
12:25 – 1:25 pm	Lunch	
1:25 – 1:55 pm	**Industry Talk:** More Scalable IC Design Workload Executions on the Hybrid Clouds	Gi-Joon Nam / IBM
1:55 – 2:25 pm	2810.087 / 2810.088: Grid Optimization and Silicon Validation for Chip Robustness	Farid Najm University of Toronto Chris Kim University of Minnesota
2:25 – 2:55 pm	3024.001: Quantum-Inspired CMOS Ising Accelerators	Chris Kim University of Minnesota
2:55 – 3:25 pm	3019.001: Hardware/Software Co-Designed Vector Dataflow Architectures for Energy-Minimal AI/ML	Nathan Serafin student of Brandon Lucia Carnegie Mellon University
3:25 – 3:35 pm	Break	
3:35 – 4:05 pm	2984.001: Silicon Photonics Artificial Intelligence Accelerators for Data Center Integration	Jaime Viegas Khalifa University
4:05 – 4:25 pm	3158.001 **(NEW START)**: Hardware Accelerator for Enabling High-Performance AI on Tiny Edge Devices	Priyanka Raina / ❖Kartik Prabhu Stanford University
4:25 – 6:00 pm	TAB Caucus (Industry Members Only)	
6:00 pm	End of Day 3	

SRC

https://www.src.org/calendar/e007736/

❖ Student Presenter 💻 Remote Presenter

Agenda – Day 4

- Presentations (30 minutes)
  - 25-minute presentations with 5-minute Q&A (live)
- Kick-offs (20 minutes)
  - 15-minute presentations with 5-minute Q&A (live)

All Times in PT

Thursday, May 25th

9:00 – 9:10 am	Welcome / Introduction	Pan Marcus & John Oakley / SRC
9:10 – 9:40 am	2988.001: A Hyperdimensional Learning System for Efficient, Robust and Secure Online Learning	Mohsen Imani University of California - Irvine
9:40 – 10:10 am	2987.001: Energy Efficient Adversarially Robust Deep Nets for Edge Platforms	💻Naresh Shanbhag / ❖💻Hassan Dbouk University of Illinois at Urbana-Champaign
10:10 – 10:40 am	3040.001: LoCal+SGD: Selective Localized Learning to Accelerate Training of Deep Neural Networks	💻Anand Raghunathan Purdue University
10:40 – 11:10 am	3021.001: HDnn: The Best of Both Worlds - CNNs with Hyperdimensional Computing	💻Tajana Rosing / ❖Weihong Xu University of California – San Diego
11:10 – 11:20 am	Break	
11:20 – 11:50 am	2983.001: Alternative Numbering Systems and Architectures for AI Edge Devices	Vasileios Sakellariou student of Thanos Stouraitis Khalifa University
11:50 – 12:20 pm	3018.001: Towards Efficient Parallelism, Resiliency and Security in Large Tiled Multicore Processors for AI Computing	❖Deniz Gurevin / 💻Omer Khan University of Connecticut
12:20 – 1:20 pm	Lunch	
1:20 – 1:50 pm	3020.001: Meta-Programming for Systematic Enhancement of Hardware Diversity targeting AI and HPC	Wayne Luk / ❖Jessica Vandebon Imperial college London
1:50 – 2:20 pm	3022.001: Design and Modeling of Machine Learning Hardware for Graph Processing	Sachin Sapatnekar / ❖Sudipta Mondal University of Minnesota
2:20 – 2:50 pm	2927.001: Benchmarking Automotive Workloads for Autonomous Driving	Radoyeh Shojaei student of John Owens University of California - Davis
2:50 – 3:20 pm	3023.001: Algorithm-Architecture Co-Design for Robust Deep Learning	Yuhao Zhu University of Rochester
3:20 – 3:30 pm	Break	
3:30 – 4:00 pm	2810.083: Automated Layout of Analog Arrays In Advanced Technology Nodes	Sachin Sapatnekar / ❖Nibedita Karmokar / 💻Ramesh Harjani University of Minnesota
4:00 – 5:00 pm	Poster Session	
5:00 – 6:30 pm	TAB Caucus (Industry Members Only)	
6:30 pm	End of Day 4	

❖ Student Presenter 💻 Remote Presenter

https://www.src.org/calendar/e007736/

Agenda – Day 5

- Presentations (30 minutes)
  - 25-minute presentations with 5-minute Q&A (live)

- Kick-offs (20 minutes)
  - 15-minute presentations with 5-minute Q&A (live)

All Times in PT

Friday, May 26th

9:00 – 9:10 am	Welcome / Introduction	Pan Marcus & John Oakley / SRC
9:10 – 9:40 am	2810.085: Applications of Circuit Transient Sensitivity Simulation to Semiconductor Circuit Analysis and Design	Ronald Rohrer Southern Methodist University
9:40 – 10:10 am	3112.001: Formal Analysis of System-on-chip Firmware Interactions	Sandip Ray University of Florida
10:10 – 10:40 am	3105.001: ProxyVM: A Scalable and Retargetable Compiler Framework for Privacy-Aware Proxy Workload Generation	❖Alif Ahmed / 💻Ashish Venkat University of Virginia - Charlottesville
10:40 – 11:10 am	2810.058: Machine Learning-Based Overkill/Underkill Reduction in Analog/RF IC Testing	❖Vineeth Niranjan / 💻Yiorgos Makris University of Texas at Dallas
11:10 – 11:20 am	Break	
11:20 – 12:10 pm	3160.004 **(NEW START)**: Inductive Fault Analysis for Determining Statistical Analog Test Metrics	Sule Ozev (VIDEO) Arizona State University
	2810.089: Techniques for Low-cost Design Test, and Calibration of RF MIMO Systems	Sule Ozev (VIDEO) / 💻Georgios Trichopoulos Arizona State University
12:10 – 1:10 pm	Lunch	
1:10 – 2:20 pm	TAB Caucus (Industry Members Only)	
2:20 pm	End of Review	

❖ Student Presenter 💻 Remote Presenter

https://www.src.org/calendar/e007736/

Thank You!

Opens?

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Marcus Pan
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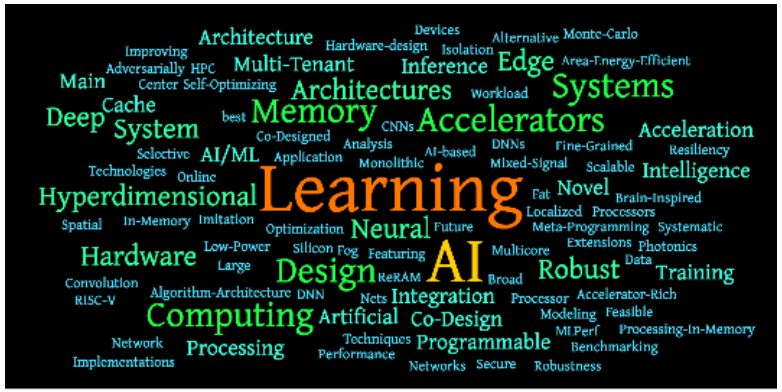
SRC

Artificial Intelligence Hardware Research Program

AIHW

"Creating new highly-efficient AI platforms to enable neuro-inspired, cognitive and learning abilities to address the vast range of future data types and workloads as intelligence is enabled from edge devices to the cloud."



Research Directions:

- Architectures for Power Efficient AI Acceleration
- Modeling, Analysis, and Simulation/Emulation of AI Hardware for Early System Exploration
- HW/SW Co-design of AI Compute Systems
- Fairness, Robustness, Privacy, and Explainability of Models and Algorithms for AI Hardware
- Interplay of AI and System Architecture/ Microarchitecture Design

SRC

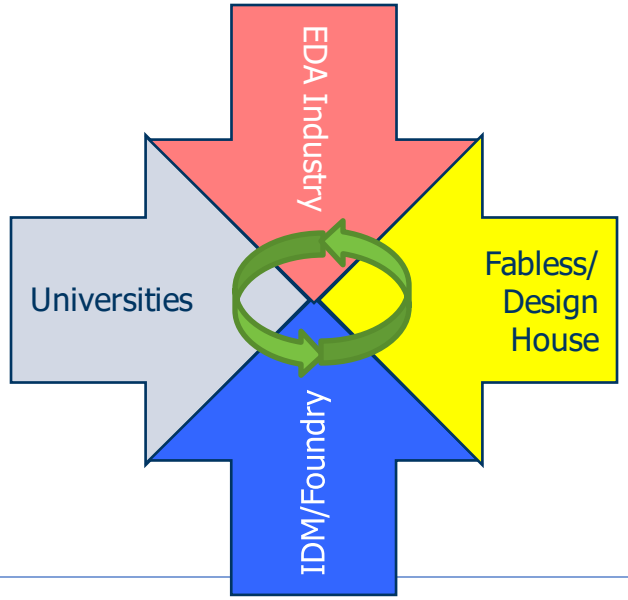
https://www.src.org/program/grc/aihw/

Computer-Aided Design and Test Research Program

"Computer-aided design and test are critical to extracting the highest performance from each technology node, poised to leverage new technologies—and needed to squeeze even more out of older technologies"

CADT

- Ever-growing design complexity: transistors, design rules, cores, defects, power management, reliability, correctness, testability, …
- Design methodology and CAD are the only way to address the design complexity challenge
- CADT address:
  - Designer productivity
  - Time to market
  - Heterogeneity
  - Emerging applications
  - System level complexity
  - Process complexity
  - Reliability
  - Power/energy management



Research Directions:

- Reduce cost and time to market, assuring design correctness and productivity
- Enable high level/high value design through advanced linkages to manufacturing
- Take full advantage of technology advances, anticipate future CMOS and post-CMOS challenges and advanced interconnects
- Address growing design complexity
- Make their way into member use, through direct adoption or through EDA vendors

https://www.src.org/program/grc/cadt/

SRC Liaison Program

Maximizing the Value of Participation

Move Yourself, Your Company and the Next Generation Forward

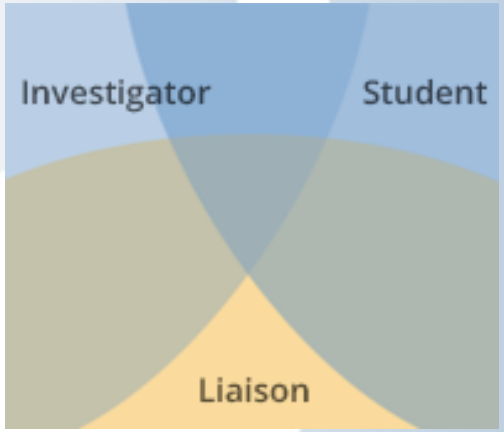
Develop the Workforce

- Provide relevant guidance for industry challenges
- Prepare students to enter industry or pursue future academics

Contribute to Research

- Encourage technology exchange between university and industry
- Bridge the conventional gap between academia and industry

Expectation to have regular PI-Liaisons calls at least one every 4-8 weeks



Academia Contributes to Industry

- Provide an out of the box approach to current problems which enhance industry research and development enables a differentiated product for the marketplace
- Provide an outside perspective adding diversity to the thought process of how best to attack a challenge

Access New Technology

- Gain valuable insights into problems and solutions that will ultimately impact industry competitiveness
- Provide an effective way to deliver actionable research results directly into their companies

Identify the Best

- Identify the most compelling research from current and recent research

SRC

https://www.src.org/liaison/

SRC's Amazing Community

Academics solving meaningful problems
Increase of tech transfer to industry
Clear investment Return Of Investments

SRC Program Manager

- Runs Advisory Board and aligns research
- Educates PI about requirements and responsibilities
- Encourages Liaison participation
- Finds opportunities for further engagement

University Principal Investigator

- Pursues ambitious, ground-breaking research
- Schedules regular calls, every 4-8 weeks
- Arranges meet-ups at conferences
- Presents research at annual reviews

Research Scholar

- Leads meetings
- Presents findings
- Aims to present at TECHCON
- Is knowledgeable about SRC members

Industry Liaison

- Provides industry perspective to PI
- Transfers technology & people into company
- Advocates for SRC research
- Coordinates with Advisory Board

SRC