

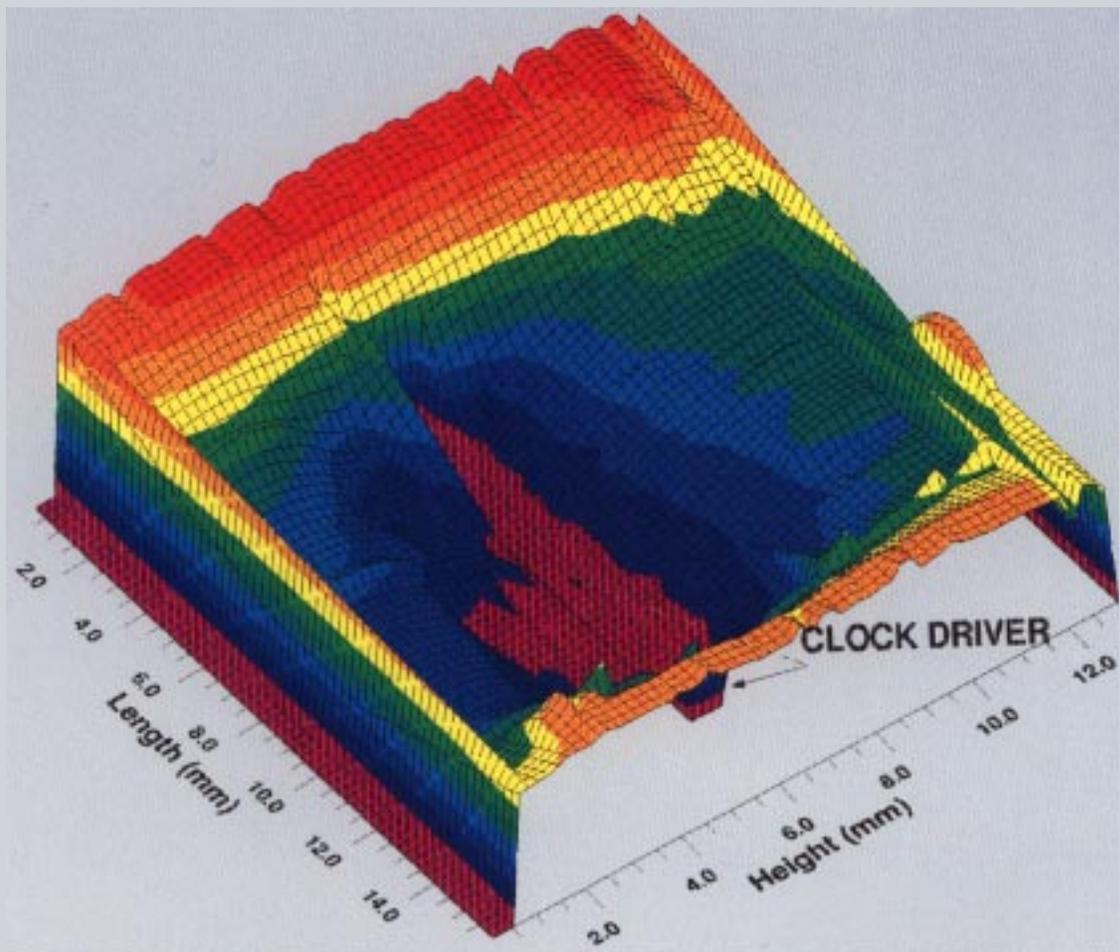
# 1991 Annual Report

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COOPERATIVE RESEARCH



*Delay as a function of chip location for Digital Equipment Corporation's Alpha chip. Computer-aided design software developed by SRC researchers at Carnegie Mellon University was used in Digital's Alpha and NVAX chip designs (see photo top of page 15).*

# ***Semiconductor Research Corporation***

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*In the cooperative research program of the Semiconductor Research Corporation (SRC), industry, government, and universities combine their talents and resources in a symbiotic relationship to address common goals.*

*These goals are defined by the SRC's mission, which is to advance technology and improve the education of scientific and engineering personnel in the semiconductor technologies important to the U.S. microelectronics industry and, thus, to improve the industry's competitiveness. The success of this mission is becoming increasingly evident with each passing year.*

# ***Executive Message***

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*During this past year, the SRC has continued to expand its value as the cooperative research arm of the North American semiconductor industry. The high quality of its products is leading to their rapid adoption by industrial users. More and more users are assuming that the flow of research results will always be available and are including the SRC in their strategic development plans. This, of course, was a major goal of the SRC; however, it creates additional challenges.*

*A company that looks to the SRC for essential needs must not forget that, in a consortia, the agenda can change. New needs, variable budgets, progress, and even the retirement of a researcher can lead to such changes, although, since the SRC's inception in 1982, few disruptive or unexpected changes have occurred.*

*Without a doubt, one of the reasons for the SRC's success is its ability, in important areas, to appropriately manage change. Companies can rely on the fact that, given reasonable performance, the research project in which they are interested will be active next year. Projects and tasks change, but always with good cause, ample warning, and an opportunity to object.*

*The ninth year of the SRC saw the creation of the three-volume management plan, which provides roadmaps for administrative operations and the research program both for the next year and the next decade. These are excellent guides.*

*Factors remain, however, over which the SRC has less direct control, such as future revenues and the progress of the technology. Leaders of the SRC — the Board of Directors, the Technical Advisory Board, and the corporate staff — must be constantly alert to these externalities and adjust to them. Permanent solutions to the endemic challenges faced by high technology industry are needed. The SRC is beginning to look like one of these.*

*During 1991, coordination of cooperative research and development efforts of the semiconductor industry improved. A major step forward was the formation of an Executive Technology Coordinating Group, currently chaired by Gordon Moore as the Chairman of the SIA Technology Committee and including the Presidents of SEMATECH and the SRC. Commitment to unify, as appropriate, the technology strategies of the SRC, SEMATECH, and the Micro Tech 2000 national technology strategy should position industry with a fully coordinated cooperative research and development effort.*

*An important guideline from these efforts is that the portion of the SRC's university research program dealing with manufacturing and process sciences will principally address needs of the "beyond-five-year" period of time. This will not change the nature of our research planning process significantly. The SRC, working with universities, recognizes that academic research is generally inefficient in directly addressing short-term needs. When this is attempted, it interferes with the education process.*

*What causes us to stop and think is that even with long-range goals and short-term graduate-student researchers, the output of the SRC research program is finding immediate short-term applications. Granted, some of these applications are in industry development efforts that will not be productized for several years, and others are in CAD where the attainment of long-range research goals requires that short-term needs be addressed. However, even beyond the development and CAD applications, rapid technology transfer is occurring in areas such as defect control, dielectrics, metallization systems, packaging, metrology and analysis, and processes, even though the research is ostensibly long-range; and no one wants to stop that from happening.*

*In applying total quality management (TQM) to the SRC, we see improvement in the research-to-product cycle time. This year the SRC began TQM analysis of not only the cycle time but also its procedures and*



*Mr. Sumney and Dr. Parker*

*those of others in the SRC research program. Our goal is to apply TQM techniques to insure that SRC customers are able to obtain and rapidly apply the highest quality, generic long-range research results.*

*The nature of research has always been to expect unexpected results. The nature of the SRC's applied research is that the primary long-range goals may be substantially altered by the continuous outward flow of knowledge, information, and creativity that meets short-range needs without being directed to that purpose. Someone noted that this results directly from the close industry-university interactions occurring through SRC reviews, workshops, mentoring, and other activities. This observation appears to be correct.*

*The SRC experience is one of outstanding success in facing its challenges to date. Success and events will present it with even greater challenges in the future.*

*Gerhard H. Parker  
Intel Corporation  
Chairman, SRC Board of Directors*

*Larry W. Sumney  
SRC President and  
Chief Executive Officer*

## **Member Companies**

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AT&T  
Advanced Micro Devices, incorporated  
Alcoa  
Control Data Corporation  
Digital Equipment Corporation  
E. I. du Pont de Nemours & Company  
E-Systems, Incorporated  
Eastman Kodak Company  
Eaton Corporation  
Etec Systems, Incorporated  
General Motors Corporation  
Harris Corporation  
Hewlett-Packard Company  
Honeywell Incorporated

IBM Corporation  
Intel Corporation  
LSI Logic Corporation  
Micron Technology, Incorporated  
Motorola, Incorporated  
NCR Corporation  
National Semiconductor Corporation  
Rockwell International Corporation  
Texas Instruments Incorporated  
Union Carbide Corporation  
Varian Associates, Incorporated  
Westinghouse Electric Corporation  
Xerox Corporation

## **Associate Members**

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Los Alamos National Laboratory  
Microelectronics and Computer Technology Corporation (MCC)  
Sandia National Laboratories  
SEMATECH, Incorporated

## **Affiliate Members**

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Advanced Technology Applications, Inc.  
Analogy, Inc.  
Arizona Packaging Software, inc.  
Dawn Technologies, Inc.  
Hampshire Instruments  
Hestia Corporation  
Integrated Silicon Systems, Inc.  
Intersonics, Incorporated  
Jamar Technology Co.  
Meta-Software, Inc.  
Mission Research Corporation  
nChip, Inc.  
Peak Systems, Incorporated  
Process Technology Limited  
Prometrix Corporation

QuanScan, Inc.  
Rapro Technology Inc.  
Sienna Technologies Inc.  
SILVACO Data Systems  
Solid State Equipment Corporation  
Solid State Measurements, Inc.  
SRI International  
Sunrise Test Systems, Inc.  
Technology Modeling Associates, Inc.  
Tech ware Systems Corporation  
Tyecin Systems Inc.  
Unit Instruments, Inc.  
VLSI Standards, Inc.  
WYKO Corporation

## **Participating U.S. Government Agencies**

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Army Research Office (ARO)  
Defense Nuclear Agency (DNA)  
National Institute of Standards and Technology (NIST)  
National Science Foundation (NSF)  
National Security Agency (NSA)  
Office of Naval Technology (ONT)  
Wright Laboratory

## Research Organizations

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*FATHER AND SON work on SK-funded research at Ohio State. Professor Carl Popelar, Principal investigator, looks over the shoulder of his son, Scott, as he prepares a slow crack growth specimen in their investigation of the long-term performance of polymeric dielectric materials.*

Arizona, University of  
Arizona State University  
Auburn University  
Boston University  
California at Berkeley University of  
California at Irvine, University of  
California at Los Angeles, University of  
California at Santa Barbara, University of  
California at Santa Cruz, University of  
California Institute of Technology  
Carnegie Mellon University  
Case Western Reserve University  
Clemson University  
Colorado at Boulder, University of  
Colorado State University  
Columbia University in the City of New York  
Cornell University  
David Sarnoff Research Center  
University of Florida  
Florida Institute of Technology  
Florida State University  
Illinois at Urbana-Champaign, University of  
Lehigh University  
Louisiana State University  
Maryland, University of  
Massachusetts at Amherst, University of  
Massachusetts Institute of Technology  
Michigan at Ann Arbor, University of  
Massachusetts Microelectronics Center  
Minnesota at Minneapolis, University of  
New Jersey Institute of Technology  
New Jersey University of Medicine and Dentistry  
New Mexico, University of  
North Carolina at Charlotte, University of  
North Carolina State University  
Northeastern University  
Ohio State University  
Princeton University  
Purdue University  
Rensselaer Polytechnic Institute  
Research Triangle Institute  
Rutgers, The State University  
Sandia National Laboratories  
South Florida, University of  
Southern California, University of  
Stanford University  
State University of New York at Albany  
Stevens Institute of Technology  
Texas at Austin, University of  
Texas A&M University  
Vanderbilt University  
Vermont, University of  
Virginia at Charlottesville, University of  
Virginia Polytechnic Institute  
Wisconsin at Madison, University of  
Yale University

# ***A Model of Collaboration***=====

*Since its inception in 1982, the SRC has contributed many very important things to the industry and to the nation's technology base. One of the most important of these is the SRC model for research cooperation which has worked better and produced more than any other in the high technology world.*

*The SRC was originally an experiment. It has become a proven paradigm, providing a framework for industrial companies and other organizations to combine their resources and support generic research. The SRC Model is outlined on the facing page.*

*Other contributions resulting from the application of this model include:*

- methodology for joint industry technology planning,*
- a highly productive university-industry partnership,*
- restoration of silicon-related research as a major focus of university research,*
- students who have graduated and joined the work force with skills and experience that make them instant contributors,*
- research results flowing into the industry that have buttressed industry's internal programs and have proven to be immediately applicable,*
- intellectual property being banked for future industry use,*
- a national R&D community that promotes, and works with other organizations to promote, national policies supportive of high technology competitiveness, and*
- education and curricula development initiatives.*

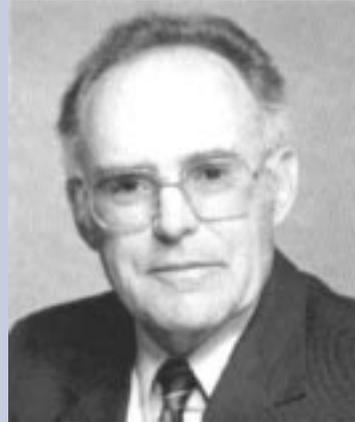
*These results have differing degrees of importance to various SRC participants. Every product is Number One on somebody's list.*

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## **The SRC Model**

- *A Concept and a Mission*
- *Articles of Incorporation and Bylaws*
- *Interaction with industry management*
- *Policy and Governance*
  - Board of Directors*
- *A Management Plan*
  - Mission and Outlook*
  - Research Strategy*
  - Research Operations*
- *An interactive Structure*
  - Technical Advisory Board*
  - University Advisory Committee*
  - Government Coordinating Committee*
  - Research contracts, reports, and reviews*
  - Member relationships*
  - Public relations and publications*
  - Technical meetings, workshops, and short courses*
- *Research Agenda*
  - Goals and roadmaps*
  - Product relevance*
  - Research management*
  - Technology leadership*
  - Industry mentoring*
- *Outreach*
  - Industry and government research groups*
  - Effective technical communication*
  - Dissemination and transfer of technology*
  - International semiconductor technology*
- *Funding*
  - Shared industry funding with government support*
- *Organization*
  - Small staff with low overhead*
  - Partial staffing by industry residents*
  - Efficient operation and management*
    - *plans, contracts monitors, and manages research*
    - *includes broad-based technical skills*
    - *carries out effective publication dissemination*
    - *uses existing research organizations/facilities*
    - *identifies trends and paradigm opportunities*



*"... the SRC has taught us how to work effectively in 'precompetitive' research with other competitors. These interactions were not easily learned, but they serve as a role model for how other industries could also interact to gain competitive advantage through early research collaboration. "*

*Gordon Moore  
Chairman of the Board  
Intel Corporation*

# ***The SRC Team***

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*The SRC cooperative research team consists of: (1) the organizations that define the agenda and provide resources, (2) the research performers from universities, and (3) the forty-some-person administrative and technical staff based at corporate headquarters in Research Triangle Park, North Carolina.*

*Stated another way, the SRC is a team of between 1500 and 2000 people. Several hundred of these are associated with member organizations and contribute to the SRC effort through the Board of Directors, the Technical Advisory Board, research mentoring, or participation in SRC meetings. They are scientists or engineers employed by industry other cooperative organizations, or government agencies. All have primary responsibilities within their organizations with limited effort focused on the SRC.*

*About one thousand members of the SRC team come from the universities where they either teach or study, and perform research. An increasing number of these university participants identify their efforts closely with the SRC and its industry-defined goals but, in most cases, the SRC is not their highest priority*

*The only team members whose full-time job is the SRC are those based at corporate headquarters. In addition to providing the ongoing support functions required for coordinating and managing the large team effort, the full-time staff provide the technical leadership and research integration that is essential to maintaining a quality research effort.*

*The challenge of cooperation is to provide all of the team members with something they value. In the case of semiconductor manufacturing-and-using organizations, this value consists of knowledge, data, software, and new hires. In the case of universities, value is associated with research support, with the guidance for this research that comes from the SRC, with the industry interaction that accelerates the application of research results, and with the provision of career opportunities for their graduates,*

*Since the team consists of many types and sizes of organizations, it is impossible to optimize the SRC's operations for any one segment. This applies to industry, government, and university participants. Attempts are continually being made by the SRC staff to respond to the real needs of participants and to thus strengthen their identity with the SRC team.*

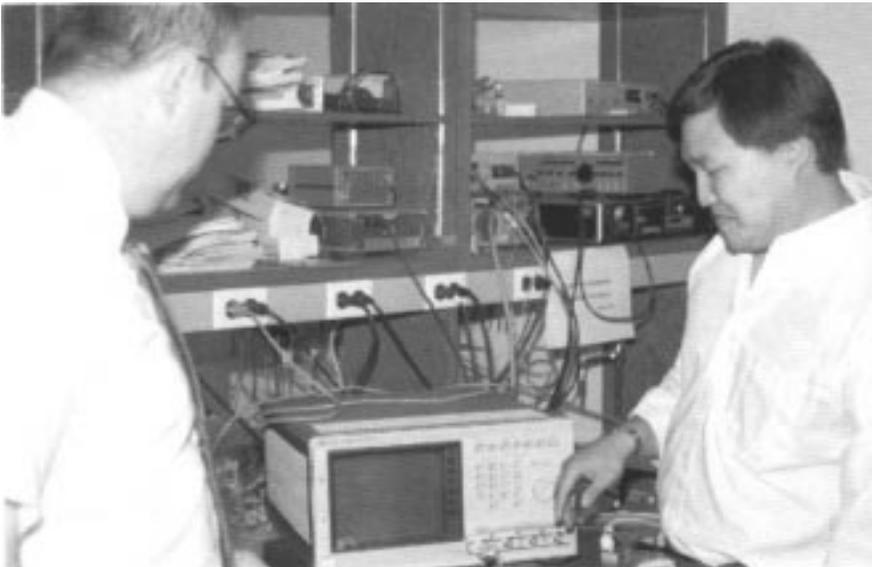
*Since the SRC is being considered as a model for cooperative activities, it is important that the model be continuously strengthened and improved. In the long run, the model that the SRC provides may be among the most important of all of its products.*



*Working group at the 1991 Summer Study of the Technical Advisory Board.*

*" . . . the SRC brings together the thinkers in semiconductor technology and establishes a vision for the industry "*

*Dr. Robert M. White  
Under Secretary for Technology  
U.S. Department of Commerce*



*Industry Mentor William E. Starks of Varian Associates meeting with Ph.D. candidate Steve T. Cho at the University of Michigan.*

# **The SRC Research Program**

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*The quality and productivity of SRC's cooperative precompetitive research program is derived from a management plan that*

- provides a policy and environment context for the research,*
- defines realistic goals based upon industry projections of its product needs in the next decade and upon trends in the enabling technologies for these products, and*
- identifies from these goals and from analyses of the technology, a set of research thrusts that describe specific areas in which additional knowledge and innovation are required by the industry.*

*Beyond this planning, research must retain the flexibility to explore promising new areas that develop and potentially high-payoff opportunities originating elsewhere, even when not included in its technology roadmaps.*

*In the most general terms, this planning process defines SRC global research objectives in terms of providing a generic technology base that enables participants to produce products that:*

- exceed industry trends in chip functionality, performance, and cost/functional element,*
- demonstrate increased chip reliability,*
- include improved design productivity, and*
- utilize enhanced packaging technologies.*

*This research objective is used to define more specific parametric goals relating to complexity performance, technology packaging, quality, cost, design efficiency, and factory performance. Research thrusts and subthrusts are then identified with these parametric goals. In 1991, eighteen thrusts were identified in this process:*

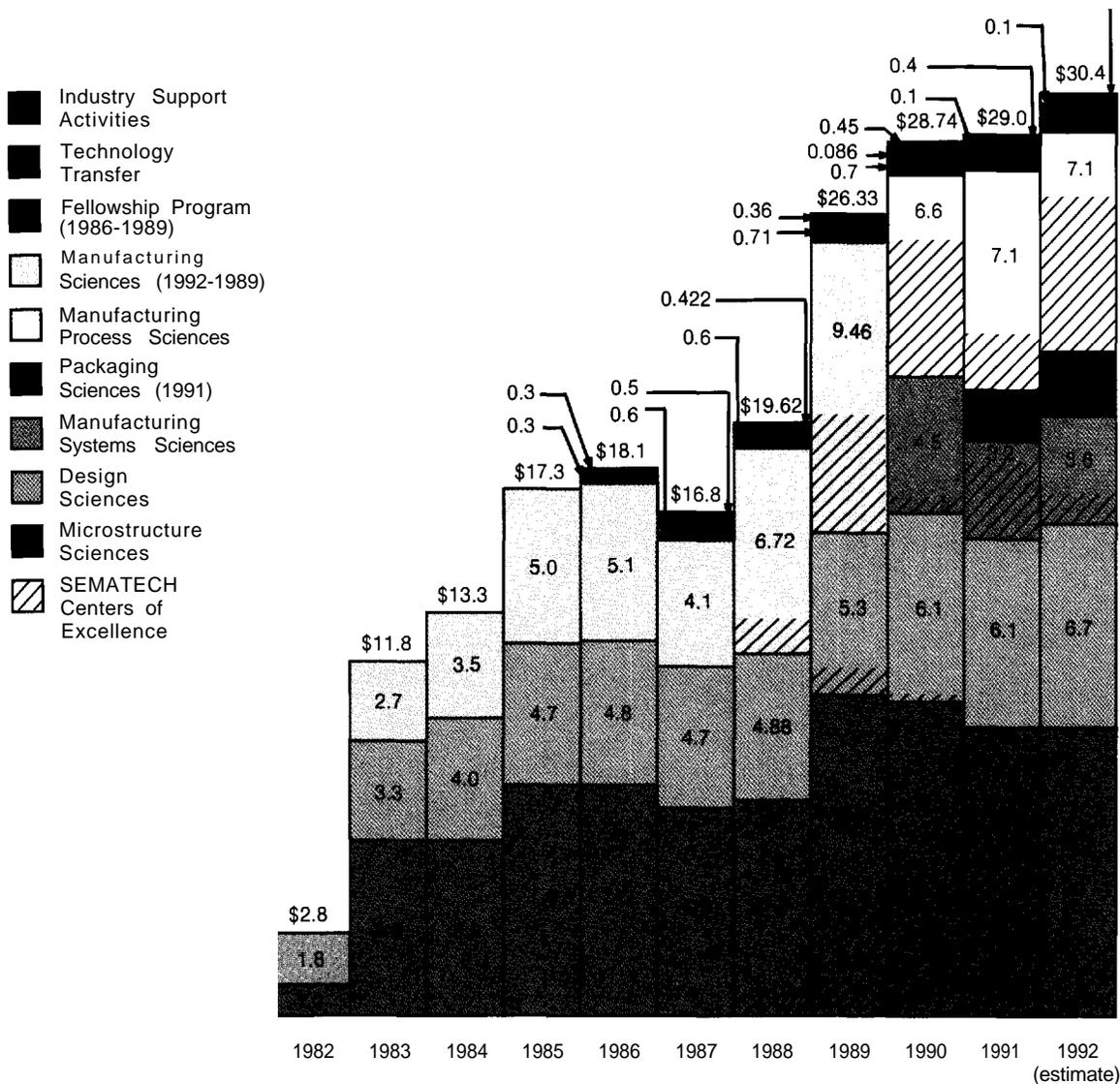
<i>advanced devices</i>	<i>multilevel interconnect</i>
<i>advanced technology</i>	<i>packaging</i>
<i>circuit design</i>	<i>physical design</i>
<i>contamination control</i>	<i>plasma etch</i>
<i>deposition</i>	<i>process and equipment</i>
<i>design synthesis</i>	<i>automation and control</i>
<i>design verification</i>	<i>product development</i>
<i>factory automation</i>	<i>environment</i>
<i>and control</i>	<i>reliability</i>
<i>lithography</i>	<i>technology CAD</i>
<i>metrology</i>	

*Each of these thrusts is further divided into subthrusts that are, in turn, correlated with contract tasks and the research budget.*

The SRC has created a large and productive university research program in U.S. universities that directly addresses the goals and needs of the semiconductor industry. This research has helped sustain U.S. leadership in the design of integrated circuits and in microstructures, and has created new productive university R&D directed to manufacturing technology and microelectronics packaging. An important and enhanced part of the SRC manufacturing research program is funded through SEMATECH.

The resultant interactive process that relates research activities of multiple universities with a broad industry is unique, and is an important national asset. The products of this process are the many specific research accomplishments described in the following pages that are now being beneficially applied by that industry.

Research Program Commitments  
(\$ in Millions)





*Testing phase of chips for research at the Ohio State University on analog CMOS/BiCMOS standard cells for VLSI signal processing applications under the direction of Professor Mohammed Ismail.*

## **Research Operations**

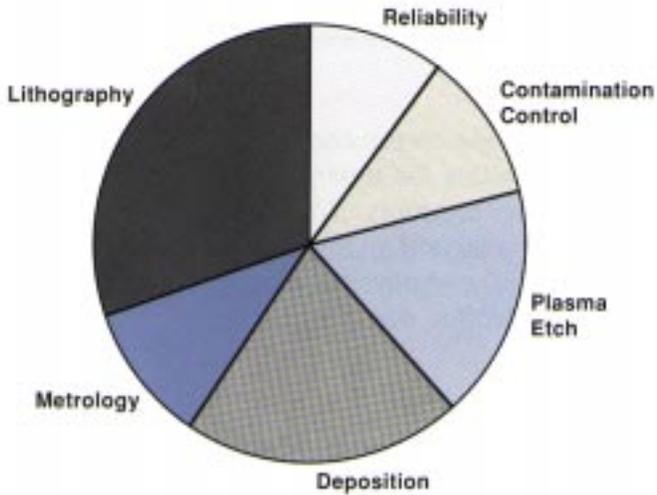
*Based on the Management Plan, the SRC implements and oversees an integrated program of applied research that is conducted primarily by faculty and graduate students in universities. The result is that the more than \$200 million which the SRC has committed to this research over the last decade has supported a solid majority of academic silicon-device-related research. In 1991, the research efforts of over 250 faculty and 700 graduate students at 56 research organizations were directed to SRC research goals.*

*Research is implemented primarily through research contracts. Three types of research activity are defined:*

- a "project", which involves a few faculty members and graduate students, is directed to specific needs, and is typically completed in a three-year period.*
- a "program", which requires a larger effort, is directed to a defined need requiring multiple tasks and typically requires five years or more before completion.*
- an "SRC Center-of-Excellence", which is the largest effort, is designated by the Board of Directors, addresses broad areas of needed research with tasks redefined annually in response to changing needs, and is recognized as a premiere institution for which the SRC intends to maintain substantial support.*

*These diverse university research efforts are managed by the SRC staff with annual reviews conducted with the Technical Advisory Board. As tasks and projects are completed, new research efforts are solicited in areas defined by the management plan. Opportunities are provided to all persons in the university research community who have relevant capabilities.*

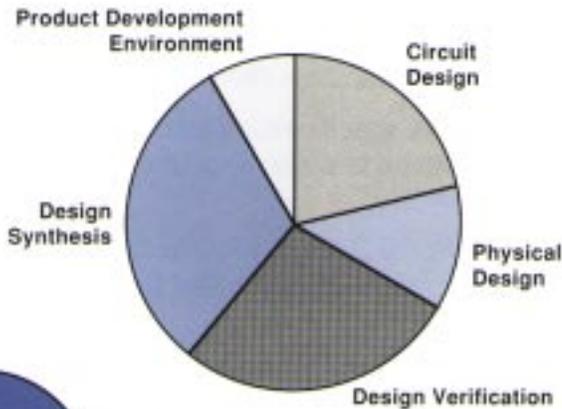
*The SRC research program has matured to the extent that a continuous stream of research results flows to its participating companies, and companies are finding that they can depend upon this cooperative research effort to meet many of their future needs.*



**Manufacturing Process Sciences**  
\$8.6 million

## The Science Areas

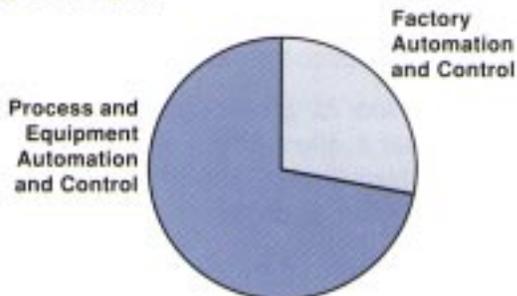
For management purposes, research in the SRC program is partitioned into the five science areas depicted by the accompanying pie charts. The segments of the pie charts represent the major technology thrusts. Embodied in the program are all the areas significant to microelectronic semiconductor technology, ranging from product design, through manufacturing, to packaging of the product. The large investment in Manufacturing Process Sciences is a direct result of the SEMATECH Center-of-Excellence program, which is funded by SEMATECH and managed by the SRC as an integral part of its research program.



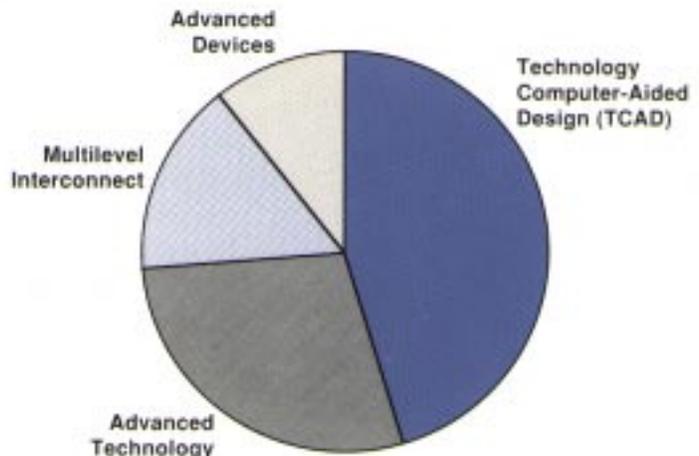
**Design Sciences**  
\$5.2 million



**Packaging Sciences**  
\$1.8 million



**Manufacturing Systems Sciences**  
\$3.2 million



**Microstructure Sciences**  
\$7.8 million

*A preponderance of projects in SRC Design Sciences research focuses on the challenge of providing the microelectronics industry with the seeds for the tools needed to translate the emerging submicron ULSI technological capability into timely marketable chip and system-level products. The current Design Sciences research portfolio contains major efforts in synthesis of digital and analog designs, test and design for testability advanced circuit design techniques, verification, and physical design. In addition, increasingly important research work is being done in design frameworks, which manage the complexity of the design process, itself.*

## **1991 Key Research Results:**

*A new timing simulation technique, Adaptively Controlled Explicit Simulation (ACES), for use in evaluating parasitic effects in ICs, in Multichip Modules, or on printed circuit boards.*

*Rapid Interconnect Circuit Evaluator (RICE) that exploits the treelike structure of interconnect networks to calculate interconnect models efficiently.*

*SpecCharts specification capture system that exploits a combination of state diagrams and the VHDL language.*

*HiTec/PROOFS fault simulation and test generation software, released and in use by several member companies.*

*BLIS 2.0, a mixed synchronous/asynchronous sequential logic synthesis software package that provides a complete architectural level synthesis environment.*

*Techniques for systematically designing phase-shifting masks, including predistortion to compensate for optical diffraction and proximity effects, proper biasing for submicron features, defocus effects, and verification procedures.*

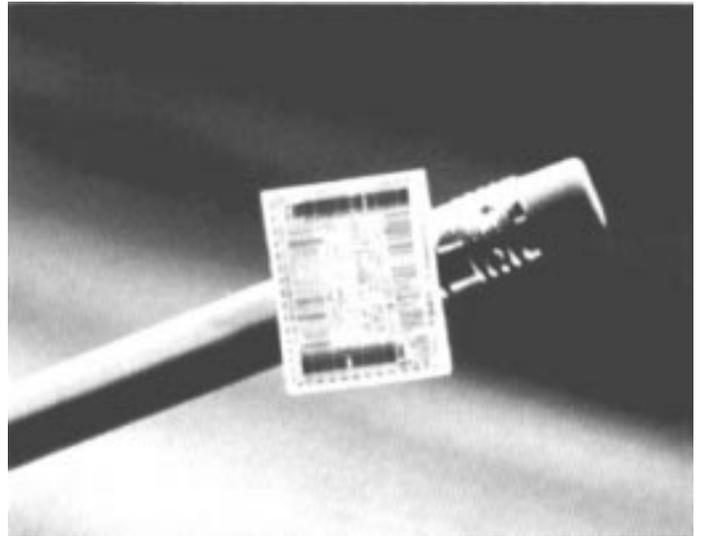
*Continuing development of BSIM3, a robust, physics-based, deep-submicron MOSFET model that is being incorporated into the circuit simulator Spice3.*

*SURF, a software tool for physical design of Multichip Module routing that successfully simulates and exploits lossy, unterminated transmission lines for interconnections between chips.*

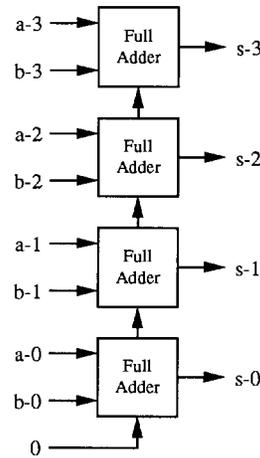
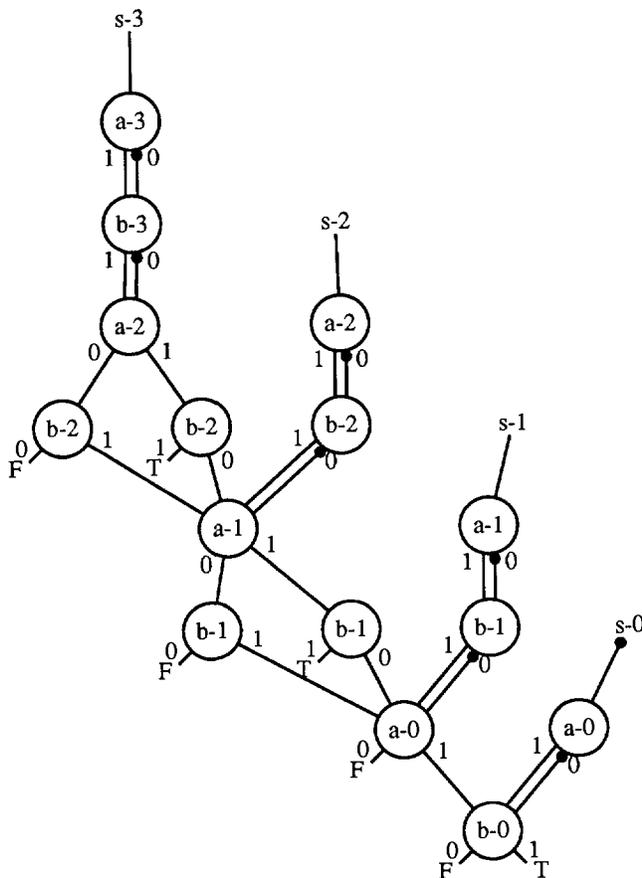
*Continuing development of a unified model for the analysis and synthesis of systems that will include hierarchical partitioning, reliability estimation, and high level models of systems combining both hardware and software.*

*"The AWESim ANAMOS, and COSMOS computer-aided design software developed at Carnegie Mellon were used in Digital's Alpha and NVAX chip designs. ANAMOS and COSMOS identified a number of bugs in these designs that were fixed before tape-out. They contributed significantly to the fact that these chips are functionally correct at the first pass."*

*Robert E. Caldwell  
Vice President  
Semiconductor Operations  
Digital Equipment Corporation*



*DIGITAL'S ALPHA CHIP: As can be seen in the photo, Digital Equipment Corporation's 21064 microprocessor is only slightly larger than a pencil eraser. This central processing unit (CPU) can be used to run all types of applications, from automatic teller machines to sophisticated aircraft simulations. It contains 1,700,000 transistors and can process as many as 400,000,000 instructions per second.*



*The two line drawings illustrate the Binary Decision Diagram (BDD) generated for an adder circuit. BDDs provide a canonical representation of Boolean functions. Given a translator netlist, the COSMOS symbolic simulator, developed at Carnegie Mellon with SRC funding, can generate BDDs describing the circuit function. By comparing these to ones generated from the system specification, the program can verify the correctness of the circuit.*

*BDDs have revolutionized the way Boolean equations are represented and manipulated. Professor Randal E. Bryant won IEEE's Baker Prize for the best paper in any IEEE transactions for this work.*

# **Microstructure Sciences**

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*SRC Microstructure Sciences research is directed toward the physics and chemistry of novel processes, materials, and devices, and their integration into industry-driven roadmaps. The major thrust areas are advanced technology advanced devices, technology CAD, and multilevel interconnect. The Microstructure Sciences strategy is to recognize opportunities for paradigm shifts that circumvent current technology limitations.*

## **1991 Key Research Results:**

- *Multidimensional (e.g., 3-D projection, isocontours, color mapping, and time progression) standardized formats for process/device visualizations and videos.*
- *Release of Version 1.0 of the Run-by-Run (RbR) Controller for adaptive optimization and control of processes, with verification on commercial stations.*
- *Advanced charge pump measurement techniques for quantitative measurements of post-stress lateral distributions of trapped charge and interface traps in MOSFETs.*
- *Thermodynamic/kinetic models for low energy incorporation of dopant atoms during vapor-phase deposition.*
- *3-D BiCMOS process with a dual gate fully depleted PMOS load in a chemical-mechanical polished epitaxial lateral overgrowth (ELO) film and with an area reduction of 3.5.*
- *2-D hydrodynamic (HD) model solutions that are self-consistent with a range of HD to DD (drift-diffusion) models and using MINIMOS as initiation driver for the 2-D HD simulation.*
- *Modification of the GILD (gas immersion laser doping) technique to achieve non-melt predeposition doping of shallow, lightly doped junctions.*
- *Demonstration of luminescence in short period  $Si_mGe_n$  monolayer superlattices, with RTA and hydrogen passivation to eliminate defect-induced luminescence.*
- *Creation of special grid support features that permit the integration of PISCES into the demonstration TCAD Framework.*

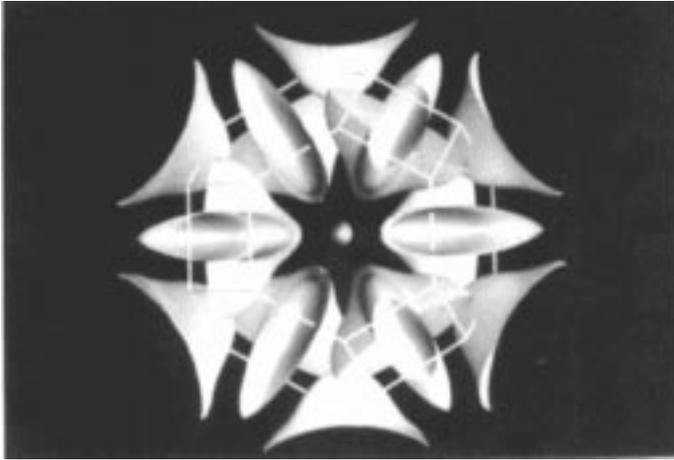


PHOTO ABOVE: The visualization team of the computational electronics group at the University of Illinois. Seated at the right is Professor Umberto Ravaioli. With him are graduate students (L to R) Alan Beck, Sridhar Iyer, and Franklin Bodine. They produced the two photos at left.

PHOTO TOP LEFT: The Brillouin zone for silicon, where an isosurface of the energy (approximately equal to 2eV) for the first conduction band is displayed as a function of the 3-D crystal momentum.

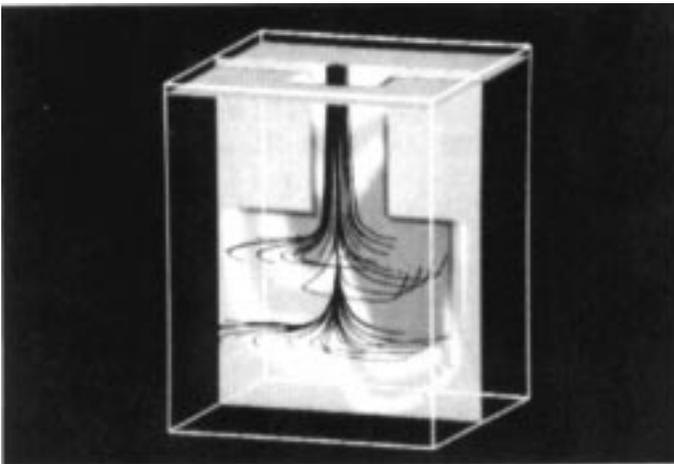
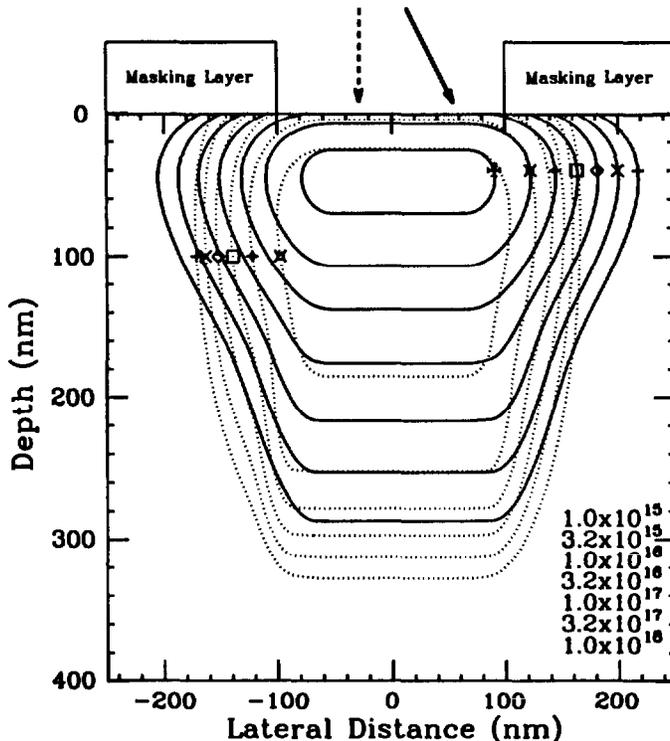


PHOTO CENTER LEFT: A particle tracing technique to generate streamlines, representing the hole current flux in a 3-D integrated bipolar transistor. The longitudinal cross-sectional plane shows a gray contour plot of the current magnitude. The emitter (top half) and the base (bottom half) of the transistor are shown here. The current blocking region in the emitter is clearly visible. The data are from a 3-D drift-diffusion simulation by Ronald Goossens and Robert Dutton of Stanford University.



Shown at the left are simulated two-dimensional, boron-implanted profiles in silicon at the edge of a masking layer. Compared are the isoconcentration contours of two profiles implanted with 15 keV, 30° rotation,  $1 \times 10^{13} \text{cm}^{-2}$  dose, and at 0° tilt (dotted line) and 7° tilt (solid line). They were simulated by the recently developed, computationally efficient 2-D boron implant model currently being retrofitted in SUPREM 4 under a project led by Professor Al Tasch, Jr., at the University of Texas at Austin. This model has explicit dependence on tilt angle, rotation angle, dose, energy, mask height, and mask orientation.

# **Manufacturing Process Sciences**

SRC Manufacturing Process Sciences explores the manufacturability of new processes and device structures and develops tools that can implement these processes and structures cost effectively. Research is divided into six thrusts: lithography metrology, contamination control, deposition, etch, and reliability. Examples of research under investigation are short-wavelength optical and X-ray lithography systems, optical methods to measure submicron features, evaluation of low thermal budget film deposition methods, in-situ and cluster-tool manufacturing approaches, impact of process radiation on device reliability, and the monitoring and control of contaminants in process reactors.

## **1991 Key Research Results:**

- *Accurate modeling and simulation of an X-ray proximity printing system which shows that features as small as 0.1  $\mu\text{m}$  can be printed with practical wafer-mask gaps on the order 10  $\mu\text{m}$ .*
- *Diffraction pattern produced by the latent image in exposed resist used to improve CD control by a factor of four over the conventional fixed-time exposure method.*
- *Two comprehensive references for the industry: "X-Ray Induced Damage in Silicon CMOS Circuits" and "Metal Contaminant Deposition on Silicon Surfaces from Solutions. "*
- *Implementation of equipment/process model and simulation of remote plasma-enhanced chemical vapor deposition to accelerate understanding of deposition in the cluster tool.*
- *Significantly enhanced detectability of particles on wafers at optical wavelengths by angularly resolved scattering.*
- *New method for on-line measurement and characterization of trace impurities in water.*
- *Simple absolute CD measurements of periodic structures on photo masks.*
- *Model that correlates the volume concentration of copper contamination in a solution with the resultant surface concentration on silicon wafers.*
- *Optical measurement of trenches in silicon as narrow as 0.45  $\mu\text{m}$ .*
- *Correlation of particle formation in reactors with potential wells.*
- *Measurement of wafer temperature to an accuracy greater than 0.5°C over the temperature range 10°C to 800°C using Moire interferometry.*



*Graduate student examines central wafer handler of North Carolina State University's cluster tool for low-thermal-budget, single-wafer, in-situ processing.*

# **Manufacturing Systems Sciences**

*SRC Manufacturing Systems Sciences research focuses on developing software and hardware tools, and the methodologies for their use, that will support flexible, cost-effective, integrated-circuit factories. Major research thrusts are directed towards the automated monitoring and control of wafer fabrication processes and equipment, and the efficient planning and scheduling of the flow of product through the factory.*

## **1991 Key Research Results:**

*CHIPS (Coherent Integrated Planning System) integrated-circuit factory simulation package successfully trialed at SEMATECH and an SRC member company. CHIPS concepts commercialized by a software supplier.*

*Highly sensitive integrated thermal microsensor technology transferred to commercial suppliers.*

*Initial version of the SPEEDIE plasma process simulator released for evaluation.*

*Several factory planning and scheduling concepts developed for the Berkeley Planning System (BPS) incorporated in to a worldwide production planning system at Harris Corporation.*

*Development of an initial version of the PREDITOR process simulation and yield prediction system.*

*An automated semiconductor equipment/process monitoring and diagnostic system, based on cumulative evidential reasoning.*

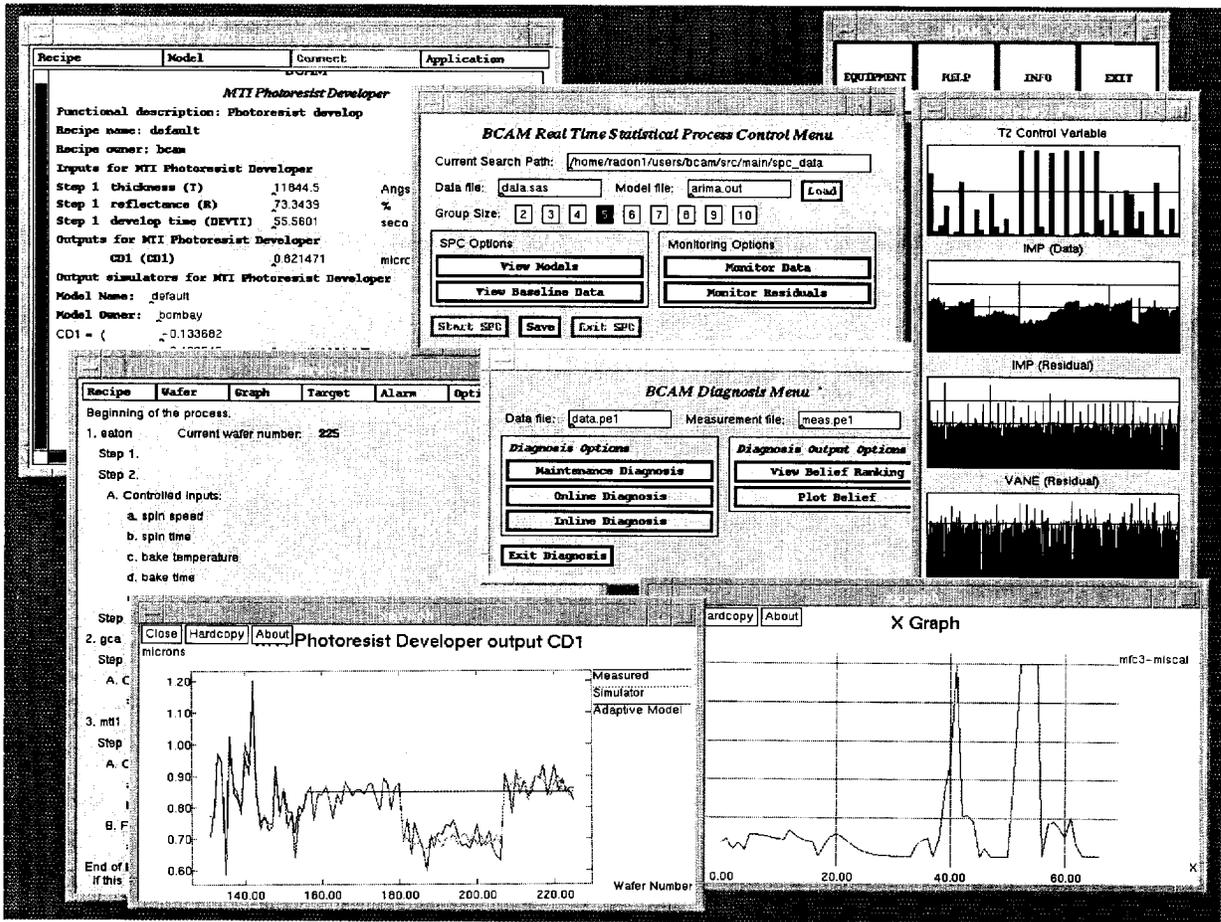
*Comparative costs and manufacturing process intervals modeled as a function of production volume for single-wafer, cluster-tool-based (versus conventional) IC factories.*

*Surface profile Fourier imaging system interfaced with image processing algorithms for enhanced image interpretation.*

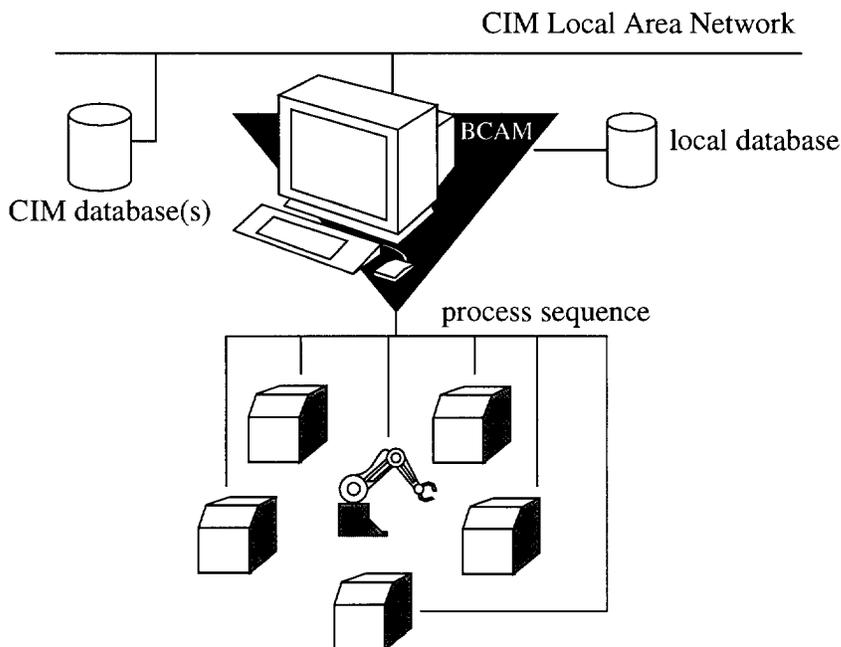
*Improved dynamic wafer temperature control for rapid thermal processing using a circularly symmetric heat source and associated control algorithms.*

*PHENOM equipment modeling methodology exercised on a chemical vapor deposition process at SEMATECH.*

*STADIUM software environment beta tested for the automated design and evaluation of manufacturing processes.*



The X-window interface of the Berkeley Computer-Aided Manufacturing (BCAM) Framework has been created to accommodate multiple applications, such as real-time statistical process control, run-by-run control, malfunction diagnosis, and recipe generation. Professors Costas J. Spanos, Lawrence A. Rowe, and Roger C. Glassey are the research Principal Investigators for the BCAM project at the University of California at Berkeley.



The Berkeley Computer-Aided Manufacturing (BCAM) System has been developed to take advantage of existing MIS systems to control a multistep semiconductor manufacturing process.

# **Packaging Sciences**

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*SRC Packaging Sciences research spans the breadth of technologies from those associated with system-level design concerned with functional partitioning, thermal management, signal interconnection, and power distribution to those associated with package materials, methods of construction, test methodologies and reliability. It is anticipated that Packaging Sciences will assume increased importance in the future.*

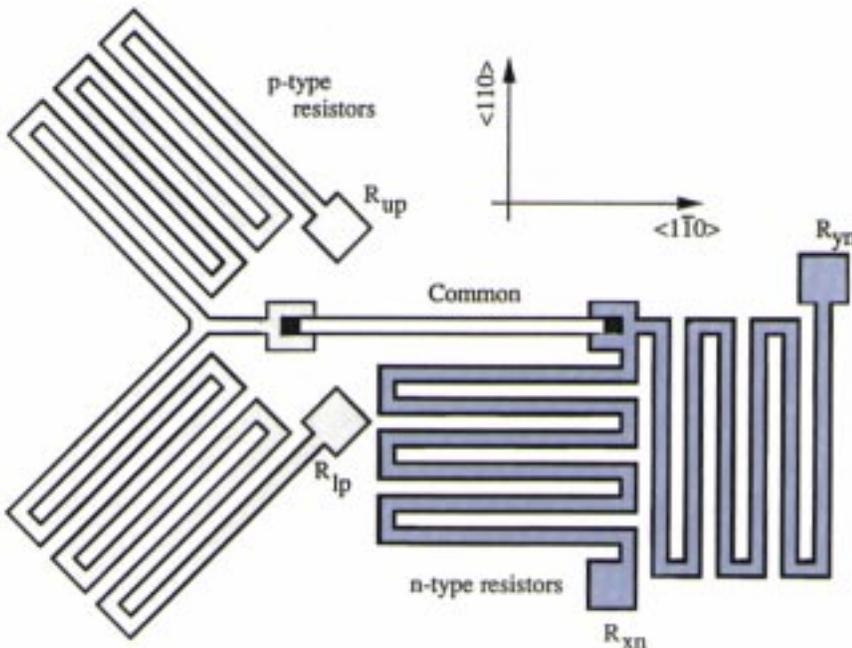
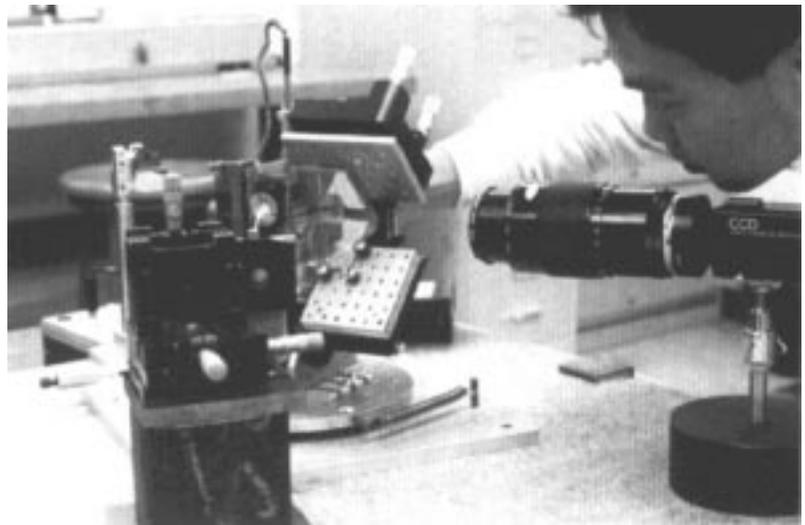
## **1991 Key Research Results:**

- *Completed and tested new three-dimensional capacitance modeling software tool.*
- *Switching noise calculation methods for CMOS and BiCMOS circuits developed and tested against SPICE.*
- *New version of package design software AUDiT.*
- *Improved ultraviolet-ozone method for cleaning surfaces prior to protective coatings against electrical leakage.*
- *CINDAS packaging materials database available in PC-compatible electronic format.*
- *High aspect ratio film transmission line structures successfully fabricated, modeled, and tested.*
- *Generic curves generated for slow crack propagation in polyimide films under mechanical stress.*
- *Piezoresistive silicon stress sensor design research completed.*
- *Techniques for making miniature (50  $\mu\text{m}$ ) solder joints for flip-chip attachment reliability testing.*
- *Prototype high frequency, flexible-diaphragm 'probe card' for verifying good chips prior to MCM assembly.*
- *Model for the thermal conduction through oxygen containing AlN surface layers.*



Ms. Josephine Chen and Ms. Gabriela M. Marinescu are shown verifying data at the Center for Information and Numerical Data Analysis and Synthesis (CINDAS) at Purdue University. They are part of a team which, under the direction of Professor C. Y. Ho, compiles evaluated data on the thermal, mechanical, electrical, and physical properties of selected microelectronics packaging materials for use by scientists and engineers in the SRC community. The CINDAS packaging materials database is available from the SRC library on diskettes for IBM PCs or compatibles.

Shown at the right is the experimental moire interferometry setup at Lehigh University used to measure thermally induced strain in microelectronics packages for a project directed by Professor A. Voloshin.



A piezoresistive strain gauge design for an Auburn University project under the direction of Professor Richard C. Jaeger.

# **Technology Transfer**

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*The SRC has made a strong commitment to expedite the transfer of technology from its university-based research program to practical uses by its industry members and participating government agencies. Because the SRC research program functions within the framework of the U.S. university system, the academic community's mechanism for research evaluation through peer-reviewed publications and/or presentations is strongly encouraged. In addition, a variety of mechanisms are used to create opportunities for person-to-person interaction among participants from industry, government agencies, and research organizations. Primary among these mechanisms are an Industrial Mentor Program and SRC-sponsored events.*

## **1991 Key Technology Transfers:**

- *Design/manufacturing technology from thermal imaging integrated sensor transferred to a commercial fabrication facility.*
- *EVOLVE — a feature scale, predictive, software module for CVD step coverage.*
- *Modeling and analysis tools for package design being used by several companies.*
- *HiTec/PROOFS testing software methodology formed nucleus for a new start-up company.*
- *Design of precursor delivery systems and low-temperature copper CVD process chambers.*
- *Many concepts and capabilities of the Coherent IC Planning System (CHIPS) transferred to a supplier of manufacturing modeling software for incorporation in to a commercial offering.*
- *AUDiT packaging design tool evaluated by industry.*
- *UMDFET — a 2-D submicron device simulator that incorporates an energy transport model.*
- *The RICE (Rapid Interconnect Circuit Evaluator) software package transferred to several member companies and used in the design of a number of products, resulting in several orders of magnitude reduction in simulator computer time.*
- *Concepts behind the Berkeley Planning System (BPS) transferred to industry and embedded in a worldwide planning system for integrating circuit order inputs and assigning production loading to multiple fabrication facilities.*



*Pictured above are members of the technology transfer team from the Florida Institute of Technology demonstrating the STADIUM TCAD software tool. The team has been carrying out an SRC project on Transfer of Advanced Technology to the Semiconductor Industry. Shown from left to right are Professor Thomas Sanders (project Principal Investigator), Mr. Dale Means (researcher), Mr. Jose Calvino (graduate student), Professor Roger Manley (School of Business), and Mr. Pat Begley from Harris Semiconductor.*



*In 1991, nearly 1300 new university research documents were added to the SRC library. More than 15,000 copies of these documents were sent, on request, to the staff of organizations participating in the SRC. Seventeen new video tapes were also added to the library. A majority of the tapes are presentations by university researchers, who discuss emerging technology for the benefit of scientists and engineers at participating companies and government agencies.*

## **1997 SRC Courses, Conferences, and Workshops**

### **Technology Transfer Course**

*TimberWolf Suite of Automatic Layout Software*

### **Topical Research Conferences**

*Integration of Novel Processes*

*Curricula Development for Courses in Microelectronics Manufacturing Engineering*

*Package Design and Simulation*

*Packaging Materials and Measurements*

*Process Architecture Design:*

*Technology CAD Tools*

### **Video Conferences**

*Contamination Issues in ULSI Manufacturing*

### **Workshops**

*Computer-Integrated Manufacturing for Integrated Circuits*

*Formal Verification*

*Ion Beam Projection Lithography*

*Real-Time Tool Controllers*

*Reliability*

# **Intellectual Property**

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The SRC identifies and protects selected intellectual property resulting from both the research it funds and the projects it manages on behalf of SEMATECH. The number of resulting patents is limited by budgetary constraints that require prioritizing inventions so only those with the highest potential are fully protected. Patent applications or software copyrights were filed for many of the 1991 Key Research Results listed on the preceding pages. In December, 1991, the SRC Board of Directors authorized the Technical Excellence Award as a complement to the Inventor Recognition Award that was established in 1986. The new award is shared among the researchers under SRC contracts who contribute to technology that significantly enhances the productivity of the U.S. semiconductor industry

## **1991 Inventor Recognition Awards**

Each researcher contributing to work under an SRC contract that results in a U.S. Patent application is honored with an SRC Inventor Recognition Award. Following are the titles of the 1991 U.S. patent applications, for which 38 recognition awards were presented.

- *CD Measurements of Periodic Structures on Photomasks (New Mexico)*
- *Depositing a Liquid Film on Surfaces within a Subatmospheric Pressure Chamber (Research Triangle Institute)*
- *Differential Cascade Operational Amplifier (Carnegie Mellon)*
- *Diffraction Light from Latent Images in Photoresist for Exposure Control (New Mexico and Sandia)*
- *Electron Energy Distribution Function in a Plasma Processing Source (Princeton)*
- *Generic Cell Controller for Computer-integrated Manufacturing System (Michigan)*
- *Laser Absorption Spectroscopy Using Fringe Rejection Technique (Stevens Institute of Technology)*
- *Oxynitride Dielectric for Use in Submicron Devices and Structure (Texas at Austin)*
- *Reactive Ion Etching of Copper Using a SiCl<sub>4</sub>-Based Plasma (Rensselaer)*
- *Reactive Membrane Filtration and Purification of Gases (Arizona)*
- *Selective Epitaxial Growth/Triple Self-Aligned Bipolar Junction Transistor (Purdue)*
- *Self-Aligned Dual-Gated SOI MOSFETs (Purdue)*
- *Surface Activation for Selective Metal Deposition (Texas at Austin)*
- *Synthesis of TiN Films by Nitridation Spin-on Oxide (Cornell)*

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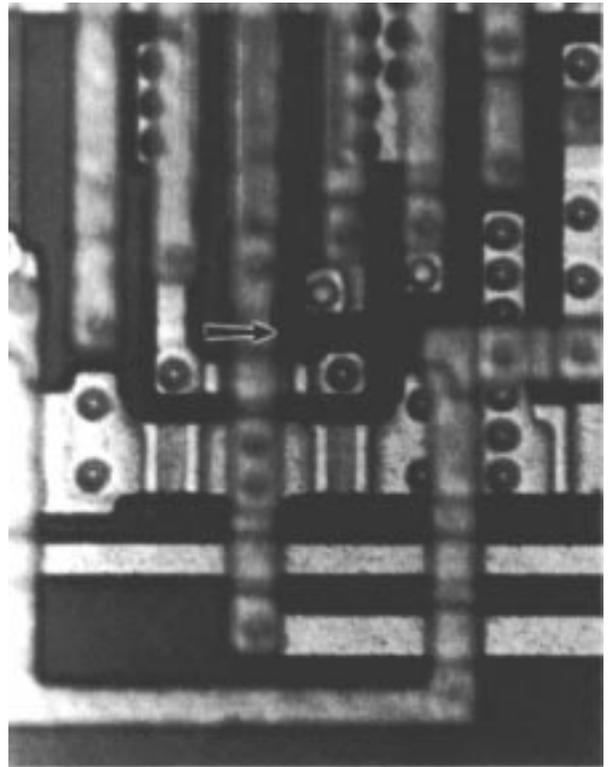
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## 1991 Key Software

- *AWESpice* — general tool for efficient and accurate simulation of interconnect problems (Professor Rohrer, Carnegie Mellon)
- *BLIS2.0* — Behavior to Logic Interactive Synthesis, version 2 (Professor Brayton, California at Berkeley)
- *CARAFE* — fault extraction software (Professor Ferguson, California at Santa Cruz)
- *ILLIADS-R* — ILLinois Analogous Digital Simulator, R-version that handles reliability simulation of very large circuits (Professor Kang, Illinois)
- *iSPLICE3* — mixed analog/digital simulator (Professors Hajj and Saleh, Illinois)
- *RICE* — Rapid Interconnect Circuit Evaluator (Professor Pillage, Texas at Austin)
- *TimberWolfMC* — automatic layout package, version 6 (Professor Sechen, Yale)

## 1991 U.S. Patents

- *Built-In Current Testing of Integrated Circuits* (Professor Maly, et al.; Carnegie Mellon)
- *Hot-Carrier Suppressed Submicron MISFET Device* (Professor Tasch, et al.; Texas at Austin)
- *Measurement of Ultrafine Particle Distributions* (Dr. Ensor, et al.; Research Triangle Institute)
- *Merged Bipolar and Insulated Gate Transistors* (Professor Reif, et al.; MIT)
- *Monolithic Silicon Thermopile Infrared Detector* (Professor Wise, et al.; Michigan)
- *Optically Pumped Step Quantum Well infrared Source* (Professor Wang, et al.; UCLA)
- *Static RAM Memory Cell Using N-Channel MOS Transistors* (Professor Maly, et al.; Carnegie Mellon)
- *Sputter Encased Reentrant Microcapillary Channels and Interface* (Mr. Paal, Ph.D. candidate, Stanford)
- *Triode Plasma Reactor with Phase Modulated Plasma Control* (Professor Thomas, et al.; Stevens Institute of Technology)



In research directed by Professor Wojciech Maly at Carnegie Mellon University, it was determined that significant improvement could be achieved in the efficiency of current testing to detect abnormalities in integrated circuits by using Built-In Current (BIC) sensors instead of off-chip current measurements. In 1991, Professor Maly received a U.S. patent for this innovative technology. The photo above shows the layout of a segment of an IC with an artificially created defect (indicated by arrow) that was used during the performance evaluation of the 18-transistor BIC sensor implemented on the same chip.

# Financial Report

## BALANCE SHEET

3100 Snowtree Court Suite 900 Telephone 919 678 5700  
Post Office Box 55-15 Facsimile 919 676 5337  
Raleigh, NC 27625

Price Waterhouse



### Report of Independent Accountants

March 13, 1992

To the Board of Directors  
of the Semiconductor Research Corporation

In our opinion, the accompanying balance sheet and the related statements of revenue, expenses and changes in fund balance and of cash flows present fairly, in all material respects, the financial position of the Semiconductor Research Corporation (SRC) at December 31, 1991 and 1990, and the results of its operations and its cash flows for the years then ended in conformity with generally accepted accounting principles. These financial statements are the responsibility of the SRC's management; our responsibility is to express an opinion on these financial statements based on our audits. We conducted our audits of these statements in accordance with generally accepted auditing standards which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for the opinion expressed above.

Membership fees are determined based on certain formulae and, in the interest of preserving the confidentiality of the underlying information, are computed separately by each corporate member. Our testing of these fees consisted primarily of direct confirmation of the self-assessed amounts with certain members.

*Price Waterhouse*

DECEMBER 31,  
1991 1990

### ASSETS

Current assets:	\$ 1,986,805	\$ 3,552,179
Cash and cash equivalents	6,991,528	7,197,113
Marketable securities (Note 2)		
Membership fees receivable (net of allowance for doubtful accounts of \$0 in 1991 and \$230,000 in 1990)	25,645	1,982,750
Other current assets	270,919	75,749
Due from SEMATECH, Inc.	38,495	35,694
Due from SRC Competitiveness Foundation (Note 6)	12,380	59,164
Total current assets	<u>9,325,772</u>	<u>12,902,649</u>
Leasehold improvements	16,180	—
Computer equipment	531,093	701,545
Furniture and fixtures	308,075	157,120
	855,348	858,665
Less - accumulated depreciation	<u>(307,375)</u>	<u>(543,712)</u>
	547,973	314,953
Note receivable from SRC Competitiveness Foundation (Note 6)		450,000
Other noncurrent assets	45,492	48,920
Total assets	<u>\$ 9,919,237</u>	<u>\$13,716,522</u>

### LIABILITIES AND FUND BALANCE

Current liabilities:		
Research contracts payable	\$ 4,496,274	\$ 7,764,631
Accounts payable and accrued expenses	220,706	492,884
Due to SRC Competitiveness Foundation (Note 6)	6,068	—
Total current liabilities	4,723,048	8,257,515
Fund balance	5,196,189	5,459,007
Total liabilities and fund balance	<u>\$ 9,919,237</u>	<u>\$13,716,522</u>

## Notes

The accompanying notes are an integral part of these financial statements

### NOTE 1 - DESCRIPTION OF ORGANIZATION AND SUMMARY OF SIGNIFICANT ACCOUNTING POLICIES:

#### Background

The Semiconductor Research Corporation (SRC) is a not-for-profit organization formed in 1982 to conduct research in the fields of engineering and physical science related to semiconductor development and manufacture. Activity has centered around initiation and administration of contract research with various institutions and universities. The SRC has expended approximately \$170,153,000 since inception through December 31, 1991, relating to fellowship, contract research and grant expenses. The SRC's charter requires that member corporations, which are all corporations involved in the manufacture, use or sales of semiconductors, be assessed membership fees based on a percentage of their semiconductor sales, use or manufacture. These fees are subject to certain limitations.

In 1988, the SRC created other classes of membership which allow organizations and companies otherwise not eligible for membership to join the SRC. Associate and affiliated members must undertake research and development of semiconductor devices within the United States; they have similar privileges of membership except they do not have direct representation on the Board of Directors.

#### Computer equipment, furniture and fixtures

Computer equipment and furniture and fixtures are recorded at cost, and depreciation is calculated using the straight-line method over estimated useful lives of five years

#### SEMATECH revenue

Revenue from SEMATECH, an associate member, IS recognized quarterly based on anticipated expenditures related to approved contract commitments for the succeeding quarter.

#### Grant revenue

Revenue from unrestricted grants is recognized upon receipt.

#### Contract research and grant expense

The SRC accounts for contract research when qualified costs are billed by the recipient in accordance with the terms of the contract document. Unrestricted grants are expensed at the time the grant is awarded.

#### Income taxes

The SRC is exempt from federal income taxes under Section 501 (c) (6) of the Internal Revenue Code. An examination by the Internal Revenue Service of the SRC's tax exempt status is currently underway. The outcome of this examination is unknown at this time.

#### Cash and cash equivalents

Cash equivalents consist of various short-term investments, which are recorded at cost which approximates market value.

#### NOTE 2 - MARKETABLE SECURITIES:

Marketable securities consist of investments in U.S. Government obligations recorded at the lower of cost or market value. Market value was approximately \$169,000 and \$57,000 greater than cost at December 31, 1991 and 1990, respectively. With respect to December 31, 1991, these investments mature from 1993 to 1998 and bear interest at rates ranging from 6.875% to 7.875% (7.25% to 8.00% at December 31, 1990).

#### NOTE 3 - OPERATING LEASES:

In October 1988 the SRC entered into a non-cancelable lease for office space; the lease expires in October 1995 and has minimum rental payments as follows:

1992	\$ 294,385
1993	303,216
1994	312,312
1995	266,735
	<u>\$ 1,176,648</u>

Rent expense was approximately \$278,000 and \$277,000 for 1991 and 1990, respectively.

**STATEMENT OF REVENUE, EXPENSES  
AND CHANGES IN FUND BALANCE**

	YEAR ENDED 1991	DECEMBER 31, 1990
<b>Revenue:</b>		
Member fees	\$22,493,787	\$20,668,721
Associate member fees (Note 6)	10,784,910	12,781,780
Affiliate member fees	32,209	15,142
Grant revenue	925,000	1,265,885
Investment income	<u>966,227</u>	<u>707,103</u>
Total revenue	<u>35,202,133</u>	<u>35,438,631</u>
<b>Expenses:</b>		
Contract research and grants	29,935,368	29,845,662
Cash contribution to the SRC Competitiveness Foundation (Note 6)	950,000	
General and administrative	4,441,278	4,142,517
Depreciation	<u>138,305</u>	<u>138,206</u>
Total expenses	<u>35,464,951</u>	<u>34,126,385</u>
<b>Revenue net of expenses</b>	(262,818)	1,312,246
<b>Fund balance, beginning of year</b>	<u>5,459,007</u>	<u>4,146,761</u>
<b>Fund balance, end of year</b>	<u>\$ 5,196,189</u>	<u>\$ 5,459,007</u>

**STATEMENT OF CASH FLOWS**

	YEAR ENDED 1991	DECEMBER 31, 1990
<b>OPERATING ACTIVITIES:—</b>		
Revenue net of expenses	(\$ 262,818)	\$ 1,312,246
Adjustments to reconcile revenue net of expenses to net cash provided by operating activities:		
Depreciation	138,305	138,206
Forgiveness of note receivable	450,000	
Loss on disposal of fixed assets	55,767	1,424
Decrease (increase) in membership fees receivable	1,957,105	(1,500,389)
Decrease (increase) in receivable from SRC Competitiveness Foundation	52,852	(40,569)
(Increase) decrease in receivable from SEMATECH, Inc.	(2,801)	2,347,849
(Increase) decrease in other current assets	(195,170)	5,236
(Decrease) increase in research contracts payable	(3,268,357)	1,744,214
(Decrease) increase in accounts payable and accrued expenses	(272,178)	169,937
Decrease (increase) in employee note receivable	<u>3,428</u>	<u>(48,920)</u>
<b>NET CASH (USED) PROVIDED BY OPERATING ACTIVITIES</b>	<u>(1,343,867)</u>	<u>4,129,234</u>
<b>INVESTING ACTIVITIES:</b>		
Proceeds from sale of fixed assets		33,817
Acquisition of fixed assets	(427,092)	(118,902)
Decrease (increase) in marketable securities	205,585	(3,330,204)
(Increase) in note receivable		<u>(250,000)</u>
<b>NET CASH USED BY INVESTING ACTIVITIES</b>	<u>(221,507)</u>	<u>(3,665,289)</u>
<b>NET (DECREASE) INCREASE IN CASH AND CASH EQUIVALENTS</b>	(1,565,374)	463,945
<b>CASH AND CASH EQUIVALENTS, BEGINNING OF YEAR</b>	<u>3,552,179</u>	<u>3,088,234</u>
<b>CASH AND CASH EQUIVALENTS, END OF YEAR</b>	<u>\$ 1,986,805</u>	<u>\$ 3,552,179</u>

**Notes (continued)**

The accompanying notes are an integral part of these financial statements

**NOTE 4 – BENEFIT PLANS:**

The SRC has a defined contribution retirement plan covering all employees. Expense under this plan was approximately \$286,000 and \$264,000 for 1991 and 1990, respectively. A deferred compensation plan was established in 1985; the expense of this plan was approximately \$123,000 and \$111,000 for 1991 and 1990, respectively.

**NOTE 5 – COMMITMENTS:**

The SRC has research contracts and grant commitments outstanding of approximately \$14,772,000 at December 31, 1991. These commitments represent active research contracts and grants entered into through December 31, 1991, less expenses incurred by the SRC on the related contracts. During the period January 1, 1992, through March 13, 1992, the SRC committed to additional contracts and grants aggregating approximately \$11,062,000. The SRC may, at its option, terminate any contracts and commitments upon sixty days' written notice. Termination, however, would not occur without due reason, justification and negotiation of contract close-out costs as well as bridging costs for SRC-funded graduate students, as appropriate.

The SRC membership agreement stipulates that members commit to financial support of SRC on a

rolling three-year period based on an annual fee schedule. The fee schedule stipulates that the maximum one-year decline in a member's fee shall not exceed 30%. As of December 31, 1991, the minimum three-year membership fee commitment to the SRC, assuming all members' fees declined at the maximum rate of 30%, would be approximately \$34,000,000.

**NOTE 6 – RELATED PARTIES:**

In 1988 the SRC Competitiveness Foundation (SRCCF) was formed to promote educational programs and focus resources towards increasing the competitiveness of the domestic semiconductor industry. As of December 31, 1990, SRCCF had borrowed \$450,000 from the SRC to fund its operations. An additional \$500,000 was advanced to the SRCCF during 1991. During 1991, the Board of Directors forgave the funds borrowed and advanced from the SRC. This forgiveness was recorded as expense by the SRC and as income by the SRCCF.

The SRCCF administers the Graduate Fellowship Program with funds provided by the SRC. For the year ended December 31, 1991 and 1990, the SRC had provided through its contract research programs approximately \$776,000 and \$852,000, respectively, in support of fellowships. At December 31, 1991, \$6,068 was due to the SRCCF from the SRC for unpaid fellowship expenses.

The SRC shares offices and administrative support with the SRCCF. At December 31, 1991 and 1990, \$12,380 and \$59,164, respectively, was due to the SRC for reimbursement of costs paid by the SRC on behalf of SRCCF. The SRC expects payment in full in 1992 of all amounts due from SRCCF.

In 1987 SEMATECH was formed as a not-for-profit research organization to improve the available technology associated with the manufacture of semiconductors in the United States. All members of SEMATECH are required to be members of the SRC. In 1988 SEMATECH and the SRC entered into an agreement under which they will work collaboratively to identify areas of semiconductor manufacturing technology which could benefit from research performed by various institutions within the United States. The SRC solicits proposals for and manages these research contracts which are ultimately funded by SEMATECH. In 1991 and 1990 the SRC recognized revenues of approximately \$10,335,000 and \$12,405,000, respectively, from SEMATECH of which \$9,139,000 and \$10,877,000, respectively, was used by the SRC to fund research contracts identified under the agreement with SEMATECH. A revision of the invoice and billing process caused approximately 52,300,000 of 1989 SEMATECH funds to be recorded as 1990 revenue of the SRC.

# University Advisory Committee

<b>Lex A. Akers</b> Arizona State	<b>Lynn F Fuller</b> R.I.T.	<b>David V. Kerns Jr.</b> Vanderbilt	<b>R. Fabian W. Pease</b> Stanford	<b>Herbert H. Sawin</b> M.I.T
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<b>Jerry G. Fossum</b> Florida	<b>Ralph J. Jaccodine</b> Lehigh	<b>James W. Mayer</b> Cornell	<b>Ronald A. Rohrer</b> Carnegie Mellon	<b>Timothy N. Trick</b> Illinois
<b>James F. Freedman</b> SRC	<b>Richard C. Jaeger</b> Auburn	<b>Shyam P. Murarka</b> Rensselaer	<b>Thomas J. Sanders</b> F.I.T	

Cynthia Grotz (SRC), Committee Secretary

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<b>Defense Nuclear Agency</b> Lewis M. Cohn	<b>National Security Agency</b> Kermit Speierman*	<b>Wright Laboratory</b> William J. Edwards
<b>NIST</b> Frank F. Oettinger	<b>Office of Naval Technology</b> James A. Cauffman	

Richard D. LaScala (SRC), Committee Secretary

★ Committee Chairperson  
 ★★ Committee Vice Chairperson  
 ★★★ TAB Co-Chairperson

# Technical Advisory Board

## TAB Executive Committee

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<b>Delco Electronics</b> Edward G. Whitaker	<b>IBM</b> E. Hal Bogardus Paul Landler	<b>Micron Technology</b> Tyler Lowrey	<b>National Semiconductor</b> John M. Pierce Court Skinner	<b>SEMI/SEMATECH</b> Sam Harrell
<b>Digital Equipment</b> Ken Bano Kenneth M. Brown	<b>Intel</b> John t?. Carruthers Michael Garner	<b>Motorola</b> Kenneth J. Polasko Kenneth Ray	<b>NC State University</b> Nino A. Masnari	<b>SRC</b> James F. Freedman***
<b>Harris</b> W. Dale Edwards		<b>NCR</b> Jack Mullins	<b>Rockwell international</b> John D. Bastian	<b>Texas Instruments</b> Robert R. Doering P. B. Gbate

Cynthia Grotz (SRC). Committee Secretary

## TAB Design Sciences Committee

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<b>Alcoa</b> Anil Agarwal	<b>Harris</b> William Terry Coston	<b>LSI Logic</b> Daniel Wong	<b>NSF</b> Bernie Chern	<b>Sunrise Test Systems</b> Charlie Cump
<b>Analogy</b> fan Getreu	<b>Hewlett-Packard</b> James Duley	<b>MCC</b> Noel R. Strader	<b>National Security Agency</b> Dennis Heinbuch	<b>Texas Instruments</b> Paul Kollaritsch
<b>AT&amp;T</b> Basant Chawla	<b>Honeywell</b> Larry Bashaw	<b>Meta-Software</b> Shawn Hailey	<b>National Semiconductor</b> Tom Jones **	<b>Westinghouse Electric</b> Vincent Zagardo
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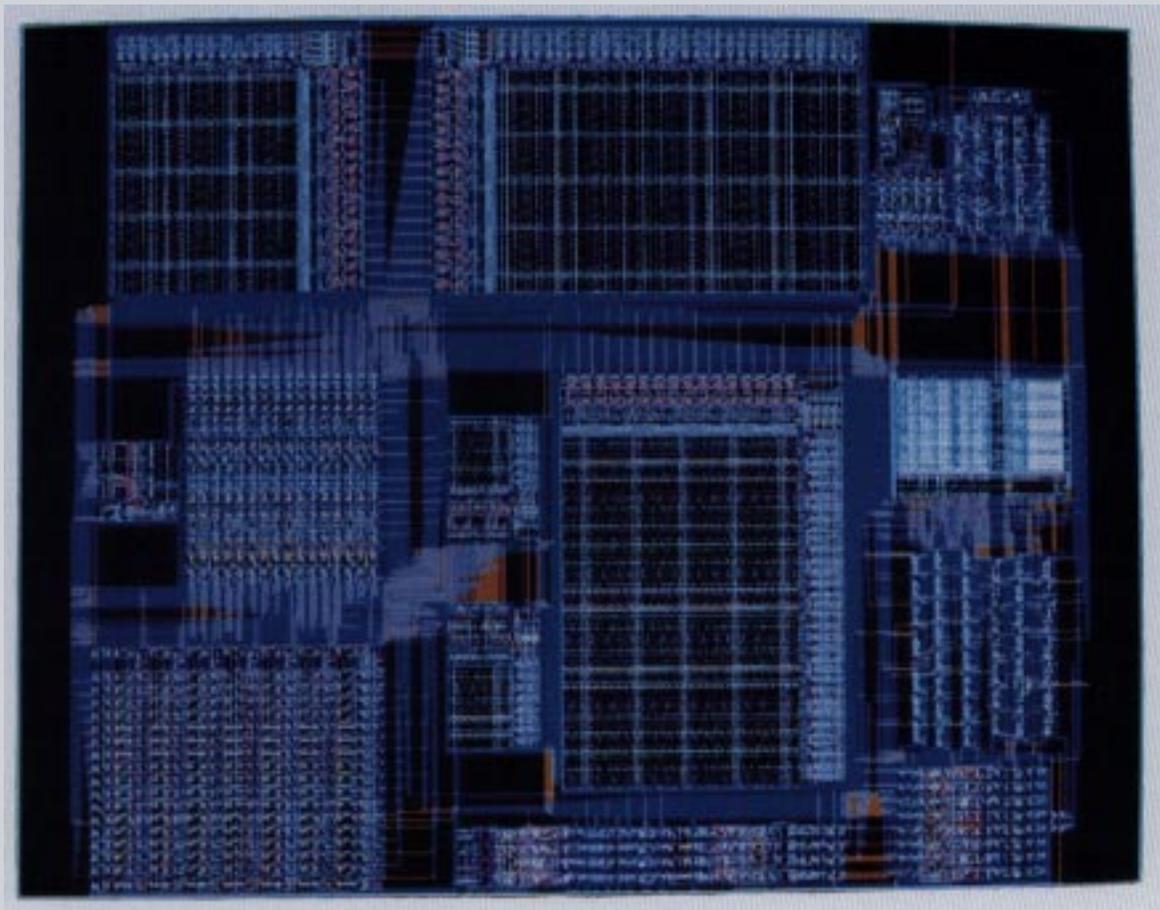
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*Example of successful use of Carnegie Mellon University's System Architect's Workbench (SAW) by General Motors. This is a shot of a chip layout done using a commercial silicon compiler backend, from input generated, via synthesis, by SAW.*



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