

Semiconductor Research Corporation
1993 Annual Report

Strategic

Research for

Global

Competitiveness



Cooperative Research

Mission

It is the mission of the Semiconductor Research Corporation (SRC) to solve the technical challenges required to keep the United States number one in the global semiconductor industry.

Goals

The goals of the SRC are to:

Champion research tasks consistent with the Semiconductor Industry Association's (SIA) technology roadmap.

•

Serve as a communication forum for SRC participants and the semiconductor industry.

•

Maximize the satisfaction and return on investment of SRC participants.

Objectives

To accomplish these goals, the SRC will:

Work with the semiconductor industry to develop and implement a research strategy.

•

Transfer results of this research rapidly to SRC-participating companies and organizations.

•

Educate scientists and engineers in areas relevant to industry needs.

•

Exhibit technical leadership.

•

Leverage the research investment of SRC participants.

Be the world's best research management organization.

Message from the President and the Chairman

Semiconductor technology is the driving force of the information age. To maintain leadership and competitiveness, the North American semiconductor industry is faced with formidable technological and manufacturing challenges. Significant progress toward meeting these challenges has been made over the last decade. The Semiconductor Research Corporation (SRC), the industry's first cooperative research venture, believes additional progress can best be achieved through strategic planning and continuous improvement in teamwork among industry, academia and government.

Through unique cooperative relationships forged among these three groups, the SRC's research and its technology transfer programs, aligned with the vision of the Semiconductor Industry Association (SIA) technology roadmap, are playing a key role in providing technical solutions to SRC-participating companies and organizations and to the industry as a whole.



Larry W. Sumney

Technology Transfer

Maximizing the satisfaction and return on investment of SRC participants was established as a main goal of the SRC in 1993. To accomplish this goal, the SRC has helped open channels of communication throughout the industry, directed a comprehensive program of semiconductor research, and provided participants with a significant return on their investment by transferring results of this research to them. Some of these research results are described in this Annual Report.

In 1993, the SRC leveraged participant research dollars by funding and managing more than \$30 million in research contracts at 62 major North American universities and research institutions. Sixteen patents were issued in 1993 as a result of SRC-sponsored research, demonstrating the SRC's commitment to provide its participants with access to new technical ideas and concepts. The SRC also educated numerous scientists and engineers in industry-relevant curricula, supporting more than 750 students at 56 universities.

Complementing these activities is the SRC's concurrent technology transfer system, a unique merger of technology transfer and total quality management activities. This system ensures that the SRC continues to provide outstanding research management services to its participants.



William T. Siegle

Roadmap for the Future

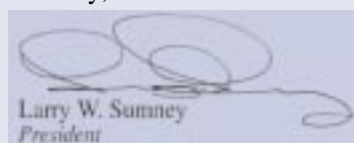
The SRC has made significant contributions to North American semiconductor industry competitiveness since its formation by SIA in 1982. This record of success in improving industry-wide, generic, precompetitive research and providing scientific leadership resulted in SRC research roadmaps, which were incorporated this year into the SIA technology roadmap.

This roadmap is a national technology research and development plan that serves the needs of all SRC participants by providing researchers in industry, academia and government with a clear picture of the industry's long-term technology needs. The strong relationships among industry, university and government, fostered by SRC research, are instrumental in the implementation of the roadmap.

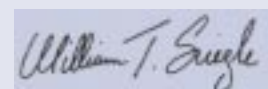
The SRC wishes to thank the many individuals – scientists, engineers, managers and other personnel from SRC-participating companies and organizations – who helped make 1993 a success. In 1994, the SRC looks forward to further enhancing relationships among industry, university and government, strengthening the research program, continuing to optimize the alignment of this program with the SIA roadmap, filing new patents, communicating research benefits and transferring technology to SRC participants.

Beyond this, the SRC wants to examine strategic directions that can best enable it to satisfy its customers into the next century. The SRC will continue improving its processes and making optimal use of available resources both to ensure the future health of the North American semiconductor industry and become the best research management organization in the world.

Sincerely,



Larry W. Sumney
President



William T. Siegle
Chairman

Overview of the SRC

*Planning,
Directing and Funding
the Semiconductor
Industry's Long-Term
Research*

The Semiconductor Research Corporation, a consortium of more than 60 semiconductor industry companies and government agencies, plays a crucial role in planning, directing and funding the industry's long-term research. The SRC, headquartered in Research Triangle Park, N.C., plans and implements an integrated program of basic and applied pre-competitive research conducted by faculty and graduate students at leading universities and research institutions. Through the SRC, businesses, government agencies and universities work together to advance semiconductor technology capabilities.



Since its formation in 1982, the SRC has invested and managed more than \$250 million in semiconductor research.

The SRC has reinitiated semiconductor research at North American universities. In the early 1980s the SRC was the dominant funding source for semiconductor research at these universities. Today, the SRC leverages research funding from a variety of sources, including industry, and state and federal governments.

The SRC has invested and managed more than \$250 million in semiconductor research since its formation by the Semiconductor Industry Association in 1982. SRC research dollars have supported hundreds of faculty members and more than 1,000 graduate students hired by the semiconductor industry. As part of the SRC's concurrent technology transfer system, more than 950 meetings have been held, and more than 8,000 research reports have been published. The SRC has been responsible for 62 patents issued and another 119 applications on file.

The semiconductor industry's cooperation in the SRC research program has resulted in:

- Nationally unified research goals for key science areas critical to the semiconductor industry, which have been incorporated into the SIA's technology roadmap;
- Improved relationships among industry, academia and government;
- Graduate students educated in the needs of industry, who are becoming leaders in the industry; and
- Timely and effective transfer of research results to SRC participants for commercialization.

Through their work on SRC-funded research, more than 100 engineers and scientists enter the workforce each year with a background in microelectronics. In 1993, the SRC supported 771 students at 56 universities. Overall, researchers who have been associated with the SRC account for about ten percent of all electrical and computer engineering Ph.D.s granted each year.

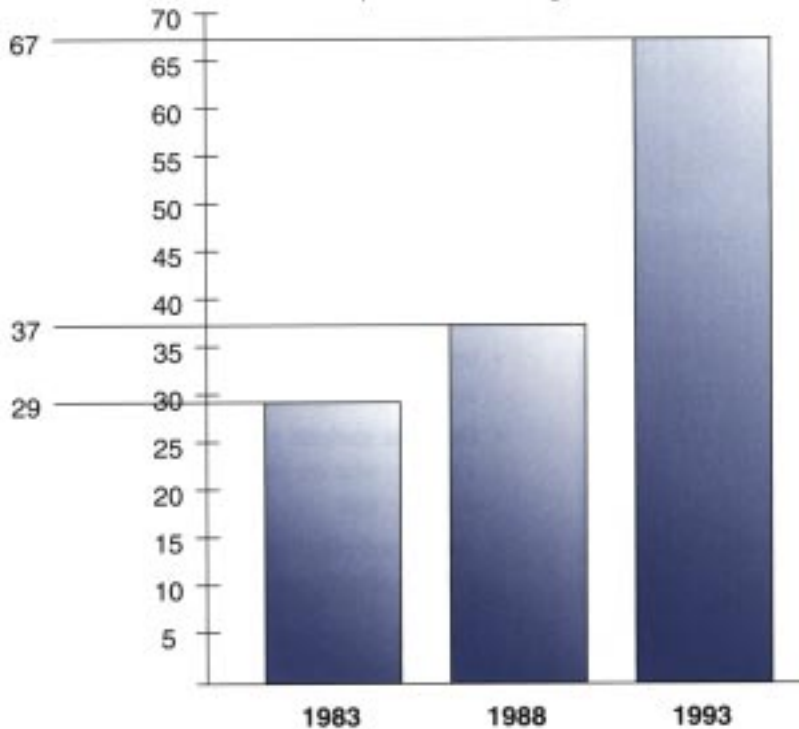
SRC-Participating Companies and Organizations

*Leveraging R&D
Investments into
Global Competitiveness*

The SRC's strength comes from its ability to bring industry relevance to university research and to transfer research results quickly from universities and research organizations to industry for commercialization.

The SRC's participating companies, organizations and government agencies make these technological advances possible. More than 60 companies and government agencies fund the SRC's work, leveraging their own research and development dollars to achieve a substantial return on their investment.

Number of SRC-Participating Companies and Organizations



The SRC was pleased to continue working with these members in 1993:

Members

Advanced Micro Devices Inc.
Alcoa
AT&T
Digital Equipment Corporation
E. I. du Pont de Nemours & Company
Eastman Kodak Company
Eaton Corporation
E-Systems Inc.
Etec Systems
General Motors Corporation
Harris Corporation
Hewlett-Packard Company
Honeywell Inc.
IBM Corporation
Intel Corporation
LSI Logic Corporation
M/A-COM
Motorola Inc.
National Semiconductor Corporation
Northern Telecom
Praxair Inc.
Rockwell International Corporation
Texas Instruments Inc.
Westinghouse Electric Corporation

Associate Members

Los Alamos National Laboratory
MCC
SEMATECH
The MITRE Corporation

U.S. Government Participants

Army Research Office
National Institute of Standards and
Technology
National Science Foundation
National Security Agency
Naval Surface Warfare
Center – Crane
Office of Naval Research
Wright Laboratory

Affiliate Members

AG Associates
Analogy Inc.
Arizona Packaging Software Inc.
CVC Holdings Inc.
Dawn Technologies
DTX/Thermacore Inc.
Famtech International
Hestia Technologies Inc.
Ibis Technology Corporation
Integrated Electronics Innovations Inc.
Integrated Silicon Systems Inc.
Meta-Software Inc.
Mission Research Corporation
nCHIP Inc.
PDF Solutions
Phenix Semicron Corporation
Process Technology Ltd.
Prometrix
Q-metrics Inc.
SILVACO Data Systems
Solid State Measurements Inc.
SRI International
Sunrise Test Systems
Technology Modeling Associates Inc.
Techware Systems Corporation
Tyecin Systems Inc.
Verity Instruments Inc.

New Participants in 1993

In 1993, the SRC welcomed six new affiliate members:

ANACAD Electrical Engineering Software Inc.

Santa Clara, CA

Develops advanced circuit design software for the EDA market.

BTA Technology Inc.

Santa Clara, CA

Develops CAD tools for IC characterization, design and manufacturing. President and CEO Boon-Khim Liew was a 1992 SRC Technical Excellence Award winner.

Essential Research Inc.

Cleveland, OH

Develops models and software tools for thin-film processing and vacuum-system design.

Matrix Integrated Systems Inc.

Richmond, CA

Produces plasma etchers and strippers.

MEREX Corporation

Tempe, AZ

Develops management tools for semiconductor companies in areas of workplace education, needs assessment, technical writing systems and workplace interaction.

Solid State Systems Inc.

Santa Clara, CA

Designs and manufactures semiconductor products specified to customer's linear applications.

SRC and the National Technology Roadmap for Semiconductors

*Providing Leadership
to Chart the Industry?
Future Course*

“With the SIA roadmap, for the first time our industry has a set of documents, carefully, constructed by a broad constituency, which lay out the steps needed to move ahead. We have an extraordinary opportunity to rally our efforts around the roadmap.”

William T. Siegle, Chairman, SRC



SRC participants meet in Washington, D.C. to discuss industry needs with key decision-makers.

There is a growing recognition by policy makers, industry leaders and academic researchers that the economic future of North America lies in the hands of the developers of enabling technologies for leading-edge products.

In November 1992, 179 of the country's leading integrated circuit (IC) technologists assembled at the SIA Technology Workshop in Irving, Tex., to create a common vision of the course of semiconductor technology for the next 15 years. The group included semiconductor industry scientists and engineers, suppliers and customers, as well as representatives of the SRC, SEMATECH, government agencies, national laboratories and universities.

Building on the technology vision previously set forth by the SRC, SEMATECH and others, the assembled technologists created a roadmap that clearly defines the industry's research and advanced technology needs for the next 15 years. The summary report of this meeting was released in March 1993.

By providing decision-makers and technologists with information on the important needs of the industry for the next 15 years, the roadmap enables better investment decisions, decreases the gaps in technology efforts and brings about a better-balanced, coordinated, national technology effort.

The strategic direction of the SRC's research program is defined in the SIA roadmap, yet this program is not static. It will be carefully assessed every two years and redirected as appropriate, taking into account industry accomplishments, needs, problems and trends.

The SRC is responsible for extending the roadmap to specific research thrusts consistent with the needs defined in the roadmap. SRC science technical advisory boards annually define the key research thrusts in Volume III of the *SRC Management Plan*, Research Operations.

The SRC's Continuous Quality Improvement program will ensure that SRC research continues to achieve its ultimate aim: satisfying the more than 60 companies and organizations that make up the SRC and helping the North American semiconductor industry retain its global strength into the next century.

“One of the great results of this effort was the cooperation of 179 top scientists from different companies putting these roadmaps together. Given the competition and even confrontation that frequently characterize this industry, it is phenomenal we could all agree on a set of technology roadmaps for our industry and be eager to see them implemented.”

Owen P. Williams, Motorola Inc.



Robert M. Burger

“To meet the challenges and needs defined in the roadmap, the approach to semiconductor technology must be changed. All participants must share a single vision of needs and priorities.

The industry must improve its cooperation with government, strengthen its linkages – both upstream and downstream – and sustain its support for technology efforts extending from invention through commercial application.”

Robert M. Burger Vice President and Chief Scientist, SRC



Larry W. Sumney greets Sen. Jeff Bingaman (D-N.M.) who is holding a copy of the summary report of the national technology roadmap meeting.

Intellectual Property

*1993 Intellectual
Property
Achievements Enhance
Industry's Long-Term
Competitiveness*

The value added by the SRC to the industry's technology base includes the appropriate protection of intellectual property rights that result from SRC research.

In 1993, the SRC's research program resulted in a substantial increase in intellectual property activity. Sixteen patents were issued – a 35% increase over the total number of patents issued in the previous ten years. In 1993, SRC research also resulted in 22 patent applications. The SRC has a worldwide, unrestricted, royalty-free, non-exclusive license to these patents as well as the ability to license the patents to SRC participants.

The SRC's portfolio of patents was strengthened by 1993 intellectual property activity, particularly in the technology areas of contamination and defect control, aerosol processing and novel additions to advanced devices.

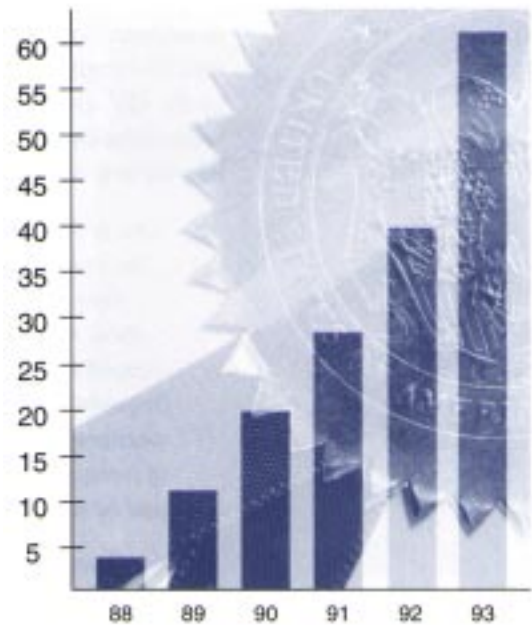
Contamination and Defect Control

Farhang Shadman of the University of Arizona was recognized by the SRC as a 1991 Technical Excellence Award winner for his research achievements. This research resulted in a 1993 patent that discloses a novel filter membrane comprised of a carbon-coated reactive layer of a reduced metal that reacts with and removes impurities from gases. The patent has been licensed by a major U.S. vendor that intends to manufacture a filter based on this technology.

Aerosol Processing

Peter McMurry and researchers at the University of Minnesota have developed and patented a technique for producing and controlling a very narrow aerosol beam via gas expansion and contraction, applicable to the manufacture of semiconductor wafers.

Total Number of SRC Patents



A 1993 patent granted to Robert Donovan and his Research Triangle Institute team discloses a method of uniform wafer coating achieved by sweeping an aerosol particle beam. This method applies photoresist without breaking vacuum, providing a distinct advantage in semiconductor wafer manufacturing.

Novel Additions to Advanced Devices

Technology developed and patented in 1993 by Mehmet Ozturk and researchers at North Carolina State University discloses doped Si-Ge alloy as a diffusion source for defining the source-drain regions and contacts of a field-effect transistor (FET). This eliminates the need for ion implantation.

Gerold Neudeck of Purdue University developed technology that describes a self-aligned, dual-gated silicon-on-insulator (SOI) FET. This patented technology eliminates the need for lithographic alignment steps.

1993 SRC Patents	Inventor Institution	Patent Number	Issue Date
Reactive Membrane for Filtration and Purification of Gases of Impurities	Farhang Shadman University of Arizona	5,196,380	3/23/93
Synthesis of Titanium Nitride Films	Emmanuel Giannelis et al. Cornell University	5,202,152	4/13/93
Ultraminiature Single-Crystal Sensor with Movable Member	Kensall D. Wise et al. University of Michigan	5,207,103	5/4/93
Method & Apparatus for Alignment and Overlay of Submicron Lithographic Features	Steven Brueck et al. University of New Mexico	5,216,257	6/1/93
Method & Apparatus for High Speed Digital Sampling of a Data Signal	Thomas A. Hughes, Jr. et al. North Carolina State University	5,229,668	7/20/93
Apparatus & Method for Uniformly Coating a Substrate in an Evacuatable Chamber	Robert P. Donovan Research Triangle Institute	5,229,171	7/20/93
Method & Means for Reducing Speckle in Coherent Laser Pulses	Willam N. Partlo et al. University of California at Berkeley	5,233,460	8/3/93
Alkaline-Free Electroless Deposition	Yosi Y. Shacham-Diamand et al. Cornell University	5,240,497	8/31/93
Selective Deposition of Doped Silicon-Germanium Alloy on Semiconductor Substrates	Mehmet Ozturk et al. North Carolina State University	5,242,847	9/7/93
Process for Preparing a Polyphenylene Polymer	Christopher K. Ober et al. Cornell University	5,248,734	9/28/93
Deposition of Germanium Thin Films on Silicon Dioxide Employing Interposed Polysilicon Layer	Mehmet Ozturk et al. North Carolina State University	5,250,452	10/5/93
Conical Rapid Thermal Processing Apparatus	Jimmie J. Wortman et al. North Carolina State University	5,253,342	10/12/93
Method & Apparatus for Reducing Fringe Interference in Laser Spectroscopy	Ed Whittaker et al. Stevens Institute of Technology	5,267,019	11/30/93
Apparatus & Method for Shaping & Detecting a Particle Beam	Peter H. McMurry et al. University of Minnesota	5,270,542	12/14/93
Apparatus & Method for Determining Power in Plasma Processing	John Thomas et al. New Jersey Institute of Technology	5,273,610	12/28/93
Methods for Fabricating a Dual-Gated Semiconductor-on-Insulator Field Effect Transistor	Gerold W. Neudeck et al. Purdue University	5,273,921	12/28/93

Technical Excellence Awards

*Recognizing
Outstanding
Research*

The SRC Technical Excellence Awards were established in 1992 to recognize outstanding research and create a bond between student and faculty researchers and the SRC's industrial participants. Awards are based on scientific merit, relevance to the technical objectives of the semiconductor industry, utility and technology transfer potential. In 1993, two research teams were selected as winners of the 1992 Technical Excellence Awards, which were presented in an awards dinner at the North Carolina Museum of Life & Science in Durham, N.C. in June.

The winners were:

IDDQ Testing and the Quality of IC Test

Science Area:

Design Sciences

Contributors:

Wojciech Maly and Thomas M. Storey (a former SRC graduate student, now employed at IBM), **Carnegie Mellon University**

Impact:

Detecting faults in complementary metal oxide semiconductor (CMOS) logic circuits through monitoring of static power supply current has significant advantages over traditional testing. Maly and Storey developed a technique for characterizing and sensitizing circuit faults and methods for measuring IDDQ to detect faults. Extensively used by industry for final testing of digital CMOS circuits, the technology has resulted in a significant improvement in product quality.

Chemometrics for the Analysis of Dielectric Films – Multivariate Analysis of FTIR Spectra for Boron and Phosphorous Concentration and Thickness of BPSG Films

Science Area:

Manufacturing Process Sciences

Contributors:

Thomas M. Niemczyk, **University of New Mexico**, David M. Haaland and David K. Melgaard, **Sandia National Laboratories**

Impact:

This technology's real-time capability of optical emission data allows *in situ* measurement and control of dielectric film thickness and composition – including boron and phosphorous content and borophosphosilicate glass (BPSG) film thickness – during planarization and interlevel deposition. Potential applications in industry include real-time monitoring of dielectric film properties during deposition.



SRC Chairman William Siegle (right) presents Technical Excellence Award to Thomas Niemczyk, University of New Mexico.

TECHCON'93

Interaction and Cooperation



Keynote Speaker James Burke addresses
TECHCON'93 audience.

More than 450 scientists and engineers from industry, university and government came to Atlanta in late September for TECHCON'93, the SRC's third national research conference.

“TECHCON presents a unique atmosphere for fostering technology transfer. It allows a panoramic view of the entire SRC research program, creating an unparalleled opportunity for interaction.”

*William T. Siegle, 1993 Chairman,
SRC Board of Directors
and Honorary Chairman, TECHCON'93*

TECHCON's plenary session, “Integration of Semiconductor Research: Formula for Success,” examined opportunities for cooperation in precompetitive research among universities, government and industry. Remarks on innovation and change by keynote speaker James Burke, a well-known author and British television commentator, had strong implications for the SRC.

“When you put things together that were never put together that way before, you cause one plus one to equal three – the outcome is more than the sum of its parts,” Burke said. The SRC research program, by bringing together disparate university research efforts into a comprehensive program, creates an outcome greater than each of the separate research efforts alone – SRC management of the research program makes the difference.

TECHCON's technical sessions featured presentations by SRC-funded faculty and graduate-student researchers, on topics ranging from TCAD process modeling, advanced devices and lithography, metrology and contamination control to plasma etch and deposition, packaging and multilevel interconnect. In all, 130 papers were presented.

TechFair, TECHCON's poster session, served as a showcase for SRC-funded research by displaying 118 student exhibits and presenting examples of technology transfer. Industry technology transfer successes were described by Advanced Micro Devices, Motorola, PDF Solutions, SILVACO, Sunrise Test Systems and Texas Instruments. University technology transfer presentations were given by Cornell, Purdue, Stanford and the University of Texas at Austin.

In post-conference evaluations, TECHCON'93 participants gave the conference high marks for the valuable information presented, and the opportunities for networking and interacting with fellow semiconductor scientists and engineers.



TechFair, TECHCON's poster session,
showcased SRC-funded university research.

SRC Industrial Mentor Program

*Bringing Industry
Perspective to the
University Research
Laboratory*



UC-Irvine Prof. Nikil Dutt, SRC 1993 Outstanding Industrial Mentor Award winner Robert Larsen, SRC fellow Nancy Holmes and Prof. Daniel Gajski (clockwise, from top right).

The SRC Industrial Mentor Program seeks to enhance the value of SRC research to industry and provide SRC-participating companies with early access to key technologies. The program included 526 participants from 38 companies and organizations in 1993. Scientists, engineers and managers who participated in the SRC Industrial Mentor Program are associated with specific, SRC-funded university research tasks. These industry technology experts provide perspective and insight into industry needs and access to corporate resources, helping accelerate the research and transfer results to their companies. Student and faculty researchers receive the benefit of direct contact with industry engineers.

When the program was started ten years ago, it included 42 mentors assisting university researchers with practical technical guidance and industrial resources. In 1993, there were more than ten times that many individual industrial mentors serving the SRC community. Some participating companies have more than 50 employees assigned to the mentoring program.

Each year, the SRC honors the significant contributions of all SRC mentors with the SRC Outstanding Industrial Mentor Award.

1993 winners, honored at TECHCON'93, were:

Robert P. Larsen of Rockwell International Corp., Newport Beach, CA, who has mentored SRC Design Sciences contracts at the University of California at Irvine and Case Western Reserve University since 1991.

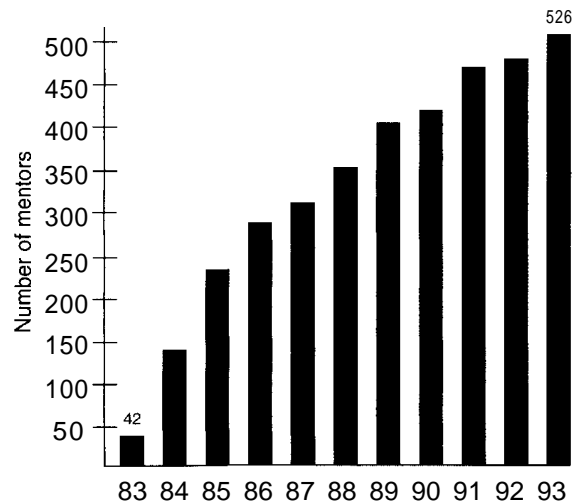
Thomas E. Zirkle of Motorola Inc., Phoenix, AZ, who, since 1990, has mentored an SRC Microstructure Sciences contract at Arizona State University.

Peng Fang of Advanced Micro Devices, Sunnyvale, CA, who has mentored a Manufacturing Process Sciences contract for the past three years at the University of California at Berkeley.

Herbert A. Lord of AT&T Bell Laboratories, Princeton, NJ, who has mentored a Manufacturing Systems Sciences contract since its inception in 1992 at the University of Colorado at Boulder.

Tien Y. Wu of IBM Corp., Endicott, NY, who has mentored a Packaging Sciences contract at The Ohio State University for the past four years.

SRC Mentor Program Involvement
1983 - 1993



SRC's Concurrent Technology Transfer System

1993 SRC Technical Advisory Board,
Technology Transfer

W. Dale Edwards
Hams Corp.
Chairman

Mahboob Khan
Advanced Micro Devices Inc.
Vice Chairman

Graham Alcott
Intel Corp.

William A. Butz
E-Systems Inc.

Jim Carroll
Motorola Inc.

Dao-Long Chen
NCR Corp.

William J. Flood
AT&T

Michael A. Fury
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Digital Equipment Corp.

John Pankratz
Texas Instruments Inc.

Robert I. Scace
NIST

James F. Skalski
Wright Laboratory

Court Skinner
National Semiconductor Corp.

Mark Stager
LSI Logic Corp.

Al F. Tasch, Jr.
University of Texas at Austin

Ken VanBree
Hewlett-Packard Co

Combining Total Quality Management with Technology Transfer

Quality is a benchmark by which companies are judged by their customers and judge themselves. In order to meet the needs of its customers and to emphasize its commitment to quality, the SRC has merged its technology transfer efforts with total quality management. The result is the SRC Concurrent Technology Transfer (CTT) System.

Over the past eleven years, the CTT System has evolved from the traditional serial process to a new system of parallel processes. The serial process transfers new technology from providers to recipients with similar technical backgrounds. Communications channels are point-to-point and cover a narrow subject focus.

The parallel processes of the CTT System transfer technology throughout development by using cross-functional teams. These teams, characterized by members from diverse backgrounds, consist of SRC personnel, principal investigators, graduate students, and operational and scientific industry representatives, including those involved in SRC's Industrial Mentor Program. The CTT System involves industry, academia and government at every stage of research and development, from planning through commercialization. It has helped facilitate unified research goals for key science areas critical to the semiconductor industry, which have been incorporated into the SIA roadmap. The result is a reduction in product-cycle time through the timely transfer of industry-relevant research results to SRC participants for commercialization.

Continuous Quality Improvement

Complementing the CTT System, the SRC implemented a Continuous Quality Improvement (CQI) program in 1992 with the goal of improving all of the SRC's internal processes and those of its "suppliers," North American universities.

Goals of the SRC's quality program are to increase customer satisfaction, reduce the SRC's contribution to research process-cycle time and maximize return on investment of SRC participants through effective technology transfer.

The SRC Member Quality Advisory Committee is composed of quality experts from SRC-participating companies: Motorola, Advanced Micro Devices, Harris Corporation, IBM and Texas Instruments. The committee reviews the SRC's quality implementation activities, helps the SRC maintain its focus on customer-defined goals, and recommends improvements and modifications that can leverage the achievements and services of the SRC.

The SRC Research Program

William C. Holton, Vice President, Research Operations

*More than \$28 Million
Invested in Research*

*New Center of
Excellence Established
at MIT*

The centerpiece of the SRC's efforts on behalf of its participating companies and organizations is its comprehensive research program. The SRC research program is goal-oriented – well-defined goals are employed in each science area with specific research thrusts to guide, focus and prioritize efforts and provide a basis for measuring progress. Research thrusts and goals for the next several decades, which were developed in the SRC Management Plan, have been incorporated into the SIA technology roadmap for the industry.

In 1993, 135 research contracts and grants were awarded by the SRC to 62 North American universities. The SRC invested \$28.3 million on these contracts and grants, distributed among five SRC science areas: Design Sciences, Manufacturing Process Sciences, Manufacturing Systems Sciences, Microstructure Sciences and Packaging Sciences. Research is subdivided into thrust areas within each science area.

Each science area's research director and technical advisory board conduct annual site reviews and technology transfer courses, evaluate proposals and provide technical guidance to researchers.

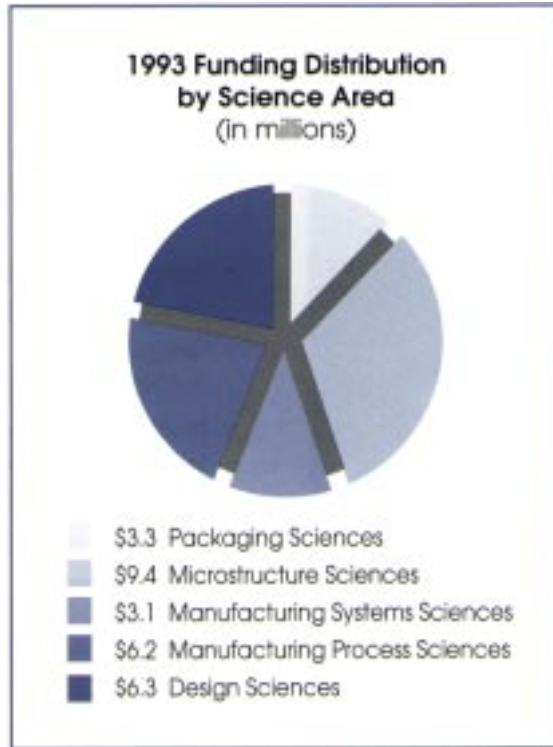
The SRC Research Program consists of four levels of activity: SRC Centers of Excellence, SRC Programs, SRC Projects, and SEMATECH University Funding.

The SRC Center of Excellence designation recognizes a sustained and distinguished record of significant contribution to the integrated circuits field by an institution over a number of years. There is a continuing commitment to each center of excellence from the SRC and annual funding exceeds one million dollars.

MIT Designated an SRC Center of Excellence

The SRC created its sixth SRC Center of Excellence at the Massachusetts Institute of Technology in 1993. Under the leadership of Dimitri A. Antoniadis, the newest Center will address technical challenges in microsystem technologies. Current SRC Centers of Excellence, which involve up to 75 graduate students and faculty, are:

- **SRC/Carnegie Mellon University** Center of Excellence in Computer-Aided Design
- **SRC/Cornell University** Center of Excellence in Silicon-Based Nanoelectronics
- **SRC/Massachusetts Institute of Technology** Center of Excellence in Microsystems Technologies
- **SRC/Stanford University** Center of Excellence in Computer-Integrated Manufacturing Sciences and Technology for VLSI
- **SRC/University of California at Berkeley** Center of Excellence in CAD/IC Design
- **SRC/University of Michigan** Center of Excellence for Automation in Semiconductor Manufacturing

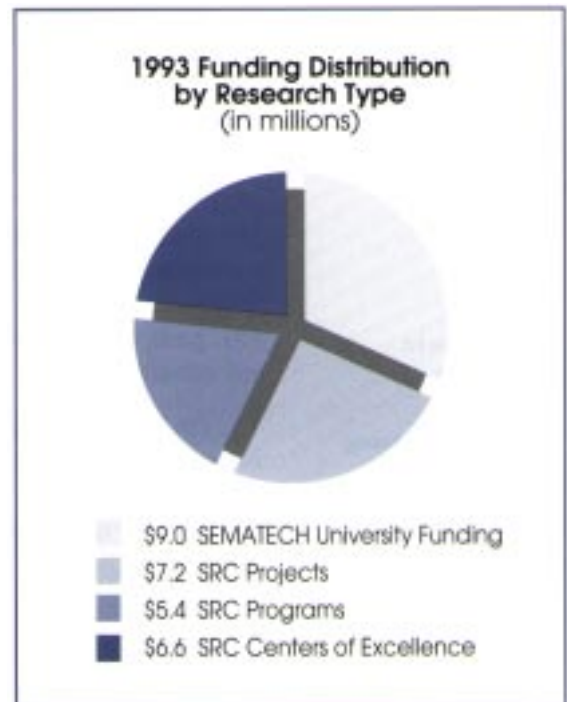


SRC Projects support the research of from one to six faculty and graduate students with annual funding of approximately \$100,000. Projects are more narrowly focused than SRC Programs and have three-year life expectancies.

With the introduction of the SIA technology roadmap, SEMATECH's mission was broadened to include activity in all roadmap areas. As a result, SEMATECH's research needs are shifting from just manufacturing to include needs in lithography, interconnects, environmental safety and health, design and other roadmap areas. The SRC is working with SEMATECH to restructure SEMATECH's university research program to make it responsive to the new mission.

SRC Programs, which are team efforts within universities with annual funding approaching one million dollars, generally support 15 to 40 researchers. SRC Programs now exist at:

- **University of Arizona** in Packaging
- **Clemson University** in Reliability
- **University of Florida** in Bipolar Devices
- **University of Illinois** at Urbana-Champaign in Reliable System Architectures
- **Lehigh University** in Packaging
- **North Carolina State University** in Process Technology
- **Purdue University** in Packaging
- **University of Texas** in Testable Systems
- **Stanford University** in System Level Packaging



Design Sciences

Peter Verhofstadt, Director

1993 SRC Technical Advisory Board,
Design Sciences

Tom Jones
National Semiconductor Corp.
Chairman

Kenneth L. Pocek
Intel Corp.
Vice Chairman

David Agnew
Bell Northern Research Inc.

David L. Blackburn
NIST

David Boisvert
Eastman Kodak Co.

Richard Byrne
The MITRE Corp.

Basant R. Chawla
AT&T

Bernie Chern
National Science Foundation

Raymond E. Cook
National Security Agency

William Terry Coston
Harris Corp.

Antun Domic
Digital Equipment Corp.

James Duley
Hewlett-Packard Co.

Ian Getreu
Analogy Inc.

Shawn M. Hailey
Meta-Software Inc.

John W. Hines
Wright Laboratory

Jim Kawakami
Advanced Micro Devices Inc.

John K. Kibarian
PDF Solutions

Boon-Khim Liew
BTA Technology Inc.

Dickie Lonnie
SEMATECH

Doug Parse
Motorola Inc.

Jeanne Pitz
Texas Instruments Inc.

Kenneth Sienski
E-Systems Inc.

Kevin M. Walsh
ANACAD Electrical Engineering
Software

Vincent Zagardo
Westinghouse Electric Corp.



University of Illinois at Urbana-Champaign graduate students John Chandy and Steve Parker stand with Prof. Prith Banerjee (at right) in front of UIUC's 512 processor CM-5.

With today's accelerated time-to-market needs, the semiconductor industry's challenge is to rapidly design integrated circuits and systems that achieve specified levels of performance, while ensuring that the resulting products can be manufactured with a high yield, tested to high levels of confidence and operated with high reliability.

To address this challenge, the SRC Design Sciences program funds research in areas which support the rapid, economic and testable design of very large-scale integration (VLSI) and ultra large-scale integration (ULSI) semiconductor products. Sponsored research also must support the overall SRC goals of high performance, quality, reliability and manufacturability.

The Design Sciences program addresses issues related to the design environment, design management and process, aspects of systems and analog circuit design, and concurrent engineering opportunities.

In 1993, emphasis was placed on low power design, as well as signal integrity design and interface standards for CAD tools. Design-related thrust areas include:

- **Design Environment** – platforms, frameworks, databases, methodologies, metrics
- **Design Synthesis** – logic, analog, block level and behavioral synthesis
- **Design Verification** – circuit, timing, logic and behavioral simulation, and formal methods
- **Test and Testability** – TPG, BIST, scan techniques, diagnosis
- **Physical Design** – placement and routing, analog layout, layout verification, design styles, partitioning and MCM
- **Design Techniques** – circuit design, modeling, DFM, DFR
- **System Level Design** – system modeling, system partitioning, task level synthesis, hardware/software co-design

The design sciences research program funded 30 research contracts or grants at 24 North American universities in 1993, with a total value of \$6.3 million. Forty-two design sciences students supported by the SRC graduated in 1993, and the majority went to work for SRC-participating companies and universities.

Design Sciences research highlights for 1993 include:

- **Carnegie Mellon University** – Edmund Clarke has successfully verified the cache coherence protocol (CCP) specified in the IEEE Futurebus+ standard using its Symbolic Model Verifier (SMV) formal verification technique. The Futurebus+ standard was developed to improve the performance of multi-processor computer systems. It has recently been adopted by the U.S. Navy as a standard for Navy applications. A number of errors and ambiguities were detected in the protocol, and the resulting concise, unambiguous model of the CCP will be useful to both Futurebus+ working group members and designers. This project demonstrates that formal specifications and model-checking techniques can be used to help design real industrial standards.
- **University of Illinois at Urbana-Champaign** – Prith Banerjee and his research team have developed a portable parallel algorithm for standard cell placement, called ProperPLACE. This is the latest in an integrated set of parallel VLSI CAD tools developed by UIUC researchers. The team had previously developed parallel algorithms for circuit extraction, test generation and logic synthesis. The ProperPLACE algorithm averaged a six-fold speed increase over the University of Washington's popular Timber-Wolf 6.0 placement program on a variety of parallel platforms, using eight processing elements. It will help provide rapid turnaround in the design process.

Technology Transfer Result

In an SRC-sponsored technology transfer experiment, students and faculty from the University of California at Irvine formed a team with engineers at Rockwell International to design a RISC processor chip with a design complexity of over two million transistors. Professor Daniel Gajski and his students have developed a comprehensive methodology for the design of complex digital circuits, called SpecSyn, which was used in the project. Students skilled in the use of high level synthesis worked with engineers experienced in a capture-and-simulate methodology. This unique collaboration not only educated each group in the other's methods, but also resulted in a working chip produced in record time. The SpecSyn system is being evaluated or used at Motorola, MITRE, Intel, Advanced Micro Devices, Texas Instruments and National Semiconductor.

Manufacturing Process Sciences

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The Manufacturing Process Science (MPS) research program focuses on robust processes and process tools that have the capability and flexibility to produce advanced integrated circuits. MPS explores the feasibility and manufacturability of innovative approaches to high-density ULSI circuits. Driving these innovations is the SIA roadmap, which specifies technologies that will make it possible to manufacture integrated circuits with feature sizes down to 100 nanometers.

MPS thrust areas are:

- **Lithography** – attempts to resolve and transfer patterned features reproducibly
- **Metrology** – provides nondestructive, *in situ*, real-time measurement at specified dimensions, concentrations, temperatures and pressures
- **Contamination Control** – seeks to minimize the deposition of contaminants on wafers during processing, allow the removal of contaminants, and determine which contaminants and at what levels cause electrically active defects during processing
- **Deposition** – develops processes that have low thermal budgets – due to the importance of temperature in the manufacture of device features – and equipment and processes that can deposit ultrathin films with required properties
- **Plasma Etch** – attempts to improve the capability to etch anisotropically, at high rates, with uniformity and without damage
- **Reliability** – seeks to understand the behavior of ultrathin films under stress, measure circuit parameters that affect reliability, and develop models for circuit reliability that can be integrated into the design process.



Penn State graduate students Kevin Torek (left) and David Hwang set up an SMS dry cleaning tool for experiments.

The MPS research program funded 21 research contracts or grants at 17 North American universities in 1993, with a total value of \$6.2 million. Twenty-seven of the 144 manufacturing process sciences students supported by the SRC graduated in 1993, with the vast majority of these taking jobs with SRC-participating companies and universities.

MPS research highlights for 1993 include:

Pennsylvania State University – Jerzy Ruzyllo and his team have developed a gas-phase dry cleaning technology for removing trace contaminants from silicon surfaces. This will improve yields and reduce both production costs and negative environmental impact.

Princeton University – Joe Cecchi has developed plasma diagnostic tools to be used on low-pressure, high-density etch tools for *in situ* monitoring of the plasma and plasma/wafer interface. Better diagnostic tools will allow more efficient use of materials and produce less waste.

Lithography Made New Science Area

To more closely align the SRC's science area structure with the SIA roadmap, the SRC Board agreed in 1993 to create a sixth SRC science area in Lithography. Research focuses on submicron optical lithography as a low-cost extension of current mainstream tools to the 0.25 micron regime. New resists, deep-ultraviolet optics and phase-shift masks provide significant research challenges at this feature size. X-ray lithography is also being investigated as a second system for meeting this pattern transfer need. Lithography research thrusts are: masks, pattern transfer, resists, alignment and overlay, systems and metrology.

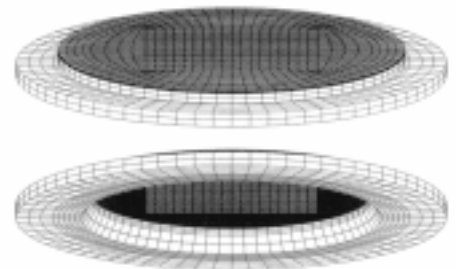
MPS research highlights for 1993 in the Lithography thrust area include:

- **University of California at Berkeley** – A.R. Neureuther and his research team have developed Mask Analysis by Computer (MASC), a computer-aided design tool. MASC generates design graphs of user-specified image quality measurements over one- and two-dimensional mask areas as a function of both optical system and mask layout parameters.
- **Cornell University** – Jean Fréchet and researchers at Cornell have developed new photo-imageable formulations with high resolution and sensitivity, suitable for a variety of radiation methods. Preliminary studies of these formulations revealed several desirable features, including: aqueous-base solubility; tunable sensitivity; good plasma etch resistance; and imageability with various radiation sources, including X-ray, deep-ultraviolet and electron-beam.

Technology Transfer Results

Roxann Engelstad and her research team at the University of Wisconsin at Madison have developed a software model for computing the 3-D stresses and distortions in X-ray mask membranes. Their efforts provide a fundamental understanding of sources of stress and a methodology for reducing mask-related errors in X-ray lithography. Working with IBM and the National Institute of Standards and Technology, Prof. Engelstad and the software her team developed have played a pivotal role in the creation of an X-ray mask standard,

Gordon Kino and metrology researchers at Stanford University have used a solid immersion lens system with a refractive index of 1.46, identical to that of the quartz mask material, to measure I-line phase-shift masks produced by IBM and AT&T. This technique allows, for the first time, width and height measurements of the mask structure from the back side of the mask.



Finite element model (top and bottom view) of the ARPA-NIST National X-ray Mask Standard – developed in part through SK-sponsored research at the University of Wisconsin at Madison – showing the 50mm x 50mm pattern area.

Manufacturing Systems Sciences

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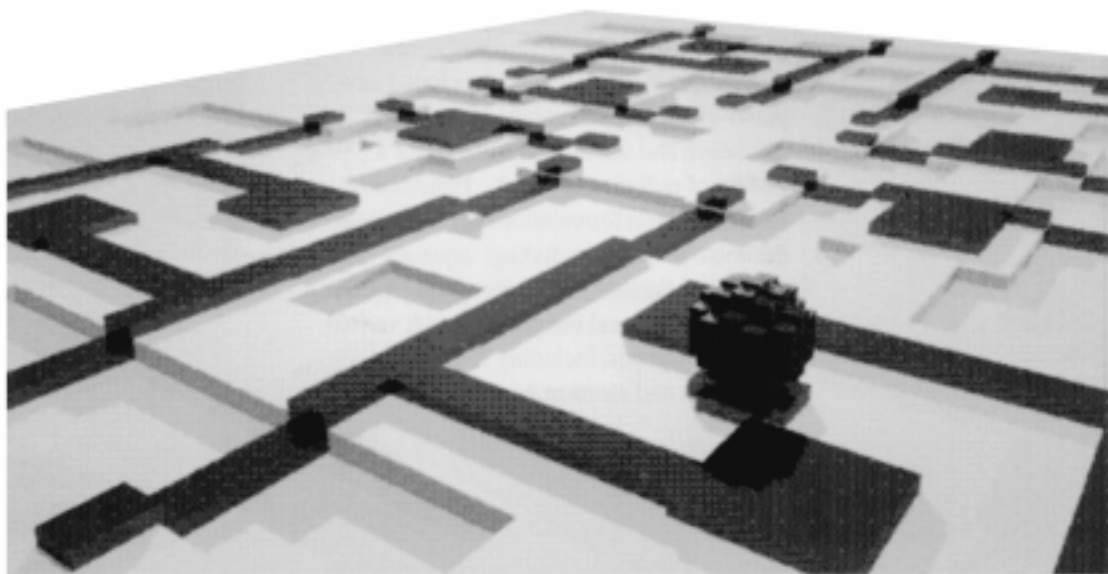
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The goal of the Manufacturing Systems Sciences (MSS) program is to provide software tools and methodologies that allow efficient and effective application of computer technology to rapid design transfer and manufacture of low-cost, high-performance integrated circuits and systems. MSS thrust areas are:

- **Equipment Automation and Process Control** – focuses on the overall wafer fabrication process and the equipment used in it. This thrust area is subdivided into three subthrusts: equipment and process modeling, sensor systems for control, and system integration and architecture.
- **Factory Automation and Management** – focuses on monitoring and controlling the overall IC factory operation in order to minimize manufacturing costs through effective equipment utilization and optimum processing times. This thrust area is subdivided into three subthrusts: data management control, factory models and wafer handling.
- **Rapid Learning** – seeks to provide rapid and accurate analytical and predictive software tools and methodologies to support IC manufacturing. The analytical tools are designed to support interpretation of experimental data and to identify causal relationships, such as those between product yield and process conditions. The predictive tools use these relationships to predict performances and yields of future products.



A 3-D representation of IC topography from Carnegie Mellon University, showing a 1 μ m dust particle which has landed on an SRAM cell after polysilicon deposition.

Each MSS thrust is the result of early SRC identification of the potential for application of advanced statistical methodologies to manufacturing tool control and to computerized factory control systems.

MSS managed eight research programs at nine North American universities in 1993, with a total value of \$3.1 million. Nine MSS students supported by the SRC graduated in 1993, and five have taken jobs with SRC-participating companies and universities.

MSS research highlights for 1993 include:

- **University of California at Berkeley** – Robert C. Leachman has defined an optimal wafer release and scheduling strategy for fabs using dynamic programming. He developed a new release control rule, called descending control (DEC). This rule outperforms currently employed release rules, such as CONWIP, starvation avoidance and workload regulation. The DEC rule can be applied readily to multi-product networks and produce-to-order systems.
- **Carnegie Mellon University** – Researchers at Carnegie Mellon have been involved in developing software tools for yield simulation for the past 15 years. The newest yield simulation system, called Defect to Fault Mapper (DEFAM), estimates yield given the IC mask artwork, process flow and process disturbances. DEFAM employs the PREDITOR TCAD framework to perform statistical process simulation. Then it uses a Monte Carlo method to convert local process disturbances (defects) to changes in circuit topology and performance. DEFAM exploits the design hierarchy by using the Hierarchical Chip Database to achieve a significant reduction in simulation time. This system has been tested on ICs with up to 650,000 transistors.

Technology Transfer Result

Researchers at the University of Michigan have designed a multi-thread, ready-to-run control framework for the sequential control of very large-scale integration (VLSI) processes. This design verification framework, Michigan Sequential Control and Optimization Environment (M-SCOPE), features a Generic Cell Controller (GCC) core control mechanism and is compatible with SEMATECH directions in sequential cell control. The design resulted from a detailed analysis of SEMATECH directions in run-to-run control and a technology transfer feasibility study funded by Advanced Micro Devices.

Microstructure Sciences

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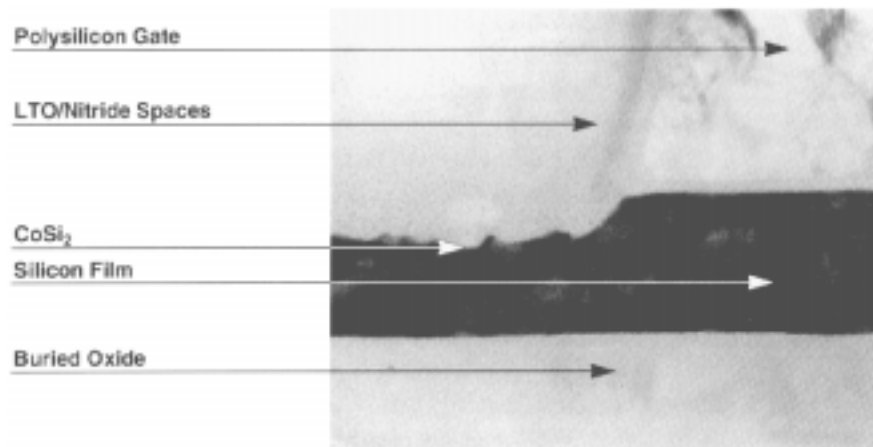
Robert M. Werner
Wright Laboratory

The driving force behind the SRC's Microstructure Sciences research program is to understand the fundamental physics and chemistry for semiconductor processes and structures. Microstructure Sciences seeks to model these processes and to search for new materials, structures, processes and concepts for integrated circuits.

Microstructure Sciences aims to: shift the focus of device technology from the standard shrink technology approach by introducing creative structures and process architectures; provide improved predictive modeling; conceive circuit elements that are yield-tolerant of manufacturing defects; and recognize opportunities for paradigm shifts that redirect engineering efforts to circumvent current technology limitations.

The major thrust areas of the Microstructure Sciences research area are:

- **Advanced Technology** – gate dielectrics and field oxides, SiGe technology, epitaxial growth, novel processes, novel materials, and characterization and analytical techniques
- **Advanced Devices** – novel structures, 3-D/SOI/TFT devices, SiGe structures, sensors and transducers, power devices and Si bulk devices
- **Technology CAD** – device processing, device performance, unit processes, advanced modeling and user environment
- **Multilevel Connect** – process modules, materials, reliability and interconnect paradigms



Extremely thin (20nm), highly textured CoSi_2 formed by a novel Ti/Co bilayer reaction with Si at the MIT Center of Excellence.

Microstructure Sciences draws its strength from university programs that span the electrical engineering, computer science, chemistry, physics and materials science departments. Diagnostic and computer science facilities exist at many universities, and several operate IC fabrication labs with etching, deposition and lithography equipment suitable for deep-submicron structure development. The combination of creativity, analysis and predictive modeling – driven by industry goals but not directly connected to product applications – permits a flexibility not available in industry. Industry interaction through programs like the SRC Mentor Program ensures that the research effort is industry-relevant and results are transferred quickly to industry.

The Microstructure Sciences research program funded 47 research contracts at 22 North American universities in 1993, with a total value of \$9.4 million. Thirty-one microstructure sciences students supported by the SRC graduated in 1993, with most taking jobs at SRC-participating companies and universities.

SRC Microstructure Sciences research highlights for 1993 include:

- **Massachusetts Institute of Technology** – Dimitri A. Antoniadis and graduate student Lisa Su have delineated the fully depleted (FD) design space for 0.1 micron silicon on insulator (SOI). Drain Induced Barrier Lowering (DIBL) is more significant in SOI than in bulk devices and film thickness must be thinner than junction depth in bulk.
- **University of Illinois at Urbana-Champaign** – Joe Greene has produced “controlled” microstructures for investigating diffusion barrier failure mechanisms. This research has led to an explanation of the interfacial degradation of titanium nitride (TiN) and the development of dramatically improved $Ti_{1-x}Al_xN$ barriers. The University of Illinois has recently extended its study of diffusion barrier reactions to include tungsten (W), tungsten titanium ($W_{1-x}Ti_x$) and $W_{1-x}Ti_xN$ alloys. The first epitaxial, single-phase, metastable, $W_{1-x}Ti_x/Al$ and $W_{1-x}Ti_xN/Al$ bilayer structures have been grown.

Technology Transfer Result

A University of Florida research team has developed a new SPICE2G6 model for vertical integrated-gate bipolar transistors (ViGBT). ViGBT is one of four widely used power devices being modeled and integrated into circuit simulators under SRC contract at the University of Florida. The models enable predictive TCAD and accurate simulation of circuits containing power integrated circuits, such as power supplies and telecommunications and automotive electronics. The SPICE2G6 model has been evaluated by the National Institute of Standards and Technology and currently is under review by six SRC-participating companies.

Packaging Sciences

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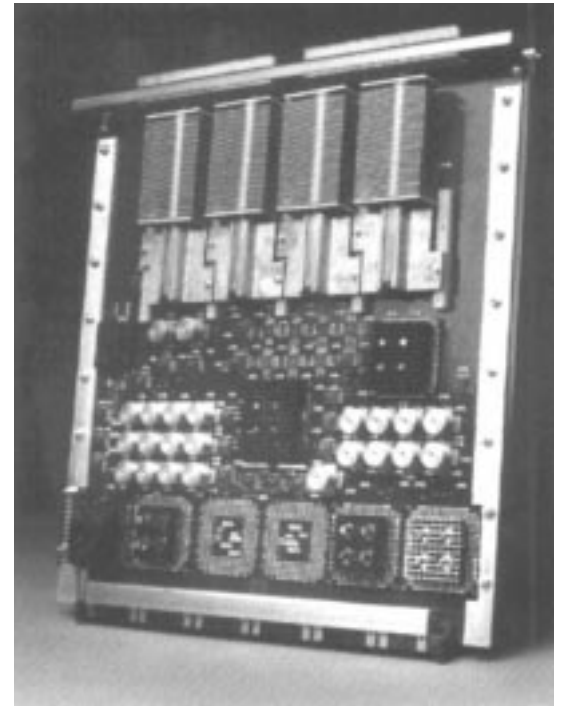
Dianna Wright
Arizona Packaging Software Inc.

The electrical, thermal and mechanical characteristics of the integrated circuit (IC) package are critical elements in the overall performance of commercial systems. The contributions of the package to the system characteristics therefore must be accurately predicted and taken into account in the system design phase. Highly sophisticated software tools have been developed for integrated circuit design and simulation; similar tools are needed for the package. The eventual goal is to integrate the circuit and package design systems to provide a single system analysis, design and simulation environment, including package manufacturability restraints.

The increasing speed and density of integrated circuits is putting ever more stringent requirements on the package to remove heat generated by the IC while maintaining operating temperatures consistent with high reliability. The SRC Packaging Sciences research program focuses on providing the information, tools and methodologies for the design and fabrication of packaging structures in order to satisfy the electrical, thermal/mechanical and reliability requirements of future systems.

The major thrust areas of the Packaging Sciences research area are:

- **Analysis, Design and Simulation** – builds and verifies models of packaging structures and integrates these models into a user-friendly design environment
- **Heat, Signal and Power Distribution** – seeks materials with high thermal conductivity and closely matched expansion coefficients
- **Materials and Measurements** – investigates composite materials and mechanical and chemical stresses
- **Package Reliability** – researches the basic physics and chemistry of mechanical and chemical stresses on materials, particularly interconnection interfaces



Heat pipes developed by SRC affiliate member DTX/Thermacore.

The Packaging Sciences research program funded 16 research contracts at 13 North American universities in 1993, with a total value of \$3.3 million. Six packaging sciences students supported by the SRC graduated in 1993.

SRC Packaging Sciences research highlights for 1993 include:

- **Cornell University** -J. Peter Krusius has implemented a thermal network model for cooling in AUDiT (Automated Design Tradeoff simulator for packaging architectures). This permits building of a global thermal resistance network for the entire packaging architecture in a simple SPICE-like format, introduction of computed chip fluxes into the appropriate network nodes, and transformation of mixed temperature/flux boundary conditions into uniform flux inputs with the node temperatures as unknowns.
- **Purdue University** – Purdue’s Center for Information and Numerical Data Analysis and Synthesis (CINDAS) has contributed to the expansion of the Microelectronics Packaging Materials Database by measuring mechanical properties of gold bonding and bump wires, leadframe materials, and lead-free and lead-rich solder alloys. Researchers at CINDAS also have compiled and evaluated data on packaging materials including new ceramics, silicon nitride, diamond, solders, and polymers such as polyimides, PTFE and Kevlar. All data are incorporated into a PC-operational Packaging Materials Database, available on diskette.

Technology Transfer Results

Data General Corporation has chosen heat pipes developed by SRC affiliate member DTX/Thermacore to cool the four central processing units (CPUs) in its Eclipse MV/60000 high-performance, fault-tolerant superminicomputer. The heat pipe packaging technology, which provides exceptional performance for cooling semiconductor devices, is based on SRC-funded research by C. Thomas Avedisian, Kenneth Torrance and scientists at Cornell University.

The Thermacore heat pipes are of a copper-water/sintered-wick design and operate in any orientation. The pipes, which have extremely high thermal conductivity, transfer heat laterally across the circuit board to an area where sufficient space is available for adequate fin size and airflow.

As reported in *Electronic Packaging & Production*, in Data General’s case, conventional aluminum finned heat sinks could not provide the required heat dissipation at the device to maintain the allowable junction temperature. This was due to height restrictions that limited heat sink size.

In this application, the thermal performance of the Thermacore heat pipes is double that of conventional heat sinks, thus achieving only one-half the temperature rise.

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