

The Semiconductor Research Corporation

15 Years of Innovation

SRC Annual Report 1997

Members

Advanced Micro Devices, Inc.
Digital Equipment Corporation
Eastman Kodak Company
Harris Corporation
Hewlett-Packard Company
IBM Corporation
Intel Corporation
LSI Logic Corporation
Lucent Technologies
Motorola Incorporated
National Semiconductor Corporation
Northrop Grumman Corporation
Texas Instruments Incorporated

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SILVACO Data Systems
Tessera, Inc.
Verity Instruments

Participating Government Agencies

National Institute of Standards and
Technology
National Science Foundation
U.S. Army Research Office

Strategic Industry Partners

SEMATECH
Semiconductor Industry Association

*15 years
of innovation*

Vision

The Semiconductor Research Corporation (SRC) will provide competitive advantage to its members as the world's premier research management consortium in delivering relevant research results and relevantly educated technical talent.

Mission

The SRC's mission is to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the NTRS, focusing on universities
- Relevantly educated university graduates
- Timely transfer of research results
- Strengthened university semiconductor technology capability through partnerships with members
- Collaboration to enhance commercialization and leveraged research

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The annual report of the Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC research program, present the formal financial report and provide information on activities and events of the SRC community for the previous calendar year. The SRC's vision and mission were revised in February, 1998, and are shown above.

A copy of this report and additional information about the SRC are accessible on the World Wide Web at <http://www.src.org>.

Message from the President & CEO



Larry W. Sumney

A Look Back

In December, 1981, Dr. Robert Noyce, then Chairman of the Semiconductor Industry Association (SIA) announced the establishment of the SRC for the purpose of stimulating joint research in advanced semiconductor technology by industry and U.S. universities. He noted that “leadership in semiconductor research will determine market performance in the future.” Dr. Noyce was a believer that investments in research and education would drive future economic growth and he was willing to lead the youthful SIA membership forward in an experiment to prove the thesis. He shared his prescience at that moment. We are fortunate to have his vision and leadership as elements of our legacy.

1997 Accomplishments

The Microelectronics Advanced Research Corporation (MARCO) traces its origins to 1994 when SRC analysis revealed a disparity between actual research being funded and the type of research that the National Technology Roadmap for Semiconductors (NTRS) technology requirements demanded. This ‘research gap’ led the SIA and SRC to form MARCO, a research organization with an emphasis on the elimination of current technological barriers by seeking more revolutionary approaches. MARCO-supported researchers are expected to seek creative options for the solution of key technology challenges so that the industry can keep pace with the cadence of Moore’s Law. MARCO, an SRC subsidiary, will invest in research universities to carry out its mission.

The SRC’s continuing commitment to providing a clear view of the industry’s technology needs was demonstrated by partnering with the SIA and SEMATECH to update the third edition of the NTRS, which was published in November. We strengthened our partnership in 1997 by identifying and launching new opportunities for long-term university research programs responsive to strategic industry needs. We also identified projects in the SRC portfolio that would benefit from transitioning to SEMATECH’s programs for hardening early technology outcomes.

A Look Ahead

The structure we have created to invest in research, manage it in a coordinated manner and deliver the results to our members will serve the SRC into the foreseeable future. We have a clear sense of the expectations our members have for us. It is our responsibility to create value for them by providing advanced enabling technologies and a relevantly educated scientific work force. We have provided our members with a very effective delivery system, our online Research Catalog, and will continue to optimize it. The strength of the university research infrastructure and its continued contributions to the vitality of the semiconductor industry along with the core competencies of the SRC and MARCO remain a viable strategic option for our industry.

I am pleased to report to you that experience has proven Dr. Noyce’s thesis and the lesson has taken root. The SRC has and continues to provide dividends for its members. In passing our fifteen year milestone, we are at once evolving and rooted in the industry’s landscape. We appreciate the support and counsel from many, many supporters. Thank you.

Sincerely,

Larry W. Sumney
President & CEO

About the SRC

SRC is a consortium of North American companies and participating government agencies engaged in planning and managing long term, pre-competitive university research for the semiconductor industry. The two products of the consortium are **research results** (knowledge) and **talented people** (students). Obviously, these are intimately coupled. In order to carry out the highest quality of research, the best and the brightest talent is required, complemented by a program of critical, challenging and meaningful research. The SRC directs an integrated program of applied research, conducted by the faculty and graduate students at dozens of leading universities and research institutions across United States and Canada. This program is funded by the member organizations that view participation as critical components of their long-term success. The SRC program is the result of the vision, commitment and dedicated stewardship of many thousands of individuals and has proven to be an excellent and enduring model for cooperative research.

Four key principles of research management are practiced by SRC: **1)** we know our customers' research needs, **2)** we invest in and manage only excellent research, **3)** we actively transfer research results to our members, and **4)** we recognize that it is in our interest to strengthen the university research infrastructure. We strive to anticipate our customers' research and human resource needs and to accelerate the R&D elements of their product life cycles.



SRC's Value

Since the founding of the SRC in 1982, the SRC staff and the member companies of the consortium have worked together to maximize the value



the members receive from the consortium. The key elements of this value are:

- High quality university **research** to meet the critical, long-term technological needs of the silicon

integrated circuit industry, performed by hundreds of faculty members and students.

- **Graduate students** educated in and knowledgeable of the technological areas important for current and future success of the industry.

- The combination of the proceeding two, in turn, has created a strong **university infrastructure** which not only nurtures and strengthens the advances in the curriculum for the development of talented people for the future needs, but also provides a pool of consulting resources for solving the industry's day-to-day technical challenges.

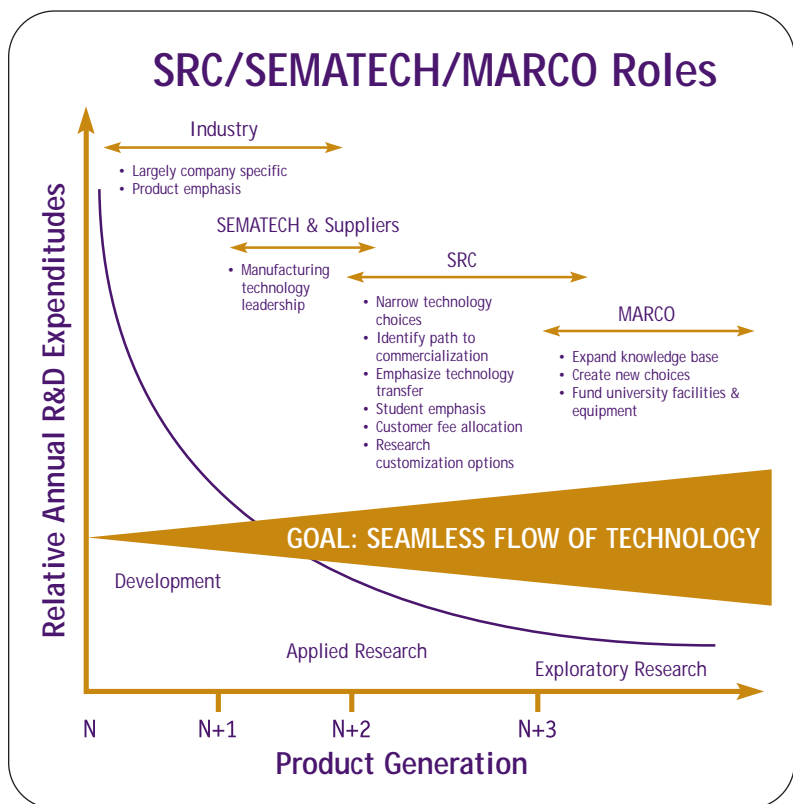
- The natural, formal and informal **networking** that results from interactions in a variety of forums allows the industry to shape the course of the technology and affords opportunities for benchmarking in a number of functional areas.

About the SRC

Since the NTRS was first published in 1992, both the SRC and SEMATECH have aligned their organizations and programs to address the R&D needs articulated by the industry through the NTRS. The SRC and its role, relative to MARCO and SEMATECH, is represented below.

In collaboration with a variety of advisory board structures, SRC focuses on creation, delivery and extraction, evaluation, and enhancement of the value in all these areas. In 1997, the Executive Technical Advisory Board (ETAB), consisting of representatives from the member companies, established a committee to address measurement and enhancement of SRC value. A consensus view of measuring the SRC value has been developed. This measurement deals with both the quantitative and qualitative benefits the member companies receive from the consortium. The first part quantifies net value in terms of measurable benefits minus costs. The benefits address areas such as leverage (cost avoidance) in R&D costs, value of students hired by member companies and other measurable benefits. Costs elements relate to the resources required to participate and extract the benefits. In addition to these, and, perhaps even more valuable, the second part addresses the qualitative benefits which are characterized as “priceless.” These include the

unquantifiable, long-term benefits accrued through the contributions made by the students as valuable resources to the member companies who hire them, as well as the specific research results which the member companies are able to use and which make sizable contribution to their business success. More than the simple leverage and cost avoidance, these benefits are the basis of the “compelling reasons” for the member companies to participate in the SRC.



This figure illustrates the present day commitment of R&D expenditures to ensure future generations of semiconductor devices. The largest investments are made by individual companies as they prepare for their next generation of products. Additionally, significant resources are committed on a cooperative basis to meet the difficult challenges presented by future products two generations and more from present day practice. Each product generation represents increasing risk.

Research Contributions

The SRC's research community yielded critical contributions to member companies in 1997. A distinguishing feature of these advanced, enabling technologies is that they are provided through the voice of the customer. The E-TAB Advocacy and Value Committee compiled this subset of SRC-sponsored research contributions and share them by science area. The SRC also launched a new research initiative in operational methods in semiconductor manufacturing, described in the Factory Sciences section below.

Design Sciences

The SRC provides benefits to members directly when external research results connect with their own in-house capabilities, and indirectly when they use commercial products having roots in SRC efforts. An example of receiving direct benefit is the formal verification tool, Verdict, developed by Motorola and used on commercial designs. Formal verification is playing an increasingly important role in assuring that electronic design implementations function correctly, and SRC members and SRC-supported faculty and students are in the forefront of this work. Two SRC-supported students, one each from the University of California at Berkeley and the University of Colorado, worked with Motorola researchers and uncovered two functional errors in an automotive safety feature control chip. This work was later reported as a case study at the 1997 Design Automation Conference. The Verdict tool, used extensively by Motorola incorporates elements of SRC-sponsored research at Carnegie Mellon University, The University of Colorado and the University of California at Berkeley. This experience illustrates that:

1. Pre-competitive research results from the university community form a key part of the base on which SRC members build their tools and designs.
2. The work of several participating universities can be integrated and incorporated for successful applications.
3. Students play a key role in transfer of university results for application to member needs.
4. The university researchers in a particular area are strengthened by becoming a collaborative community under SRC auspices.

Members also utilize products from EDA vendors which in turn have their roots in SRC-sponsored research, the indirect benefit SRC provides to its members mentioned earlier. These 'productized' tools enable a wider range of SRC members to take advantage of Design Sciences research results. For example, Lucent Technologies' FormalCheck® verification tool benefits from SRC-sponsored research at the University of Colorado at Boulder and Carnegie Mellon University.

Factory Sciences

The cost per function for semiconductor devices has historically followed a 30% per year cost improvement. This pattern is fueled by four key contributors: reduced feature size, increased wafer size, improved yield and increased equipment and factory productivity. The direction for reducing minimum feature size is set for the next decade, and is described in the NTRS. The projected contribution in cost improvement from reducing feature size remains fairly constant. Unfortunately, the same is not so for contributions from yield improvement and wafer size increase. Wafer yields have improved dramatically over the past decade due, in part, to successful research efforts, reducing the remaining potential for contributions from improved yield. The cost return on increased wafer size is also projected to diminish. Therefore, the productivity and efficiency of the factory and the utilization of processing equipment are critical if the historic cost trend is to be maintained.

In 1997, the SRC and the National Science Foundation (NSF) launched a research initiative directed at the development of innovative new operational methods that will enable factory performance to keep pace with ongoing improvements in equipment and processes. The major theme of this initia-

Research Contributions

tive is the development of modeling, analysis, and optimization techniques based on fundamental principles leading to factory-level models that allow for effective control of semiconductor manufacturing operations. While the individual process and equipment performance are important elements of this initiative, the focus is on the system (or factory) level. The development of this capability will have a profound impact on the performance of current and future fabrication facilities.

Interconnect Sciences

Cu Metallization and Low K Dielectrics at Rensselaer Polytechnic Institute. Professor Shyham Murarka and his research team in the Center for Advanced Interconnect Science and Technology, (CAIST), led by RPI, have been developing novel processes and materials to address the fundamental issue of the lag of the on-chip interconnect performance with respect to device performance. These researchers have provided seminal information on the physics and technology of Cu processes (including deposition and CMP) and their integration with various low dielectric constant (K) insulators. Member companies, along

with SEMATECH, have drawn from the output of this research to develop process modules using Cu metallization and/or low K dielectrics for their future interconnect process technologies.

Lithography Sciences

Advanced Mask Research at the University of Wisconsin-Madison. Mask modeling research led by Professor Roxanne Engelstad has become an integral tool for the development of the NIST X-ray mask standard and process used by Motorola. In 1997, this research expanded its scope to explore the performance, potential and limitations of all five mask technology options identified as potential solutions in the 1997 edition of the NTRS. SEMATECH is augmenting SRC's program by awarding approximately \$1.5 million to support and accelerate this work to facilitate next generation lithography development and prototype decisions.

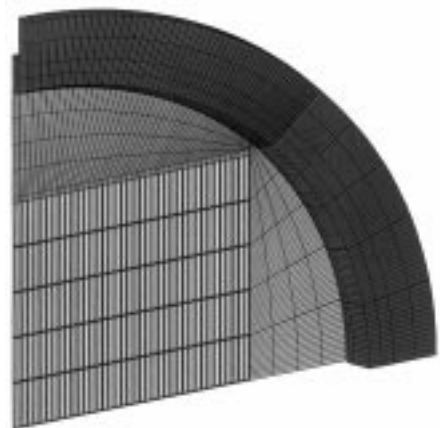


Photo and model provided by: Lucent Technologies

Collaborative efforts are underway between the UW-Computational Mechanics Lab and Lucent Technologies to use finite elements (FE) simulations to analyze and optimize the design of the SCALPEL mask. A photo of a mask blank is shown with the corresponding FE model (quarter symmetry). The 3D model is used to predict IPD and OPD during specified fabrication procedures.

Materials & Bulk Process Sciences

0.1 μm CMOS Device Design at North Carolina State University (NCSU). Researchers at NCSU have been concentrating their efforts on single-wafer manufacturing for submicron technologies. They have developed a comprehensive program on low-thermal budget, in-situ, single-wafer processing with facilities that include plasma processing, rapid thermal processing and cluster tools for stacked-gate structures and raised source-drain configurations. In the arena of gate dielectric scaling, fundamental studies have been conducted on various gate insulators for scaled MOSFETs led by Professor Carlton Osburn. The NCSU researchers have completed the design and optimization of 0.1 μm CMOS devices using conventional and alternate gate stack dielectrics also developed at NCSU. Dielectrics explored were furnace thermal oxide (used as a reference), rapid thermal oxide (RT oxide), rapid thermal chemical vapor deposited oxide (RTCVD oxide) and remote plasma enhanced chemical vapor deposited oxide (RPECVD). A design manual is available that shows the results of a statistical device design methodology and response surface analysis that optimizes the key process parameters. A key accomplishment was the identification of conditions for each gate dielectric, that yielded the best performance as given by the saturation drive current and met the 1997 NTRS off-state current specification. This work will serve as a guide for SRC members as they implement device designs for the 0.1 μm technology node and beyond.

Packaging Sciences

Microminiature Thermal Management Research at Stanford University. The NTRS projects that heat generated by most classes of devices will increase substantially between 1998 and 2012. The rate for handheld products will increase from 1.2 to 3.2 W on a per chip basis and the rate for the cost performance segment will increase from 28 to 109 W per chip. To prevent a dramatic increase in the temperatures and associated failure rates of these systems, packaging development must proceed aggressively to identify and alleviate sources of thermal resistance. Research at Stanford University led by Professor Ken Goodson contributes to this effort by developing unique tools for mapping temperature, strain, and thermal resistance distributions in packaging, and by measuring packaging materials properties needed for

simulations. The core capability is high resolution (1ns/50nm) optical thermometry, which was originally developed to map hot spots in interconnects during ESD stressing. Near field optical thermometry (NFOT) using a scanning fiber extended the spatial distribution of die-attach thermal resistance and captures cross-sectional strain and temperatures distribution in flip-chip structures. Thermal property measurements yielded data for metal-filled epoxy die attachments and for the anisotropic thermal conductivity's of novel polymer on-chip passivation. This research is conducted in close collaboration with mentors at Texas Instruments and Intel, where it is aiding in the simulation and design of reliable packaging structures.

Process Integration & Device Sciences

BSIM3 at the University of California at Berkeley. A research team led by Professor Chenming Hu is exploring the extension of the Berkeley Short-channel IGFET Model (BSIM3) to support the circuit requirements down to the 0.1 μm technology node. BSIM3 is different from earlier versions in that it is physically based, scalable and ready for digital or analog applications. Over 60 copies of the BSIM3 codes and documentation have been shipped to or requested from SRC members. All major commercial SPICE vendors have already released or plan to release BSIM3. In its current formulation, BSIM3 has been designed and verified for devices with effective dimensions of 0.25 microns or above. The formulation of BSIM3 is based on a coherent quasi-2D analysis of device structures, taking into account the effects of device geometry and process parameters. As such, scalability is inherently built-in. Currently, there are several challenges in the process of extending the model from 0.25 μm to 0.1 μm. Some phenomena that we consider insignificant may become important, and this research will collect experimental results on silicon devices to validate the scaled model. The results of this research will continue to be very significant for SRC members.

Technical Excellence Award

Rewarding Outstanding Research Accomplishments

The SRC Technical Excellence Award was established by the SRC in 1991 as an incentive and recognition program for research of exceptional value to SRC members. The awards are presented annually for research that significantly enhances the productivity and competitiveness of the North American semiconductor industry. Award criteria include creativity and innovation; relevance to the research objectives of the SRC and the semiconductor industry (as reflected by the NTRS); value or impact on industry in relation to internal roadmaps; cost reduction; and technology transfer success. This year's recipients bring the number of researchers who have been recognized with the Technical Excellence Award to 45.

In 1997, thirteen Technical Excellence Award nominations were accepted, most of them from industry, indicating the extent to which results from SRC-funded programs are utilized by the industry. One was selected to receive the 1996 Technical Excellence Award and was recognized at an awards banquet and poster session held in conjunction with the SRC's June Board of Directors meeting and operations review in Research Triangle Park, NC.

Mr. David Medeiros, Mr. Kyle Patterson, Mr. Uzodinma Okoroanyanwu, Dr. Tsutomu Shimokawa and Professor Grant Wilson, pictured below with SRC Chairman Donald Wollesen (L to R) received the Technical Excellence Award for their outstanding research at the University of Texas on "Advanced Resists." This research involved the investigation of new chemical platforms for the design of high performance 193-nm photoresists. What makes the



SRC Chairman Donald Wollesen, third from right, is pictured with the Technical Excellence Award winners from the University of Texas at Austin.

researchers' contributions especially noteworthy are the radical departure from "conventional" resist design, the breadth of detail in the investigation of all potential cyclic olefin polymerization routes, the detailed structure/ property studies performed on materials from all polymerization routes, and the unusually rapid success at gaining a degree of imaging performance on new polymer materials which bore no resemblance to any resist materials yet to be employed.

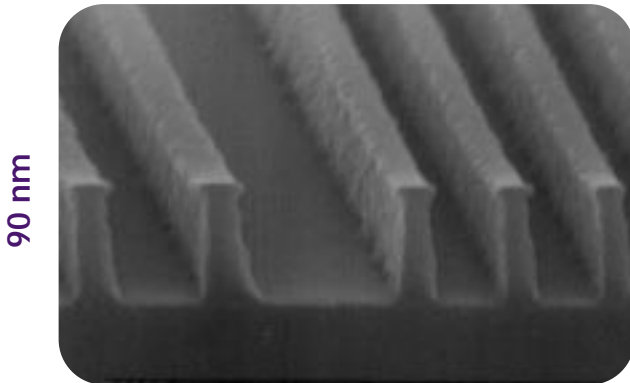
As an industry we see an accelerating push for the introduction of 193-nm lithography into manufacturing before the turn of the century. As such, the development of 193-nm lithography (tools and resist processes) is highly compressed. Never before has

there been more of a need for the contribution of the academic research community in the research of new (193-nm) resist materials.

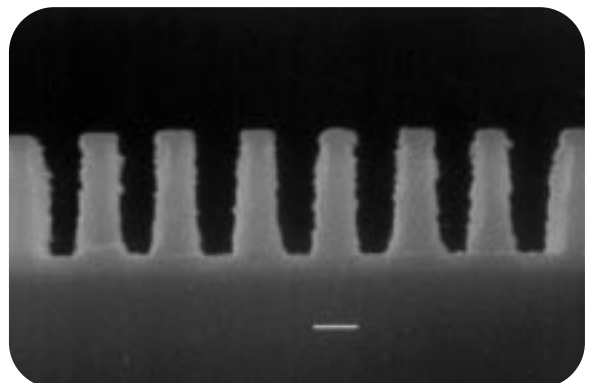
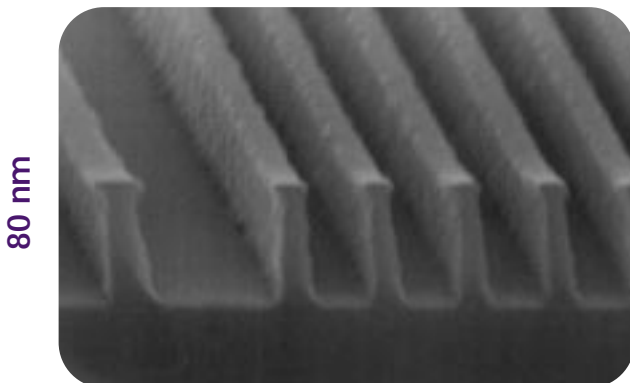
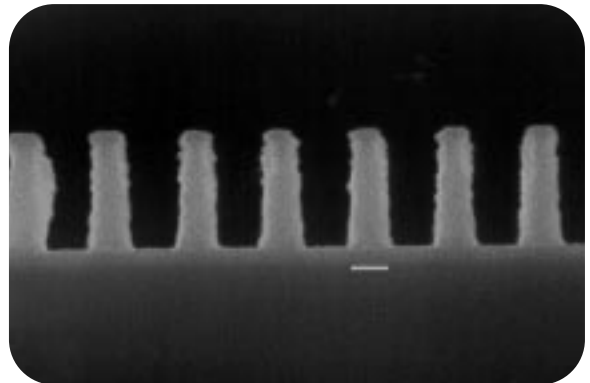
Professor Willson and his students have, perhaps for the first time in the history of the development of photoresist materials and processes, led the industry in pursuit of new, high-performance photoresist. In February, 1998, Professor Willson and his team used their resist design expertise to formulate a resist that produced a dense array of 80-nm features (see photos below). It is almost certain that through the pioneering work of these researchers, a cyclic olefin-based 193-nm photoresist will be a commercial reality.

University of Texas at Austin 193 Resist/Phase Mask Results

1:2 pitch



1:1.5 pitch



Phase Mask donated by DuPont Photomasks
Results imaged at SEMATECH

Student Services

Relevantly Educated Scientific Work Force

750 Students Supported

These young men and women conducted research under SRC contracts and were an outstanding source of technology transfer through internships and permanent hire. SRC members continue to report high satisfaction with the SRC students and designated them as the “most valuable SRC product” in 1997.

104 Graduates (at 1/98)

Of the SRC graduates in 1997, 55% joined member companies, 8% joined university faculties, 3% joined government agencies, 20% joined North American non-member companies; only 2% joined foreign companies.

40 Graduate Fellows

At the beginning of the fall 1997 term, 30 SRC-supported fellowships were in place including the Robert M. Burger Fellowship. Ten company-named fellowships were in place including 2 for AMD, 2 for IBM, 3 for Motorola, 1 for National Semiconductor, 1 for Texas Instruments, and the NIST/SRC Fellowship. The Fellows continue to represent the brightest and best our universities have to offer and to show great promise as the next generation of leaders for the semiconductor industry.

The GFP Conference was co-sponsored by Intel Corporation in Santa Clara, CA. One hundred Graduate Fellows, Master's Scholars and industry personnel attended this event. Nine invited student papers and 37 poster sessions were presented. The highlight of the two-day conference was the keynote address by Dr. Gordon Moore.

4 Master's Scholars

The Master's Scholarship Program was created in 1997 to attract qualified students in under-represented minority categories to disciplines of interest to the semiconductor industry. The Master's Scholars are performing research under SRC contracts at Lehigh University, Stanford University, the University of Illinois and the University of Washington.

Member Access to Students

The move to electronic distribution of student resumes was accomplished in the second quarter of 1997. Resumes for about 50% of the SRC students can be accessed via the Graduate Student Directory on the SRC restricted Web site; resumes are also linked to the Research Catalog through the Graduate Student Directory. Company staffing personnel have the ability to download resumes to internal resume distribution systems.

Student Services Technical Advisory Board (TAB)

1997 was the first full year for the Student Services TAB. This advisory group is different than other SRC TABs in that it includes company recruiting personnel as well as technologists and scientists. Accomplishments for this TAB in 1997 included convening a planning workshop in July hosted by Texas Instruments. The TAB also provided guidance in improving the resume distribution service and actively recruited for the Master's Scholarship Program.



At the GFP Conference, Alumni (L to R) Robert Socha and Matthew Hankinson, both employed by National Semiconductor, discuss research done by current GFP Fellows (L to R) Brad Shutzberg, Jean Kelsey and Simon Karecki.

Aristotle Award Presented at GFP Conference

Professor Kensall Wise, University of Michigan, was the recipient of the 1997 Aristotle Award, presented at the Graduate Fellowship Program Annual Conference in Santa Clara, CA. in September. The Aristotle Award recognizes excellence in teaching through the research process. In their nomination, Professor Wise's former students spoke of him as a teacher ahead of his time, emphasizing quality tools, customer interaction and interdisciplinary research before these were popular methods. He was also referred to as a "learned man, a seeker of knowledge, a teacher, a mentor, an advisor, a colleague, and above all, a very good friend." During his tenure at the University of Michigan, Professor Wise has graduated over 30 doctoral students and has taught several thousand more the art of circuit analysis and design, integrated circuit fabrication, sensor design, micromaching and microfabrication technology, and semiconductor manufacturing techniques.



Dr. Gordon Moore (L), Chairman of the Board of Directors of Intel Corporation and keynote speaker for the Graduate Fellowship Program Annual Conference with Professor Kensall Wise, recipient of the 1997 Aristotle Award.



Master's Scholars

Paul Ampadau
University of Washington

Adreanne Kelly
Lehigh University

Ronald Kinder
University of Illinois

Francisco Machuca
Stanford University

GFP Fellows

Andrew Abo
University of California at Berkeley

Peter Abramowitz
University of Texas at Austin

Daniel Bergstrom*
University of Illinois

Nicholas Bollen,* Robert M. Burger Fellow
Duke University

Michael Booth
Cornell University

Christopher Borst
Rensselaer Polytechnic Institute

Arthur Bradley
Auburn University

Scott Bukofsky
Yale University

Jir-Shyr Chen, IBM/SRC Fellow
Cornell University

Roawen Chen
University of California at Berkeley

Paul Dentinger
University of Wisconsin

Jonathan Doan
Stanford University

Cheryl Faltermeier*
State University of New York at Albany

Joel Fenner, Robert M. Burger Fellow
North Carolina State University

Timothy Fisher
Cornell University

David Fryer, TI/SRC Fellow
University of Wisconsin

Glenn Glass, Motorola/SRC Fellow
University of Illinois

Lawrence Goodby*
University of California at San Diego

Matthew Hankinson*
University of Michigan

Jennifer Havard, AMD/SRC Fellow
Cornell University

Brian Hornung*
North Carolina State University

Gregg Hoyer
University of Washington

Fredrick Huang*
University of Illinois

Anna Ison, Motorola/SRC Fellow
University of California at Berkeley

Simon Karecki, Motorola/SRC Fellow
Massachusetts Institute of Technology

Jean Kelsey
State University of New York at Albany

Steven Levine
Cornell University

Marline Manassian
University of Texas at Austin

Derek Martin
University of Florida

Bruce McGaughy
University of California at Berkeley

George McMurray
University of California at Berkeley

Katherine Mueller
University of Texas at Austin

Shipra Panda, NSC/SRC Fellow
Carnegie Mellon University

Michael Perkins, NIST/SRC Fellow
Stanford University

William Pinello*
University of Arizona

Lance Robertson, IBM/SRC Fellow
University of Florida

Eric Shero
University of Arizona

Brad Shutzberg
Cornell University

Jeffrey Snodgrass
Stanford University

Robert Socha*, NSC/SRC Fellow
University of California at Berkeley

Robert Sumners, AMD/SRC Fellow
University of Texas at Austin

Ronald Sutcliffe*
University of North Texas

Dennis Sylvester
University of California at Berkeley

Bassam Tabbara
University of California at Berkeley

Todd E. Takken*
Stanford University

Martin Tanner
University of California at Los Angeles

Nerissa Taylor
University of Illinois

Shawn Thomas
University of California at Los Angeles

Steven Walstra*
University of Florida

Peter J. VanDerVoorn
Cornell University

Xin Yi Zhang
Stanford University

***Graduated in 1997**

Industrial Mentor Program

The Vitality in Cooperative Research

The SRC Industrial Mentor Program, created by the SRC in 1983, is one of the most effective methods developed by the SRC to provide its members with early access to key technologies, substantial leverage in the explicit direction of technology development, and ultimate transfer of semiconductor technology from the research base to the supporting industry. This program enables industry's best technical people to guide, shape and support the SRC research efforts. Like most endeavors, mentoring requires dedication and willingness to work as a team long enough to create a more valuable research outcome. Each mentor and research team builds their own unique relationship based upon the particular needs of the personnel and the research project.

During 1997, 481 individual mentors from 26 SRC member companies and organizations were involved in SRC research tasks. To recognize their significant contributions, the SRC presents its annual Outstanding Industrial Mentor Award. Seven mentors have been chosen to receive this award for 1997.



Dr. Martin Giles of Intel Corporation:

Dr. Giles has been a mentor to Profs. Robert Dutton and Jim Plummer and their graduate students at Stanford University. As a mentor to this program, he brought experience with software development and the hierarchy of models for diffusion and knowledge of short- and long-term industrial needs to define development in the ALAMODE (A Layered Model Development Environment) project. Dr. Giles has shared valuable advice on the issues of representation for materials and interfaces, and how to map systems of diffusion equations and boundary conditions onto these representations. His understanding of the hierarchy of diffusion models has been a benefit both to help refine the model specification paradigm used in ALAMODE and to help bridge the gap between researchers who concentrate on a single level of the hierarchy

Dr. Ted Kamins of Hewlett-Packard: Dr. Kamins has been mentoring Prof. Dieter Ast and his students at Cornell University, and has shown diligence and strategic foresight in providing guidance and resources. In working with a student on the study of polycrystalline silicon-germanium films, Dr. Kamins supplied films needed for the experimental work being conducted. In another instance, Dr. Kamins was asked a question on the ability to use Ge to put down crystalline seeds on glass at any tempera-

ture between 400 and 580°C, and instead of merely answering the question, he ran his own experiment on three wafers and shipped the results and wafers to the research team.

Dr. Linda Milor of Advanced Micro Devices (AMD): Dr. Milor has mentored Profs. Wojciech Maly and Andrzej Strojwas' research projects at CMU. With Dr. Milor's support, MAPEX was transferred to AMD and other SRC member companies. In her work with Prof. Strojwas and his students, Dr. Milor assisted in finding an application for the defect simulation software, METROPOLE. Dr. Milor facilitated the visit of one student to AMD for a month to collect in-line defect data and for two other students to make subsequent trips to AMD to analyze and collect additional data. Working with the professors and students, she made many improvements to METROPOLE so that a much larger set of defects could be correctly simulated.

Dr. John Sauber of Digital Equipment Corporation: Dr. Sauber has been mentoring the work of Profs. Brian Harper and Vernal Kenner at The Ohio State University. He has contributed in a critical way to two tasks of this research program. In the first task on quantifying fracture resistance of

package structural elements, Dr. Sauber has been responsible for supplying the majority of fracture toughness specimens tested during the program. He collaborated with a fellow mentor in procuring and then molding specimens. He “went to bat” for the program within Digital to bring to fruition a mold for the fabrication of a complicated specimen, and after completing the mold, continued his involvement in refining it during initial trials and overseeing the molding specimens. He has made critical contributions to the task on constitutive data acquisition and interfacing. One of the most important of these was his idea to test DMA as a means for reducing the time and effort required to perform viscoelastic characterizations of electronic packaging polymers.

Ms. Denise Puisto of IBM Corporation:

Ms. Puisto has been a mentor to Prof. Roxanne Engelstadt at the University of Wisconsin at Madison, in mask development and design. She interacted closely with the students and scientists in discussing the results of their models and in providing suggestions for coordinating their mask modeling work and the experimental efforts at IBM/Lockheed. The finite element models developed at Wisconsin to simulate in-situ stress relief were benchmarked with experimental data provide by Ms. Puisto. In a second area of collaboration involving predicting the distortions due to the deposition or removal of multiple stressed layers during the fabrication process, it was again through Ms. Puisto’s efforts that researchers were able to experimentally verify their models to simulate the pattern transfer process.

Dr. Bradley Van Eck of SEMATECH: Dr. Van Eck mentored Prof. Stephen Campbell and his team of researchers at the University of Minnesota. Dr. Van Eck became involved as a mentor to this work involving the detection of small particles in semiconductor processing equipment during the period when the research was being moved from the university

laboratory to the members. Dr. Van Eck contacted industry experts in optical detection and identified the market sector for which PBMS (Particle Beam Mass Spectroscopy), the concept developed at Minnesota, would be most appropriate. When overall SRC budget limitations threatened to preclude the construction of a portable demonstration vehicle which would allow PBMS to be taken to member companies, Dr. Van Eck helped to find the funds to build the system.

Mr. T. M. Mak of Intel Corporation:

Mr. Mak has been mentoring Profs. Joel Ferguson and Tracy Larrabee of the University of California at Santa Cruz. He has played a pivotal role in having UCSC’s inductive fault model and test generation tool suites (Carafe/Nemesis) evaluation started at Intel by starting a cross-site Carafe User-forum at Intel to promote the tool. He also managed a multiple site evaluation of the tool. He has improved the interactions between two faculty members and industry in the area of accessibility to realistic circuits and provided the researchers a better understanding of industry requirements and the relevance of their research to their needs. Mr. Mak arranged internships at Intel for three students on the project. During their internships, Mr. Mak encouraged and arranged for the students to present their work to wider audiences. These presentations gave the students opportunities to get more diverse feedback and a feel of the dynamics of an “industry-style” interaction that is not common in an academic environment.



(L to R) Denise Puisto, IBM; T.M. Mak, Intel; and Linda Milor, AMD are shown with their outstanding Industrial Mentor Awards.

Intellectual Property Report

Preserving Options for the Future

1997 U.S. Patents Issued

Title	Inventor	Issued	Patent No.
Method of Fabricating a Self-Aligned High Speed MOSFET Device	C-M Hu H.Wann (UC/Berkeley)	2/4/97	5,599,728
Process of Making Oxidation High Conductivity Copper Layers	W. Landford P. Ding (SUNY/Albany)	4/22/97	5,622,608
Method of Fabricating Quantum Bridges by Selecting Etching of Superlattice Structures	W. Lynch K. Wang M. Tanner (UCLA)	5/20/97	5,630,905
Selective Low Temperature Chemical Vapor Deposition of Titanium Disilicide onto Silicon Regions	E. Seebauer M. Mendicino (UIUC)	5/27/97	5,633,036
Method and Apparatus for Dual Modulation Laser Spectroscopy	E. Whittaker H. Sun (N7SCOE)	6/3/97	5,636,035
Reactive Membrane for Filtration and Purification of Gases of Impurities and Method Utilizing the Same	F. Shadman (Arizona)	6/3/97	5,635,148
Reactive Membrane for Filtration and Purification of Gases of Impurities and Method Utilizing the Same	F. Shadman (Arizona)	6/10/97	5,635,544
Systems for Performing Chemical Mechanical Planarization and Process for Conducting Same	S. Murarka R. Gutmann D. Duquette J. Steigerwald (RPI)	6/10/97	5,637,185
Water-Soluble Photoinitiators	J. Frechet (Cornell)	7/15/97	5,648,196
Method, Apparatus and Computer Program Product for Determining Frequency Domain Response of a Nonlinear Microelectronic Circuit	R. Saleh J. Mueller B. Antao (UIUC)	9/2/97	5,663,890
Stress-Free Mount for X-Ray Lithography Masks	F. Cerrina J. Wallace (Wisconsin)	10/7/97	5,675,403
SCRAM Cell Utilizing Bistable Diode Having SeSi Structure Therein	K. Wang X. Zheng T. Carns (UCLA)	11/4/97	5,684,737

Another value of SRC membership is protection of technology and intellectual property assets that are developed as a result of SRC support. The SRC has a worldwide, nontransferable, royalty-free, non-exclusive license right to inventions and works of authorship (e.g., software) resulting from SRC-funded research. The SRC sub-licenses such inventions and works of authorship, as appropriate, to SRC Members.

U.S. Patents which issued in 1997 included additions to existing technology portfolios in the areas of advanced devices (including SiGe superlattice quantum well devices and a self-aligned, high-speed SOI MOSFET), and in lithography (tools and water-soluble photoresists). The reactive membrane filter patents, developed at the University of Arizona under SRC and SEMATECH funding for contamination-free manufacturing research, exemplify successful 3rd party, infrastructure organization technology transfer.

Overall, the SRC added 12 newly issued U.S. Patents to its intellectual property portfolio, bringing the SRC's total number of issued U.S. Patents to 150. The table on this page lists SRC U.S. Patents issued in 1997. Eight new U.S. Patent Applications were filed in 1997 from invention disclosures developed as a result of the SRC research program funding.

Moreover, in 1997, 86 software submissions (26 alpha releases; the remainder as upgrades) were logged having been authored as a result of SRC support. Two significant programs include the POLIS/0.2 software, developed at University of California at Berkeley, and an upgrade of VIS release 1.2, co-developed by collaborators at University of California at Berkeley, the University of Colorado at Boulder, and University of Texas at Austin. POLIS is a co-design environment for the synthesis of hardware/software in embedded systems. VIS is a software environment for synthesis and formal verification of digital circuitry.

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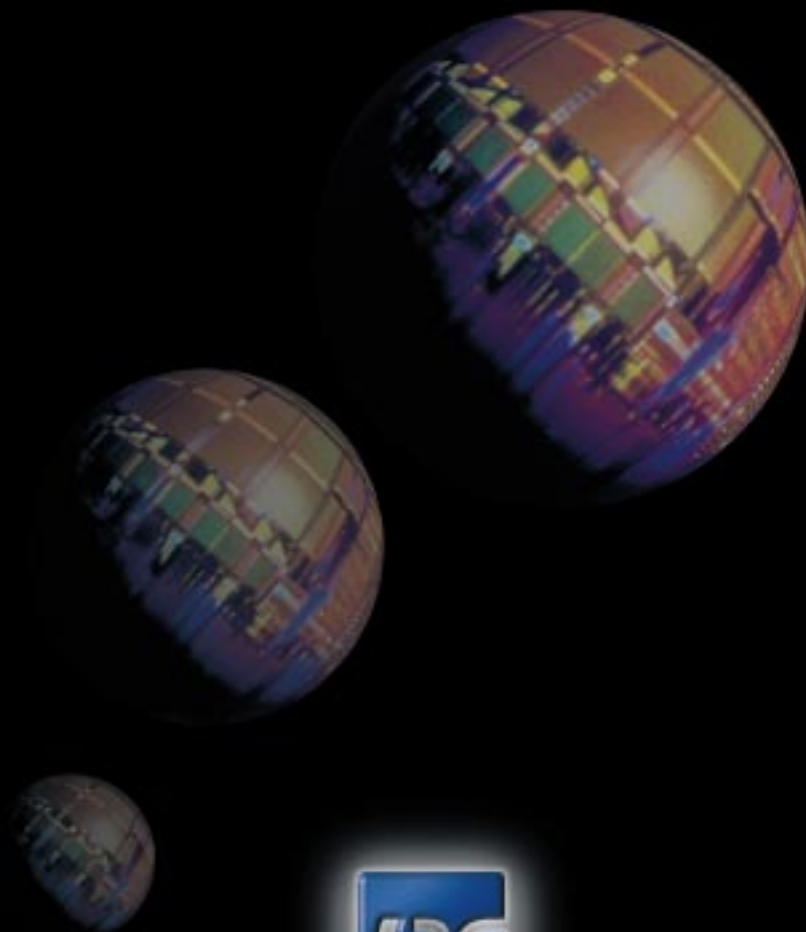


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