COOPERATIVE RESEARCH

The New Paradigm

Semiconductor Research Corporation

ROBERT M. BURGER

FOREWORD

Springing from the invention of the transistor in 1947 and the integrated circuit in 1959, the semiconductor industry became the industrial world's pacemaker in 1995. Markets for semiconductors passed $150 billion/year and were expected to continue their rapid growth to the end of the century. Less advanced nations were using successful participation in the semiconductor industry as their yardstick for progress. Earlier, competition in semiconductor markets, and the rules that govern it had been a bilateral concern of Japan and the United States. In the mid-nineties, it had become a multilateral, world-shaping issue that promised to persist for decades as nations jockeyed for relative advantage. In 1997, this situation changed when the underpinnings of the Asian economies began to unravel with major effects in the semiconductor industry throughout the world. Maintaining market levels became an elusive goal and projections became history. This narrative, however, probes the prior history that brought semiconductors to the forefront of the world economy and, in particular, the SRC paradigm for cooperative research that contains lessons for the future.

There are three roads to success in semiconductor markets; low cost, a protected substantial home market, and technology leadership. The United States cannot be a low-cost producer. As long as labor is a significant percentage of product cost, the advantage is clearly with low-labor-cost, less-developed countries. Other cost factors; capital, skills, and raw materials are equilibrated rapidly in free markets.

Subsidies and trade barriers have been and are being used by all nations to protect home markets and gain economic advantage for domestic industry. The U.S. doesn't use these artifices to manage trade in semiconductors or manufactured goods, in general, but does in mature economic sectors such as agriculture and steel. Semiconductor trade barriers have been used by other countries seeking to protect domestic markets. These have taken the form of both direct barriers such as duties and quotas, and indirect barriers such as "locked-in" customers and high administrative hurdles. The trend is in the direction of removing both overt and covert trade barriers. The U.S. semiconductor industry, generally, has been in favor of removing all trade barriers with the exception of those required by national defense.

In 1998, the success of the United States in the semiconductor industry was based on technology leadership. This required a continuing stream of innovation in both technologies and products to provide a time-to-market advantage. For semiconductors, being first in the market

provides high profits until the product is either supplanted by a next generation product, or becomes the ubiquitous product of low-cost producers. This time advantage is being compressed. It is now less than two years. The strong R&D structure required to maintain this narrowing gap is essential for U.S. market leadership.

The ingredients of technological leadership; motivation, education, investment, good management, and unrestrained competition, are well known. The integration of these in a research and development enterprise fueling successful businesses has been demonstrated most effectively in the United States semiconductor industry. However, the structure of competition is changing and the U.S. industry must adjust.

In the late 1970's and early 1980's, it became apparent that the basis of U.S. technology leadership in the semiconductor industry had been altered. No longer could U.S. corporations like AT&T, IBM, Xerox, Westinghouse, and General Electric maintain large internal research laboratories as in the past. These laboratories had provided significant competitive advantage for their corporations as well as for all U.S. industry by advancing technology on a broad front. However, they had become financial burdens limiting corporate competitiveness. At the same time, it was clear that U.S. industry could not sustain technology leadership without a productive research activity.

Fortunately, this dilemma was recognized by members of the Semiconductor Industry Association who, in 1982, created a cooperative research organization, the Semiconductor Research Corporation(SRC). Its purpose was to organize and carry out a cooperative university-based research program for its members in the U.S. industry. SRC has responded well. Over the ensuing eighteen years, it has invested over one-half billion dollars in semiconductor research in U.S. universities. Well over 1000 graduate students have participated, gained highly relevant experience, and graduated. Most are now working in U.S. semiconductor companies. In the process, a valuable array of research results have been transferred first to SRC members and then to the U.S. industry. These research results and students have become important ingredients of the U.S. industry's technological leadership providing the essential innovation and invention.

In this book, the SRC experience provides a tutorial on the role of industry cooperation in twenty-first century technology-based industry competition. Cooperative enterprises do not have smooth growth paths. A strong committed leadership and new avenues of communication and interaction are required. A consensus on goals and objectives must emerge from a series of

compromises. Cooperative research is a learning and education process with little precedent. But it is a road that U.S. based technology-driven companies must travel to remain viable in this new industry environment. More recently, the SRC has become aware that, no matter how good the original model may have been, it would have to continually change in order to retain the industry's allegiance. And, it is changing.

At least one question arises in this story that remains unanswered. It is assumed that competition is essential to progress. Nowhere has this been demonstrated better than in the U.S. semiconductor industry. The question is: 'In the twenty-first century, who will be the competitors?' In the past, SRC assumed national or regional competition, i.e., the industries of the Americas vs the European Common Market or an unidentified Asian organization. In the U.S., the semiconductor industry is the designated competitor or, at least, that part of it that participates in the SRC. This keeps alive the prospect of an industry and government partnership that provides economic advantage to the participants. On the other hand, semiconductor companies are also entering into technology and product alliances independent of political boundaries. Future competition could be between these multinational alliances. This has advantages in enabling optimum use of unique regional strengths, the software skills evident in India or the manufacturing skills of Japanese companies, to provide stronger competitors, and inhibits tendencies to gain advantage by managing trade and markets. Multinational alliances are, to some extent, a product of U.S. anti-trust law that has discouraged product focused alliances within the U.S. industry.

The ultimate form of semiconductor competition will profoundly affect the future of cooperative research, e.g., the SRC. The possibility of SRC becoming international was considered several times and rejected. At the turn of the century, it is becoming a reality. In the long run, this decision will change the nature of technological competition, perhaps to focus on device applications rather than on device technology. Some altered form of competition will be required to sustain progress. This book may help make the dilemma clear. At the least, it relates the many aspects of a highly relevant experience.

PREFACE

This book records fifteen years of experience in cooperative research in the Semiconductor Research Corporation, better known as the SRC. It sets the stage, describes the creation, and reviews the many facets of the SRC experience. SRC is still learning how to successfully carry out cooperative research even as success in cooperative research is becoming an increasingly important imperative for industry. That is the focus of this book.

In the 21st century, cooperative research, in some form, will become the widespread paradigm for commercial success. Experience tells us that companies cannot, on their own, carry out the full spectrum of R&D required to maintain competitiveness in high technology. Nor is the government the solution. The Government has demonstrated unmatched inefficiencies in acquiring and applying resources to needs of industry. Determining the overhead cost involved in collecting, authorizing, administering, and managing the distribution of applied research funds by government, and the resultant returns on these investments, is left as an exercise for someone else. It is high. However, government does have an important role. The U.S. government does an excellent job in funding basic research disassociated from products and services. It has also funded much of the research required to advance the Nation's agricultural productivity, its health care, and its military strength (where efficiency has been of secondary importance). The role of the Government in basic research is unquestionable. In the applied research required for industrial competition, there is a better solution, industry cooperation. One must emphasize, however, that government participation in cooperative research with industry is welcomed and provides considerable benefits. Without question, the SRC has gained significantly from such participation.

Cooperative research in support of its membership is the purpose of the SRC but it also interacts with government, industry organizations, other companies, foreign research organizations, and university 'intellectual property offices' on issues associated with semiconductor research and technology strategy. Although usually productive in increasing the overall efficiency of the R&D process, these interactions are often secondary in importance and can divert SRC from its mission and diminish the value of its research - but they are necessary and affect research in important ways. Thus, technology strategy as in the "Roadmap" is important because of its strong influence on R&D efficiency and effectiveness. For industry, working with the Government can increase the productivity of relevant research activities and enable more rational regulation of the industry, i.e.,

safety, health, environmental impact, and export controls. Cooperative research must be carried out the real world defined by the many organizations with which it must coexist.

Government agencies are welcomed as participants in the SRC not just because of their financial contributions but also because of the different perspectives they provide and the benefits that accrue from coordination with their substantial research programs. These and the productive interactions of the SRC with other industry organizations are discussed in appropriate chapters. However, the fact that SRC exists to foster and fund cooperative research is the primary message. It is too easy to become consumed by these many diversions.

I have tried to make the story interesting and informative for all readers, not just the SRC enthusiasts who might read it anyway. This is not easy. Connecting with non-participants through their interests in technology competition, industry cooperation, industry-government linkages, and evolving paradigms for future technology advances is the challenge. The SRC experience provides a rich lode that readers can learn from and apply in other areas. My aim is to make that experience available. You can measure my success.

This book has been a pleasure to write because of the associations and experiences it has brought back. However, writing such a history is an undertaking that I will not recommend to others. There are many diversions that slow the pace and prolong the task. Also, for one who has participated, it is difficult to rise above the churn of events to see the lay of the land. I have eased my task somewhat by minimizing use of names, especially of SRC staff, and avoiding attribution of individual accomplishments.

As in any e nterprise, differences have existed in the SRC not only on which turn to take next but also on what turns were taken in the past, whether they led to success, and who's responsible. Everyone is right, sometime, and most successes have many fathers. But that is not the story that I'm trying to tell. The story told here is that members of the SRC team, some here, some gone, have shared in its successes and failures. However, since there are many more of the former than the latter, there is ample credit to share.

Even as I try to compensate for being only a part of the SRC experience, the reader must recognize that some tunnel vision is inevitable. One writes about what one hears, sees, and understands - not what one doesn't hear, see, or understand. I am reminded (with apologies to Bob Donovan) of the blind man and the elephant - what the man "sees" depends on what part he happens to touch or smell. The trunk, the flank, and the tail provide completely different sensory reactions.

It is left to you to conclude from what perspective I am writing this account of the SRC.

Many people have provided information and corrections that have improved this account immeasurably. I thank them. This includes the SRC staff who are listed in Appendix B. My method has been to review documents saved from the 'black hole' of all paper records, i.e., off-site storage, and to distill the relevant material therein. Studying the minutes and actions of the Board of Directors, the Technology Advisory Board, and other committees has helped maintain perspective. In particular, having been part of the SRC history, I have used this documentation to restore my memory of events. The objective has been correctness, but I recognize that if opinions and perspectives are completely omitted, my primary objectives would not be realized. I also note that completeness is limited by time, productivity, and energy, thus also limited.

While this book is a task that I have planned for several years, its realization would not have occurred if Larry Sumney had not discerned that now is the time.

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CHAPTER 1

THE QUESTIONS

"The purpose of this letter is to invite your company to participate in a new cooperative research venture with other companies in the semiconductor and closely related industries. The purpose of the effort is to enhance basic research in semiconductor disciplines."

The above introduction was used by Erich Bloch, then a vice-president of IBM, to obtain commitments from companies that would become the founding members of the Semiconductor Research Corporation (SRC), an industry-based cooperative research organization. The letter was dated March 31, 1982.

The SRC funds research in U.S. universities that; (1) responds to technology needs of the semiconductor industry, (2) is within the scope of university activities, and (3) provides industry-relevant research experience to participating graduate students. This research often provides the 'seed-corn' for the rapid technology progress essential to the continued performance growth in semiconductor products. At first, this performance growth maintained U.S. industry leadership and now aids in the continued performance growth of the leading semiconductor manufacturers throughout the world..

SRC exists because market competition forced increases in company resources being used for short-range product development with a decreasing share for long-range research. The industry created the SRC in order to merge these decreasing shares with those of other companies to sustain an effective and essential research activity.

Some industry managers question the importance of the universities in the current achievements of the industry but even they will acknowledge that well-educated engineers and scientists are essential. And for those who look closely, the seeds of many important advances are found to have their origins in university laboratories, even in semiconductor technology.

Today, the semiconductor industry cannot rely on government funded research to sustain technology progress. Reductions in government funding have made industry-funded cooperative research necessary. Equally important to many SRC members is the ability of graduate students who participate in SRC funded research to rapidly become productive contributors to the continued success of the companies they join.

This is the nub of the SRC experience. The lessons learned should help in the conceptualization and structuring of similar cooperative activities and can be an increasingly

important factor in the beneficial-to-progress competition among national economies.

Although other cooperative industry research organizations preceded it, the SRC is unique in focusing on technology needs, students, and competition; and in becoming important to the success of a rapidly-growing leading-edge industry. This experience provides a useful template for other industries faced with similar challenges.

SRC was founded in 1982. From the start, a few omnipresent core issues have influenced its governance and activities. This chapter identifies several of these issues so that the rare person who reads a book from beginning to end will be rewarded by having them implanted in his mind before being exposed to the details. Six seminal issues are identified: life-span, academic capabilities, agenda, independence, growth, and role. They are intrinsic to the basic ***raison d'etre*** of the SRC and key to the broad applicability of the cooperative experience.

The SRC experience in cooperative research can set the direction for important changes in the next century as businesses search for appropriate balances between costs, cooperation, and growth.. We must learn from the SRC experience so as not to retread the same ground. All too often such experiences are repeated, and at a very high cost.

Another question that periodically arose is 'Why not make the SRC an international organization?' In responding to this question, a second question arises; 'If an organization is created to enable its members to more effectively compete and this becomes the force that motivates its performance, what is it's purpose if every significant competitor joins the organization?' These are important issues that will be addressed.

LIFE-SPAN

In 1998, a 74-year old citizen of the U.S. was 1/3 as old as his country. The SRC is much younger, sixteen years. Often the youth of countries and organizations seems to correlate with vitality and productivity, making its youth an important American asset. However, organizations that continue to exist past their period of usefulness are familiar, even in America. It is not difficult to find examples of both relatively young but moribund and relatively old but vibrant organizations. The ability to recognize and appropriately respond to both types of organizations is a necessary ingredient of progress.

Finite life-spans for research organizations such as the SRC are advisable. The question is what that life-span should be, and the correct answer varies widely with circumstances and subject.

Some organizations should die before they are born and others should continue to live beyond the well-defined future. The National Advisory Committee on Semiconductors, in its four-year life, demonstrated limited effectiveness. It is an example of an appropriately deceased organization. The National Science Foundation is a half-century old and remains vibrant.

There is a satisfaction in creating organizations that both attracts and destroys. While a new organization may be an effective response to a challenge, too much of this creativity destroys productivity. Success requires creation of organizations to be followed by creation of results. These results may take many forms, e.g., new knowledge or products for sale. Markets then determine winners. The importance of an organization is determined in this production phase, after the 'creation' has been completed. Constant re-creation, often in lockstep with a term of office, is common to many government organizations and limits productivity.

The SRC has operated for 16 years, since 1982. It works with universities that change slowly. Its staff is renewed, partly through use of temporary industry assignees and partly from turnover in its permanent staff. Through 1996, the 'permanent' SRC research management staff had included a total of 22 people in fourteen years, 10 of these remained at that time. This staff includes the president and vice-presidents. The average tenure of the technical staff at the end of 1996 was less than four years.

The life span of the SRC should be set not by years but by the productivity of its research. Research tasks are evaluated regularly and, although 50 percent of the first dozen SRC research contractors remained active participants after sixteen years, the research they conducted had changed many times. The characteristic lifetime of SRC research tasks is between 3 and 6 years. With renewal of both people and program, SRC should retain its vitality for the foreseeable future. With alert management, it should be capable of continuing without a near-term limit and without diminished productivity. Renewal and refocusing of research tasks and management, and the flexible institutional environment provided by universities, should maintain the productivity of the research, but it will remain as a continuing challenge to SRC management to maintain its relevance.

ACADEMIC CAPABILITIES

In research, the characteristic overlapping phases of projects: creation, build-up, high productivity, diminished productivity, and termination, must be recognized and dealt with. The optimum time period associated with each phase varies. In universities, a new contract may create

a new research effort but, more often, it continues or expands ongoing research. It may require new equipment or facilities. Usually, it is necessary to expand the research staff, i.e., recruit new graduate students. The availability of graduate students correlates with the academic calendar so the build-up periods for new research efforts vary greatly. It can easily be a year or more before a new research effort becomes productive.

In universities, even after a team is assembled and facilities allocated, it may take longer to become productive than in industry. This delay results from the part-time nature of university research, the limited tenure of its productive staff, limits on space and resources, and interference from higher-priority activities, education for example.

The cyclic productivity of university research contracts is a variable that must be recognized and dealt with. Productivity is interrupted when a graduate student completes his degree requirements, graduates, and departs. Sometimes a project ends with a faculty member moving to another institution. In some cases, research productivity decreases precipitously when results indicate that a dead-end or a rational endpoint has been achieved, i.e., the results are negative. Sometimes the productive phase of innovative university research can continue past the immediate milestones and even beyond the tenure of key faculty when the research environment is attuned to industry needs. 'Productive,' in the context of SRC research, means creating results that are applicable to industry technical needs, either now or later. The connection to needs is central.

The quality of SRC research is dependent on the people performing it. The natural tendency of SRC program managers is to defend the program, arguing that it is difficult to find other participants who will be as productive. **They are right.** A large percentage of the university faculty with silicon integrated circuit capabilities are involved in SRC research. Most have proven themselves through their research. In 1997, about 212 faculty investigators in eighty-one research organizations participated in SRC research. This constitutes a solid majority of those qualified. Arbitrary changes in participation can lead to less useful results. SRC supports its productive core of proven researchers while continually providing opportunities for others to demonstrate competitive capabilities and join this group. However, the ability to do this with a constant or decreasing budget level is limited.

The participants in SRC research change by about 10 percent per year. Change can involve new tasks within a continuing contract or a new contract. Personnel changes may be but are not necessarily involved. Continuous change in the participants may be beneficial, but excessive change

reduces productivity. SRC has recognized that stability is important as it introduces its agenda directed to industry's needs.

AGENDA

Inputs from SRC member companies through the Board of Directors, the Technical Advisory Board and mentors assures the continued responsiveness of SRC research to industry technology needs. The challenge is to distill from the variety of inputs, a coherent agenda that is consistent with both the needs of a majority of the membership and the capabilities of the university participants, and that makes the most effective use of the available resources. Doing this is formidable challenge that is never fully achieved.

Research needs of SRC members cover a wide spectrum reflecting the size of the company, the nature of their products, and the nature of their R&D activities. These needs will seldom be congruent with the collective agenda of the SRC particularly since its membership includes not only the core integrated circuit manufacturers but also fabrication equipment makers, fabless IC companies, and design software companies. In general, smaller companies are interested in short-term needs relating to their next product while the interests of larger companies are more focused on long-range exploratory research that helps define new methodologies or products.

SRC's research agenda has been significantly influenced by the creation and operations of SEMATECH as well as by Government participation in the SRC. Through 1996, SEMATECH had provided 22 percent of SRC revenues and the government, 3.3 percent. By 1997, these revenue sources had been reduced to a total of less than 2 percent of SRC revenues with little expectation for future increases. Consistent with this, the current SRC research agenda is influenced by these organizations only insofar as their semiconductor related R&D is recognized in the formulation of SRC's research activities.

INDEPENDENCE

SRC is an operationally independent subsidiary of the Semiconductor Industry Association (SIA). The SIA Board of Directors (BoD) elects SRC Directors each year. The stronger connection is that the majority of SIA directors are senior officers of SRC member companies. The SRC BoD consists of the research or technology executives of these companies. The result is that the position and role of the SRC in the broad scheme of industry activities is determined by the SIA Board level

executives while the internal affairs and operations of the SRC are addressed by SRC's Board. The SIA Board is thus somewhat remote from SRC's research activities.

This is important when considering the structure of industry cooperative activities, particularly SRC and the cooperative development activities of Sematech (see Chapter 12). On several occasions, it has been suggested that the industry combine the SRC and Sematech. The SRC has argued against combining these two activities noting that the smaller research effort can readily be subsumed and lose its identity in such a merger. SRC holds to the view that long-range research is essential and should be pursued independently of cooperative development in order to maintain its quality, identity, and mission. This discussion is complicated by the natural tendency by Sematech toward increased involvement in university research since this constitutes the major research activity external to the industry. Semiconductor research is also carried out in government laboratories and, to a limited extent, in independent not-for-profit research institutes.

GROWTH

The annual income of the SRC is shown in Table 1-1. After an initial four years of growth, income decreased in 1986 because of a 12 percent decrease in 1985 sales of the semiconductor industry. In 1988, income increased by $9M when Sematech funded SRC to establish a university research program in semiconductor manufacturing technology and SRC membership expanded. After several years of growth, SRC income became almost constant, varying less than 4 percent from the average from 1990 through 1995. In this same period, U.S. integrated circuit industry shipments increased from $20B to over $50B, a 2.5X expansion. The relatively constant SRC income resulted from a fee structure that limited any one member's fee to 15 percent of the SRC budget. In this 6-year period, steady cost increases for research resulted in a decreasing effort. This decrease was worsened in 1996-1997 when Government participation in Sematech was phased out and Sematech support of university research through the SRC was halted. SRC's Board of Directors subsequently took steps to replace Sematech funding and to provide resources for increasing SRC's budget more in line with industry growth.

ROLE

Even as the SRC has established a productive research base for the U.S. semiconductor industry and provided an increasing stream of useful results and well-educated students, questions

Table 1-1 ANNUAL INCOME FROM ALL SOURCES

Year	Income ($M)	Year	Income($M)	Year	Income($M)
1982	3.9	1987	17.6	1992	35.0
1983	6.1	1988	26.6	1993	34.8
1984	11.9	1989	28.0	1994	35.2
1985	19.7	1990	35.4	1995	36.5
1986	16.7	1991	35.2	1996	39.4

continue to arise as to its role, and as to the rationale that supports this role. These questions are reenforced by the fact that significant U.S. producers of integrated circuits do not belong to the SRC and do not appear to be materially handicapped by their non-participation. Moreover, much of the research output of the SRC appears in publications before it becomes applied by member companies and some of the students are also hired by non-members. Is the return-on-investment by members of the SRC appropriate?

There are several answers to these questions. Brief answers are given here and more complete answers are found in other chapters of this book. First, those things that would not exist without SRC include;

1. a relevant, productive, silicon device related, university research program in U.S. universities,
2. IC research results in design, microstructures, manufacturing, and packaging sciences currently being used by U.S. industry,
3. an additional 3,000 graduates with advanced degrees and relevant IC research experience added to the industry's manpower base, with an additional 300 graduating each year,
4. industry technology leaders working together to define needs and strategies through the "SIA National Technology Roadmap for Semiconductors",
5. hundreds of industry scientists and engineers serving as mentors to university faculty and students engaged in SRC's semiconductor research,
6. the National Advisory Committee on Semiconductor and its successor, the Semiconductor Technology Council,
7. significant additional support for integrated circuit research that was incentivized by the SRC,
8. Sematech, and
9. an altered paradigm for cooperative R&D.

There is little doubt that the crowning achievement of the SRC is the creation of a productive university research activity addressing integrated circuit technology. In January 1982, there were only a few isolated pockets of integrated circuit (IC) research in universities, mostly related to design. Fewer than 100 graduate students were involved in IC relevant research. A few years later,

there were well over 1000 graduate students directly supported by the SRC and others supported by research that was a direct result of SRC's existence. Industry needs for graduate scientists and engineers with relevant advanced training were being met. The basic research pipeline on which the industry depends had been restored.

This was the role assigned to the SRC in 1982 and one in which it has been very effective. In fact, one SRC problem is, that by motivating large increases in university silicon-device-related research, the need for the SRC has become less apparent. This is sometimes exacerbated by inadequate attention to attribution of research products by both SRC and its contractors.

SRC research results are published and become available to the entire industry. In fact, integrated circuit technology has enabled the lowering of communication barriers that once delayed oversea dissemination, e.g., the Internet and E-mail. However, SRC research provides significant unique value to SRC members including:

- early awareness of research results and opportunity to use these before they are broadly disseminated,
- the ability to steer research in response to individual needs,
- the opportunity to participate in leading edge research,
- early contact with graduate students conducting SRC research thus providing hiring advantages,
- participation in the planning, selection, and evaluation of research with other SRC members, and
- non-exclusive royalty-free rights to intellectual property produced by SRC supported research.

These are non-negligible advantages in the highly competitive integrated circuit world but require action on the part of the member companies before they pay off. Companies whose membership is passive receive fewer benefits.

SUMMARY

This initial chapter has attempted to open your eyes to some fundamental questions associated with the SRC's future;

- ***how long it will exist (tenure),***
- ***how long it should support given researchers or research (agenda),***
- ***whether to merge it with other industry cooperative activities (independence),***
- ***what size should it aspire to (growth), and***
- ***what is its mission in the broad spectrum of semiconductor research (role).***

These questions should rest in the back of your mind as you read this book. For those readers looking to emulate the SRC in other industries, take care. The conditions that permit success are

formidable. For readers associated with the semiconductor industry, be aware that the SRC may be necessary but not sufficient to assure continued competitiveness.

The following chapters will briefly review the history of semiconductor technology before the establishment of the SRC commencing with the invention of the transistor, the environment in which the SRC was created, its startup period, and its research agenda. The evolution of the industry research goals in the SRC as they evolved to become the industry's technology goals is dealt with in Chapter 6 after which the SRC research agenda, its financial history, and its advisory structure are discussed. These chapters are followed with descriptions of the SRC Summer Studies, SRC publications, and interactions with other semiconductor research organizations. The complexity of a cooperative organization's interactions and its interfaces with other organizations and its members are discussed in Chapter 12 which is appropriately titled, 'The Technology Maze.' The important lessons learned by the SRC are reviewed in Chapter 13.

The final chapter speculates on the future of semiconductor technology and of cooperative research. The overall purpose of this book is to record SRC's experience in the hope that this will provide guidance for its members and leaders as they shape the future, and for other cooperative organizations with a concern for the competitiveness of U.S. industry.

The basic tenet of the author is that competition breeds progress but that competition does not exist without identifying the competitors. The competing sides must be comprised of like-minded corporations that recognize cooperation is a requirement for survival. The author of this history is biased toward competition between groups defined by national or regional boundaries. Entangling webs wandering willy-nilly around the world through continents and countries become very complicated and eventually dilute the competitive fires. National or regionally defined competition has the advantage that it becomes an acceptable objective of governing bodies which then may help fuel the competitive fires.

CHAPTER 2

THE STAGE, 1958 - 1981

The same participants who appear as logical intelligent human beings in a history often seemed to behave as incompetent madmen in real time.

The environment of American technology and industry in the 3½ decades that began with the invention of the transistor (1947) and ended with the establishment of the SRC (1982) underwent dramatic change. In 1947, U.S. industry was in its post-World War II euphoria with little significant economic competition. At the end of this period, strong competitors existed in every industry sector and American industry was beginning the difficult task of adjusting to the competition. In those years, the U.S. provided leadership in the transition to a world economy from the pre-war national and regional economies that had stifled progress. Major restructuring resulted. Global competition began to define winners and losers. Ship-building and shoe-making were losers in the U.S.; computers and semiconductors winners. But the competition never ends. In every economic sector,

Table 2-1 BACKGROUND - SEMICONDUCTOR DEVICES

So as not to limit the readership to those erudite in the argot of integrated circuits or electronics, I will, in this chapter, pause to give appropriate instruction.

This is the initial offering.

A semiconductor is a crystalline material that carries current through the motion of either electrons or electron vacancies (holes), the normal densities of each are controlled by trace impurities.

Semiconductors are important because they are the material from which transistors and integrated circuits, the building blocks of modern electronics, are made.

Silicon is the most common semiconductor.

A transistor is an electronic switch or amplifying device formed in a semiconductor material by introduction of impurities in defined regions. The planar transistor used in integrated circuits is formed by diffusion of impurities into the silicon through an oxide mask pattern with minimum dimensions as small as 1/4 micron.

A micron is one one-millionth of a meter. For perspective, it takes over 25 thousand microns to make 1 inch.

An integrated circuit or IC is a sliver of crystalline silicon onto which is formed a microscopic pattern of interconnected transistors that provide complex electronic functions such as signal processing, memory, and computation. It is typically smaller than a postage-stamp and can embody millions of transistors

competition continues until winners are clearly defined and the economic barriers for challenging the winners become so high that competition shifts to other industries. U.S. industry is competing vigorously in high technology industry, particularly semiconductors. In the seventies, the competitors of the U.S. semiconductor industry were headquartered in Europe; in the eighties, in Japan; and now, in the nineties, all of these plus other Pacific Rim nations. In this industry, the U.S. led for the first 3½ decades, than lost, and later regained the lead. The SRC has become an important industry weapon in this competition largely because the strength of the U.S. industry lies in technology leadership.

SRC can be viewed as either a transient response to a critical need or an essential link in the evolution of a more productive industrial structure. History will decide (I vote for the latter). In either case, SRC was created by a rapidly changing industry to fill an essential need, and rests on the results of over sixteen years of fruitful experience. In any case, it is useful to examine this experience.

To set the stage, it is sufficient to review events from the invention of the integrated circuit in 1958 through the subsequent two dozen years. A few 'before the IC' paragraphs are provided for background. This chapter traces the IC history up to that time in the early eighties when the SRC was established.

PRE-IC TO 1958

After the major electronic technology advances in World-War-II, the large potential value of digital computers became apparent at about the same time that their limitations became exposed. The complexity level and thus the capabilities of computers employing electron tubes, the best logic switch then available, were limited by the finite lifetime of these devices, thousands of hours at most (still much better then the electro-mechanical relays of earlier computers). The hot filament in one of the thousands of tubes would burn out, usually just before an important computation was completed. These failures appeared to place a limit on the size and thus the capabilities of digital computers. The removal of this limit became an important goal. (The apparently insatiable demand for more powerful computers continues today, over fifty years after the first electronic computer was built and after many orders-of -magnitude increases in their capabilities).

The barrier to increased computer capabilities posed by vacuum tube failure was short-lived. In 1948, the transistor with no filament to burn out was invented. Theoretically its life was unlimited

since there is no inherent wear-out mechanism. This enabled the building of larger computers addressing larger problems, and uncovered the next fundamental limitation, interconnection failures. It is not very logical that the solder joints connecting electronic components would become the prime determinant of system reliability. After all, these connections are made with molten solder fusing metal conductors already in close contact into a solid conducting bridge. Nevertheless, small size, contamination, and the properties of the metal solders resulted in open connections and system failures when large numbers of solder joints were involved, as in computers. A typical computer in 1960 had hundreds of thousands of solder joints. Innovative approaches to reduction of interconnection failures in electronic circuits were proposed and investigated, e.g., micromodules, cordwood, thin films, and thick films. Each had merits and some, thick films for example, have found market niches resulting in sales of millions of these circuits, even today.

One proposed approach was the monolithic silicon integrated circuit in which the components and connections were formed in large batches within or on a solid substrate, a silicon single crystal wafer. When integrated circuits were first demonstrated, there were sincere proponents of other approaches who vehemently debated their relative merits in technical meetings. Needless to say, the integrated circuit approach won, but not just because of reliability. Cost became a stronger argument. With hundreds of circuits being formed at the same time in one series of processes, the IC won the cost competition hands down.

INVENTION, 1958 - 1962

Jack Kilby (Ref 1) tells us that, in 1958, ICs sprang from a thought process that began with thick film circuits formed on ceramic substrates, and matured in circuits formed on and within silicon single-crystal wafers The essential idea of the integrated circuit is that many complete electronic circuits are formed simultaneously on a silicon wafer through a manageable series of batch fabrication steps and subsequently the individual circuits are separated, packaged, and assembled into useful electronic systems. Processes such as diffusion, epitaxy, ion implantation, oxide masking, deposition, and photolithography are employed, today, in forming these monolithic structures. Savings ensued from the reliability of the monolithic structures, the elimination of the component suppliers and circuit assemblers, as well as from the overhead costs associated with this industry structure. Most important, however, is the simultaneous batch fabrication of hundreds or even thousands of complete integrated circuits, each small when compared to circuits assembled

from separate components. The resulting integrated circuits are as reliable as a single transistor.

Concurrent with the invention of the IC was the development of the planar technology at Fairchild using lithographically patterned oxide masks for impurity diffusion and to pattern the metal layers for interconnections. This was the key to the success of the IC. Without the planar process, batch processing of ICs would not be possible and IC costs would be too high for wide spread use. The planar process is based on Bell Laboratory research on oxide masking, exhibits no inherent failure modes, and provides process yields comparable to that of individual transistors using a similar series of process steps. (In 1995, Texas Instruments continued to receive royalties from the basic integrated circuit patents that resulted from Kilby's work.) The first integrated circuits consisted of tens of equivalent components. Today, they can consist of tens of millions. IC interconnections are microscopic in size, formed from metallic conductors, deposited at high temperatures, fabricated

Table 2-2 BACKGROUND - PN JUNCTIONS AND TRANSISTORS

A semiconductor junction is the interface between n-type and p-type single-crystal semiconductor material. In n-type material, electrical current consists of a net flow of negative particles, i.e., electrons as in metallic conductors albeit with a smaller controllable number of electrons. In p-type semiconductor material, current results from a net flow of positive charges, i.e., electron vacancies or holes. The junction allows the electrical current to flow in one direction and blocks the flow in the opposite direction. When current flows, majority carriers from one side of the junction are injected into the other side where they become minority current carriers. The excess minority carriers are gradually eliminated by recombination with majority carriers.

There are two basic types of transistors, bipolar and field-effect (or unipolar).

The bipolar transistor consists of a small emitter, a very thin base, and a collector. For example, in an npn transistor, the base consists of a very thin layer of p-type semiconductor separating the n-type emitter and collector. Forward current that flows through the emitter-base junction becomes a minority carrier current in the base and a reverse bias current in the base-collector junction. The close spacing of the junctions enables the minority carrier current to drift to the collector junction with negligible recombination Power amplification results when the same current flows through the low impedance emitter junction and the high impedance collector junction.

The field effect transistor operates through voltage control of the conductance of a surface inversion channel through which current flows from a source to a drain contact. The control voltage is applied to a gate electrode that is separated from the silicon by a very thin oxide layer such that the conductivity of the inversion layer varies with the applied gate voltage. Since the gate current is only required to charge the gate capacitance, power amplification results.

Both bipolar and field-effect transistors have been applied in ICs but field-effect transistors are, by far, the dominant technology today. This is because of the relative ease of making complimentary n– and p-channel field effect transistors that together, enable the very low-power switching circuits employed in a majority of today's integrated circuits.

millions-at-a-time in batch processes, and incorporated in a monolithic solid structure. And they are reliable. Interconnections and transistors have failure rates that are not only small but independent of the number of transistors or interconnects on a chip. The ability to add devices and thus functionality without lowering IC reliability has, for over three decades, sustained the growth of the semiconductor industry, opened the doors to greatly increased system complexity, and led to the creation of many new products and industries.

The demonstration of the monolithic integrated circuit by Texas Instruments, the application of the planar process to silicon ICs at Fairchild, and early support of IC development by the U.S. Air Force spurred rapid advances. A significant milestone was the decision to employ ICs in the Minuteman missile in 1962. Two-years later the Minuteman II guidance computer using ICs was successfully flight tested. This demonstrated the inherent benefits of the IC and spurred government and commercial development efforts. In 1961, the first commercial IC's became available. In 1964, 2 million ICs were sold at a total cost of about $40 million. That was the beginning.

INTEGRATED CIRCUITS BECOME AN INDUSTRY (1962-1981)

In the two decades between the invention of the IC and the founding of the SRC, IC

Table 2-3 BACKGROUND INFORMATION - INTEGRATED CIRCUIT FABRICATION

Start with a round flat single crystal wafer of silicon - now typically 6 to 12 inches in diameter

---

Polish and oxidize

Lithographically form patterns of openings in the oxide for diffusion masks, or of conductors

---

Use high temperature diffusion or ion implantation to incorporate impurity atoms though openings into the silicon, forming transistors

---

Deposit metallic electrical contacts to silicon regions through openings in oxide.

Form electrical conductor patterns interconnecting contacts and bonding pads to form circuits

---

Separate wafer into individual chips, each containing a complete circuit

---

Place chip in package, attach wire leads from bonding pads to package, and encapsulate.

Electrical test.

Sell.

capabilities followed the ambitious Moore's Law projections to a degree unforeseen even by Moore. The number of transistors in an integrated circuit are one direct measure of its capabilities. The integrated circuits designed in 1962 were the equivalent of circuits with 20 to 30 individual components. Two years later, the number was 80 and increasing rapidly. Two decades later, in 1982, the year in which the SRC was founded, the IC equivalent component count had reached

Moore's Law states that the number of transistors
in an integrated circuit doubles every 3 years.

into the hundreds of thousands with 32-bit microprocessors, 256k DRAMs, and 200k gate arrays becoming available. And, in 1997, the numbers are in the millions and still increasing.

Time was required to modify the way in which engineers perceived electronic circuit design. In the sixties, designers reflected their experiences with vacuum tubes and transistors where active devices were costly and passive devices cheap. It took almost a decade to recognize that in the integrated circuit, transistors are cheap and passive components like resistors, capacitors, and inductors are too expensive to use. This change in design fundamentals required time to permeate the design community. Artifacts of circuit design from the discrete transistor era persisted for over two decades.

What technological advances enabled increases of over three orders of magnitude in the number of components in an IC in 20 years? The technology didn't change that much. No fundamental discoveries were involved even though ion implantation became an important process for doping silicon with donor and acceptor impurities, several layers of on-chip interconnections became possible, and epitaxial deposition became available. However, much of the processing was very similar to that of the 1960's albeit with smaller dimensions. Photolithography that enabled the smaller geometries was the technology pacesetter. However, the pace was determined as much by integrated circuit design as by technology.

The progression from hand cutting stencil masks and designing circuits one transistor at a time to designing and patterning ICs with hundreds of thousands of transistors required invention. CAD (computer-aided-design) techniques for ICs were developed to manage this complexity. Originally, IC-CAD systems were closely guarded proprietary assets. The companies with the best CAD became market leaders. However, much like fabrication tools, it soon became apparent that

the cost of CAD tool development would have to be shared by the industry to minimize the costs.

After IC manufacturers stopped developing proprietary fabrication equipment and began buying from equipment suppliers, the differences between competing chip manufacturers narrowed to design ingenuity, cost, and marketing. Generic CAD systems acquired from suppliers dedicated to continually upgraded automated design software have reduced the differences between manufacturers even further. Successful competition has become more dependent on management of people and resources with incremental advantages from better usage of fabrication and design tools, and on product design ingenuity.

More important than the advances in the IC are the changes in the life and work of much of the world's population that are now underway because of it. In history, the IC will be ranked beside gunpowder, printing, plows, electricity, telephones, and television for its impacts. The integrated circuit had invaded every household, vehicle, store, hospital, and factory in all but the most undeveloped regions of the world and is rapidly changing almost every aspect of life.

There are many artifacts of the first 20 or so years of the transistor and integrated circuit; point-contact, grown-junction, alloy-junction, and surface barrier transistors, and the variety of RTL, TTL, and similar configurations in early integrated circuits. In the early 1960ies, integrated NAND gates and flip-flops with less than a dozen equivalent components impressed and won the loyalty of system designers long limited by the passive components that had been available. In the early 1980's, at the beginning of the SRC, 64k DRAMS were produced in large numbers and 16-bit microprocessors were available for launching the personal computer industry. MOS and bipolar ICs had equal market shares and CMOS devices had only a small, 10%, share.

Table 2-4 BACKGROUND INFORMATION - INTEGRATED CIRCUIT PRODUCTS

Logic

Microprocessors - Signal Processors - Gate and Logic Arrays - Switches - Adders
Programable Logic Devices - Controllers

Memory

DRAMs - SRAMs - Flash - PROM

Linear

Amplifiers - Voltage Regulators and Controllers - Comparators - Telecom products
D/A and A/D Converters - Line Drivers

In literally thousands of types covering all conceivable applications

Table 2-5 U.S. AND WORLD SEMICONDUCTOR SHIPMENTS (billion $)

Year	US	World	Year	US	World	Year	US	World	Year	US	World
1964	0.8	1.0	1974	3.2	5.2	1984	14.0	26.2	1994	44.2	101.8
1966	1.1	1.6	1976	3.6	6.0	1986	11.4	27.0	1996	*	132.0
1968	1.2	1.7	1978	4.9	8.5	1988	17.3	46.3	1998		125.6
1970	1.5	2.4	1980	8.4	13.9	1990	20.1	50.5	1999		149.0
1972	1.6	2.5	1982	8.0	14.2	1992	25.5	59.8	2000		179**

In 30 years, from 1964 to 1994, shipments increased 100 fold.
* Internationalization made US shipment data less meaningful ** SIA estimate

In the two decades between commercial availability of ICs in 1962 and the founding of the SRC in 1982, these devices became the lynch pin of the industrial universe. Semiconductor shipments in world commerce grew from $1 billion/year in 1964 (mostly diodes and transistors) to $5.2 billion in 1974, $26.2 billion in 1984 (mostly ICs), and $101.8 billion in 1994. In the year 2000, the IC market will be close to $200 B. ICs have led to fundamental changes in the world economy both because of the availability of low-cost computers that reduce the labor content of services and because of fundamental changes in many products. Toys, telephones, automobiles, cash registers, thermostats, ovens, and ATMs reflect these change

Basic to these changes is that their source, the integrated circuit, increased its performance orders of magnitude while maintaining its cost relatively constant.

READY FOR THE SRC, 1981

In 1981, the U.S. semiconductor industry remained clearly in the leadership position with six of the top ten producers. The other four producers in the top ten were Japanese. However, the trends were ominous. A year earlier, Japanese companies had responded to a demand upsurge to capture 42% of the American market for 16K DRAMs and impressed customers with the quality of their chips. (Economist 6/7/1980, p. 79) By the end of 1981, the Japanese share of the new 64K DRAM market was 70%, gained in the face of determined efforts of US companies to preserve U.S. market share.(Fortune 12/14/81, p. 52) In 1981, the DRAM was the technology driver providing the test bed for new generations of semiconductor production equipment. The Japanese success was expected to continue with a continuing erosion of U.S. market share. Buoyed by its protected consumer electronics market, semiconductor production in Japan increased by 24% in 1981

compared to a decrease of 2% in the U.S. (Business Week 12/14/81, p. 53) It was clear that the thirty years

Table 2-6 GROWTH OF INTEGRATED CIRCUIT COMPLEXITY

1965	64	1977	16 k	1989	4 M	*2001*	*1 G**
1968	256	1980	64 k	1992	16 M	*2004*	*4 G**
1971	1 k	1983	256 k	1995	64 M	*2007*	*16 G**
1974	4 k	1986	1 M	1998	256 M	*2010*	*64 G**

* forecast by SIA

of unquestioned US leadership in semiconductors was at stake and, in fact, the 60% market share of U.S. semiconductor manufacturers of the prior year would never be seen again.

In 1981, IBM was both the largest producer and largest purchaser of semiconductors with a strong world-wide presence. It was followed by the open market leaders, TI and Motorola, with the next eight spots shared equally by U.S. and Japanese firms. The challenge to the US industry was to prevent the forecast of a decreasing US-market-share from bottoming out at a level that would sustain neither a viable semiconductor industry nor a viable electronics industry. One response to this challenge is described in the next chapter. In 1981, the concern with the U.S. position in the integrated circuit industry extended beyond the industry itself to those concerned with the economy and national defense. The economists were, as usual, somewhat vague but were beginning to view semiconductors as a key to successful competition. This view was and is still less focused than that of the Defense Department which had a clear opinion. It recognized integrated circuits as a key differentiating technology, an important enabler of a military strategy based on having a technology edge. (In 1996, both the defense and economic leaders in the U.S. have become complacent with respect to technology leadership and, as a result, have focused their attention on other issues.

Table 2-7 TOP TEN OPEN MARKET IC PRODUCERS - 1981

COMPANY	COUNTRY	$M
Texas Instruments	US	1,072
Motorola	US	795
NEC	JAPAN	655
National	US	683
Intel	US	544
Hitachi	JAPAN	420
Toshiba	JAPAN	345
Signetics	US	344
Fairchild	US	375

Table 2-8 SNAPSHOT OF INTEGRATED CIRCUIT HISTORY, 1947 - 1982

1947	Invention of point-contact transistor
1950	Invention of junction transistor
1951	Alloy junction transistor
1958	R&D initiated by Department of Defense/Air Force - objective: to improve reliability of electronic systems
	Jack Kilby fabricates first working IC, a phase shift oscillator
1959	Air Force (USAF) contracts for development of integrated circuits with Texas Instruments (TI) and Westinghouse
1960	USAF-TI production contract
	First IC customer evaluation
	IBM largest single customer of every US semiconductor company
	Second USAF Minuteman production contract
	$0.5 B semiconductor business, ½ government, ½ commercial
1961	USAF/TI conduct first successful IC demonstration
	Fairchild demonstrated first planar integrated circuits
1962	USAF commits to integrated circuits for Minuteman.
	First microelectronics conference - sponsored by DoD and NASA
1963	USAF/TI/Autonetics demonstration of Minuteman computer
	NASA begins integrated circuit development for Apollo
1964	2 million integrated circuits sold for about $40 M
	Flight test of Minuteman computer
1965	First significant IC production - 14% of semiconductor sales
	ECL and PMOS integrated circuits marketed
	Government R&D funding for ICs from 1959 to 1965 totaled about $100 M with Minuteman providing 20%
	800,000 ICs in use, 177 M hours of operation
	Industry R&D estimated to total $1.2 B
1967	IC production reaches $500 M/yr, DoD spends $126 M for ICs
1970	First microprocessor appears, production of TTL, NMOS, & CMOS ICs.
1973	IC production exceeds $1 billion
1974	1958-74, Government semiconductor R&D >$930M, industry $1.2B
1975	4k RAM, microprocessor
	Government share = 22% of $1.75 billion semiconductor market
1976	ICs reach 58% of semiconductor sales
1977	Production -> $3B SIA formed to address market competitiveness
1978	Very High Speed Integrated Circuits (VHSIC) discussions initiated
1980	First 64K DRAM
	World IC production ~ $11 billion (8-US, 2.5-Japan, 0.5-Europe)
	VHSIC begins, Phase 0 program definition, 9 contractors (General Electric, Honeywell, Hughes, IBM, Raytheon, Rockwell, Texas Instruments, ,TRW, Westinghouse)
1981	IC production exceeds $10 billion, IBM largest
	VHSIC Phase I - 1¼ micron ICs, 6 contractors (Honeywell, Hughes, IBM, TI, TRW, Westinghouse)
	Bipolar - Schottky T^2L, I^2L MOS - CMOS, NMOS

	6.5 million U.S. autos built with microprocessors
1982	SRC established

Chapter 3

THE SCENE, 1982

If change is the objective, put your efforts to that end.
If results are the objective, then change must end.

Significant advances occur only when capable leadership becomes involved. In many instances, the difference between success and failure hinges on the words of a few individuals rather than on the consensus of many. On December 16, 1981, the creation of the SRC was announced by the Board Chairman of the SIA, Bob Noyce. The press release is on the next page. Just a few weeks later, 1982 began and before it ended SRC's Articles of Incorporation were filed, the first employees hired, offices opened, and the first research contracts were awarded. Although its conception came earlier, 1982 is recognized as the year in which cooperative semiconductor research was born. This date fits nicely into the five-year sequence shown below. (The sequence led to anticipation of

SIA-1977 ➜ SRC-1982 ➜ SEMATECH-1987 ➜
SIA Roadmap-1992 ➜ Focus Research Centers - 1998

Figure 3-1 TWENTY YEARS OF SEMICONDUCTOR COOPERATION

another 5-year event in 1997. This should have been the establishment of the first SRC Focus Research Centers. These, however, as we will later see, slipped, but by only a year.)

Before Noyce's announcement, there were a series of exploratory discussions on the need for cooperative research, primarily at SIA Board meetings. At the June 10, 1981 meeting, a proposal for a 'Semiconductor Research Cooperative' was presented. Support was strong. The definition shown in Figure 3-2, was used to guide the SIA Board discussions. It was noted that research was the key and that establishment of the SRC was a solution (Later the observation was made that, in the 1981 time period, long-range research was the only form of cooperation that had a chance of

Basic semiconductor research involves scientific study and experimentation directed towards increasing knowledge and understanding in those fields of engineering and physical sciences related to the semiconductor field. It provides fundamental knowledge for the solution of semiconductor technical problems. It also provides part of the base for subsequent exploratory and advanced developments in semiconductor related technologies and of new or improved functional capabilities.

Figure 3-2 DEFINITION OF SEMICONDUCTOR RESEARCH

FOR IMMEDIATE RELEASE
JOINT SEMICONDUCTOR RESEARCH BY INDUSTRY - UNIVERSITIES
IS GOAL OF SEMICONDUCTOR INDUSTRY ASSOCIATION GROUP

Palo Alto, CA--December 16, 1981--A major program to stimulate joint research in advanced semiconductor technology by industry and U.S. universities was announced today by the Semiconductor Industry Association (SIA).

"The Semiconductor Research Cooperative (SRC) has been established by the SIA to encourage increased efforts by manufacturers and universities in long-term semiconductor research, and to add to the supply and quality of degreed professional people," said Robert N. Noyce, SIA chairman and Intel Corporation vice chairman.

"As semiconductor technology becomes more complex with VLSI (very large-scale integration), and more dependent on sophisticated processes, designs, technologies, packing and testing, there is a clear need to channel more funds to research," Noyce said. "We hope that shared-research programs will encourage a broader spectrum of participation and increased research activity."

"Despite its growth, the semiconductor industry still is in its early stages. New developments are coming at a rapid rate. Leadership in semiconductor research will determine market performance in the future. Although semiconductor industry research has been increasing, for a number of reasons total U.S. research in real dollars has been decreasing in the last few years. Cooperative research such as the SRC should help reverse this trend,' continued Noyce
.
Noyce cited such generic science-related fields as electron beam and x-ray technology, new semiconductor processes, materials science and computer-aided design techniques as areas which might qualify as joint research projects.

The SRC is composed of U.S.-based semiconductor manufacturers and both merchant and user firms. Foreign manufacturers are eligible for participation provided that their home nation permits similar access. Its members who participate in the research cooperative will provide funding, equipment and technical staff to universities and research centers to pursue research projects of importance to SRC members.

Erich Bloch, IBM vice president, technical personnel development, has been named chairman of the interim board of directors of the SRC. Bloch said the SRC will concentrate on research projects of from three to 10 years in length that would be difficult for a single manufacturer or university to attempt. Bloch noted that many SIA members had pledged support for the goals of SRC, including merchant semiconductor manufacturers and companies that manufacture and use internally large numbers of semiconductor devices such as computer and instrument firms.

The SRC, which is now operating as a committee, will be established as a subsidiary of the SIA. Other members of the SRC interim board include Gordon Bell, vice president, engineering, Digital Equipment Corp.; Charles C. Harwood, president, Signetics Corp.; William Howard, vice president, Motorola/ Semiconductor Products Sector: Gordon Moore, chairman, Intel Corp.; Robert Price, president, Control Data Corp.; W.J. Sanders, III, president, chairman, and CEO, Advanced Micro Devices, Inc.; and Charles Sporck, president, National Semiconductor Corp.

Membership in the SRC will be available to all qualified semiconductor manufacturers upon incorporation, which is expected early in the first quarter of 1982.

Figure 3-3 SIA PRESS RELEASE ON ESTABLISHMENT OF THE SRC

acceptance.) The gist of this presentation is given in Figure 3-4 as abstracted from an informal record of that meeting. The presentation were successful. Six months later, the SIA Board of Directors made the decision to establish the SRC and Bob Noyce made his announcement.

INFANCY

After Noyce's December announcement, the leaders assigned to creating the SRC did not delay. In the third week of January 1982, the SRC Interim Board of Directors met in Santa Clara. It dealt with the selection of a director for the SRC, fee structure, Articles of Incorporation and By-laws, university relationships, and SRC's research agenda. Nine companies participated in this meeting, six of which would be among the initial members of the SRC; IBM, National, AMD, Intel, Control Data, and Motorola. Two other participants, Signetics and Fairchild, could not join because they were owned by foreign corporations that would not agree to fees based on world-wide corporate sales. The other participant in the founding group, ATT Bell Laboratories, joined the SRC in 1984.

In March, at a second meeting, an SRC Director was proposed, location discussed, a revised

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PROPOSAL FOR ESTABLISHMENT OF
SEMICONDUCTOR RESEARCH COOPERATIVE
"SRC"
SIA MEETING, JUNE 10, 1981

Environment - U.S. semiconductor industry growth potential is high, requires large capital, is facing intense Japanese R&D competition, and needs more and better trained manpower. U.S. technology lead is vanishing.

Purpose and objectives - Maintain U.S. technology leadership by focused and long-term university research that also adds to quantity and quality of professional manpower. Implement with broad cooperative support from industry.

Why the SRC? - Research is critical to growth, innovation, competitiveness, and productivity; and leads to market leadership. Because competition is intensifying, industry must cooperate to obtain critical mass. It must share costs and risks. Other research funding is decreasing.

What is the SRC? - Cooperative activity for upgrading:

1) uncoordinated and struggling efforts of universities, 2) research in materials, processes, tools, design, reliability, 3) semiconductor curricula, and 4) industry interactions.

Cooperative funding of research in processes, tools, materials, design, and reliability. Method for U.S. semiconductor manufacturers, and their suppliers and customers to address common needs. But neither fund or develop end products, foundries, or buildings.

Figure 3-4 SYNOPSIS OF PRESENTATION TO SIA BOARD, JUNE 12, 1981

funding formula proposed, and a well-prepared "Description" of the SRC presented. The SRC was then described as consisting of U.S. corporations whose business is closely tied to semiconductor technology with the principle purpose being cooperation in the support, definition, and guidance of university-conducted basic research. Other expected benefits that were identified included:

- obtaining a clearer understanding of technology directions, opportunities, and problems will result from cooperative planning and provide increased relevancy to the university program,
- creating efforts above the critical thresholds required in certain research areas as a result of the increased resources,
- focusing national attention on industry's dedication to technological progress and thus attracting student and faculty talent to address industry needs,
- conserving resources by reducing unintended redundancy.

Interactions with universities in planning and evaluating research, in obtaining early

knowledge of research results, and in identification of the best students would provide additional advantages to SRC members. In these discussions, it was clearly recognized that university research was openly published and thus available to non-members. The SRC made no attempt to change this. Although obtaining intellectual property protection could delay dissemination, these rights were to be the property of the university*. SRC had no reason to intervene. For SRC members, royalties would be offset by SRC fees so that they, in effect, would have royalty-free licenses for the results. (In the nineties the property rights issue resurfaced as described in Chapter 13).

SRC - The Basic Assumptions

- is compatible with US antitrust law,
- is necessary for industry competitiveness,
- will enable enlightened and threatened industry to fund new research mechanisms, primarily in universities,
- will provide required generic research results, and
- will provide required trained personnel.

Figure 3 - 5 BASIS OF THE SRC PROPOSAL

Although international competition and the decline of industry research were the motivation for the SRC, foreign companies were invited to participate with two conditions; fees would be based on worldwide IC sales as they were for US companies and reciprocal participation rights would be provided to U.S. companies for cooperative research programs in the home country of the foreign member. No foreign company was able to meet these conditions. Within a year SRC bylaws were changed to limit participation to companies headquartered in the U.S. On several occasions in the subsequent fourteen years, the relaxation of these requirements were discussed and rejected. One reason was that US-only membership enabled SRC to work closely with the U.S. government on R&D issues even though the broad foreign interests of the members limited their overt government ties. Another reason was that the competitive advantage for members that would be lost if all the leading semiconductor companies in the world joined the SRC. In 1999, these barriers became less important and the SRC began to welcome participation from companies not based in the U.S.
In 1982, the generic technologies that defined the agenda of the SRC were identified as:

Devices and materials - substrates, 3-d structures, implanters;
Lithography, etching, deposition - resists, sources, CVD, epitaxy;
Packaging - architectures, CAD, layout, testability; and
Manufacturing - process control, monitoring, testing.

Table 3-1 World and U.S. Semiconductor Device Production, 1960 - 2000

Year	US	World	%	year	US	World	%	year	US	World	%
64	0.8	1.0	80	76	3.6	6.0	60	88	17.3	46.3	37
65	0.9	1.3	69	77	3.7	6.6	56	89	18.5	49.7	37
66	1.1	1.6	69	78	4.9	8.5	58	90	20.1	50.5	40
67	1.1	1.6	69	79	6.6	10.7	62	91	21.4	54.6	39
68	1.2	1.7	71	80	8.4	13.9	60	92	25.5	59.8	43
69	1.6	2.3	70	81	7.8	13.4	58	93	33.4	77.3	43
70	1.5	2.4	63	82	8.0	14.2	56	94	44.2	102	43
71	1.4	2.2	64	83	9.7	17.9	54	95	62*	144	43
72	1.6	2.5	64	84	14.0	26.2	53	96	57*	132	43
73	2.7	4.3	63	85	10.6	21.8	49	97	59*	137	43
74	3.2	5.2	62	86	11.4	27.0	42	98	54*	126	43
75	2.9	4.9	59	87	13.6	33.4	41	99	64*	149	43
								00	77*	179**	43

*estimates based on constant share ** SIA estimate

Programmatically, the SRC program was viewed as a $5-7 million program in the first year, doubling in the second year. Subsequent SRC growth would depend on increasing membership or industry growth. Fees were based in 0.1% of sales with a member's maximum fee set at 10% of the SRC budget.

After a wide search, the Chairman of the Interim Board nominated Larry W. Sumney, Director of the Very High Speed Integrated Circuit Program in the Department of Defense, to be director of the SRC. The nomination was accepted and Sumney became the first employee of the SRC on May 1, 1982. He has remained, first as Director and subsequently as president for the entire life of the SRC.

CONCEPTUALIZATION

The SRC is a natural derivative of the development of semiconductor technology in the U.S. The generic technology on which this industry is based was spawned by the Bell Telephone Laboratories in the fifteen years following the invention of the transistor. It gained early strength from a major infusion of funding from the defense department for research in both industrial and university laboratories. The growth of the semiconductor device industry was so rapid that by the late 1960's developments within the industry were outpacing the ancillary research community.

Both Bell Labs and the Department of Defense (DoD) refocused their R&D efforts away from mainstream semiconductor technology rather than trying to keep pace with the continued advancement of the generic silicon technology.

The rapid pace of industry's technology advances also caused academic research to refocus on

longer range, more speculative areas such as compound semiconductors. Both the near-term and long-range needs of the mainstream semiconductor industry were addressed primarily in the laboratories of the companies producing the devices. Both merchant producers and the growing number of captive semiconductor producers were involved. These circumstances had negative impacts. First, the competitive companies were reluctant to share research results that could provide a competitive advantage. This slowed, but did not stop, the diffusion of new results. Second, the research efforts became highly redundant. Each company found it necessary to apply its efforts to very similar topics in order to avoid being left behind in a critical, rapidly developing technology. Gradually, research became increasingly focused on near-term needs with the result that the generic technology for the longer range future was being neglected. Third, and most important, the structure of the industry and the economy resulted in an erosion of the resources available for research, and it was necessary for each company to apply most of these resources to current product development in order to remain competitive.

In late 1981, executives of major U.S. companies that produce and/or use semiconductor products recognized that this erosion of the generic technology base coupled with government financed efforts in other countries constituted an important competitive threat to their industry. Recognizing that a government-based response to this threat was unlikely, they decided to undertake a cooperative industry-initiated response. After considerable discussion, a concept emerged that has became the SRC.

YOUTHFUL VIGOR

With its first full-time employee on board, the June 1982 meeting of the SRC Board of Directors in Denver was busy. The agenda included member recruiting, establishment of the Technical Advisory Board, site selection, organization, budgets, and staffing. Since, in fact, no firm had yet joined the SRC, member recruiting was the most important agenda item. With a fee schedule and a conceptual description of the SRC n in place, the membership drive could commence. Fifty candidates for membership had been identified and would be contacted. Member recruitment has continued as a high priority of the SRC throughout its existence.

The SRC Technical Advisory Board (TAB) was created at this meeting. It was to consist of technical representatives of the membership and was destined to have a very important role in the SRC. So much so that it merits a chapter of its own in this book.

A site selection committee of the Board under the chairmanship of George Scalise of AMD identified and gathered data on six selected candidate sites. After due consideration, the committee recommended the Research Triangle Park (RTP) of North Carolina because of the research environment provided by three strong universities, its strategic location, and the local support that would enable a rapid start. In addition, two prime candidates for the SRC staff were located in the RTP as was the Research Triangle Institute. That organization offered its assistance by making available temporary office space, the services of its personnel and contract offices, its personnel benefits package, and its administrative assistance. All of these were important for a fast startup of the SRC. This recommendation was approved by the interim Board.

Staffing plans, an organizational structure, a research agenda, and schedules were approved so that the SRC could rapidly focus on its research agenda. This was important. The fast start provided credibility that was essential. The subsequent rapid SRC growth was a direct result.

UNIVERSITIES

Those involved in the startup of the SRC knew that a reality check with the universities was necessary. In April of 1982, eleven faculty members from technology oriented universities met at a hotel in Virginia near Dulles Airport in response to a request from Ken Pickar who was then working with Erich Bloch. The meeting focused on how university microelectronic centers might interact with the SRC. Recommendations from this meeting were that the SRC should:

- acquire royalty-free non-exclusive license for intellectual property,
- select center directors with a focus on technology transfer,
- focus on multi-disciplinary programs,
- stress university-industry interactions and communications,
- assist with facilities, services, training, recruiting, and advice, and
- use three-year stepped funding to provide for gradual transitions.

Figure 3-6 is the news release from the University Advisory Committee meeting. A second meeting was held in May at which the newly selected Director of the SRC was introduced. The above recommendations were discussed and additional issues identified. These included the:

- prevention of unplanned duplication in the research program,
- definition of criteria for funding research,
- the necessity for open disclosure of results,
- procedures for monitoring and evaluation of the research, and
- the schedule for program initiation.

It was also recommended that the committee be continued to advise and support the SRC. (The University Advisory Committee remains active in 2000.)

It is no surprise that the university community responded with enthusiasm to the SRC proposal and were eager to move rapidly. They would gain. Important issues were identified, some of which remain with the SRC to the present; intellectual property, research duplication, and performance evaluation were on the table in 1982 and in 1996 as important issues.

The University Advisory Committee to the Semiconductor Research Cooperative (SRC) held its first meeting in Washington, D.C. on April 5, 1982. The SRC was organized by the Semiconductor Industry Association (SIA) in order to support basic research in the semiconductor/VLSI area.

The University participants unanimously applauded the initiative of the SIA in establishing this new support base for research and education. The Committee concluded that an opportunity exists to enhance U.S. capability and competitiveness in the semiconductor and related industries by University-Industry collaboration. A number of policy recommendations will be submitted to the SRC by the Committee regarding the nature and structure of SRC-University interaction.

"Members of the Committee look forward with enthusiasm to the new activities to be sponsored by the SRC" according to Professor Andrew J. Steckl of Rensselaer Polytechnic Institute, Chairman of the Committee. "These programs will increase the effectiveness of American universities in conducting basic research and educating engineers and scientists in microelectronics. This in turn will enhance America's competitive posture in this critical area."

Committee membership included: Charles E. Backus, Arizona State University; Stephen W. Director, Carnegie-Mellon University; Robert M. Hexter, University of Minnesota; David A. Hodges, University of California at Berkeley; George Lewicki, California Institute of Technology; John G. Linvill, Stanford University; M. A. Littlejohn, North Carolina State University; Paul Penfield, Jr., Massachusetts Institute of Technology, Ben G. Streetman, University of Illinois; and Edward D. Wolf, Cornell University. Attending on behalf of SRC was Kenneth A. Pickar of the Thomas Group, Inc.

Figure 3-6 PRESS RELEASE - UNIVERSITY ADVISORY COMMITTEE, 4/1982

METAMORPHOSIS

In September, SRC assumed a tangible form when it opened offices, hired staff, and began development of its research program. The pressure was on to have a research program in place before the end of the year. The initiation of the research program is described in the next chapter.

Production: 2-5 microns, 64-256K DRAM, 200K gates
32-bit microprocessor
Semiconductor Research Corporations founded
World semiconductor market reaches $14.6 B
Japan captures 30% market share

Figure 3-7 SEMICONDUCTOR INDUSTRY STATUS IN 1982

CHAPTER 4

THE START, 1982-1983

An ounce of action outweighs a ton of talk

Often, new organizations experience a period in which the reasons for creating the organization fade as structural and staffing issues are addressed. If not checked, this diversion from the purpose to the amenities can sap the vitality from the organization and presage a short and unproductive life. Once lost, it is difficult to restore the initial fervor.

Those selected to lead the SRC focused on the research program and were not diverted by amenities. Organization trappings would have no purpose if the program objectives were not addressed rapidly. This urgency was exacerbated by the nine months since Noyce's announcement that were used to sign up members, identify a site, and scope the agenda. Thus, when the SRC's first four employees opened the offices in September, 1982 in the Research Triangle Park of North Carolina, the focus was on the research program. The next six months would be critical to the success of cooperative semiconductor research.

Table 4 - 1 1983 SRC DESCRIPTION

The Semiconductor Research Corporation (SRC) is a new organization that is implementing an innovative form of industry-university cooperation in research related to semiconductor devices. The SRC's goals are to plan, promote, coordinate, conduct, and sponsor research that will result in (1) new knowledge of semiconductor materials and phenomena, and of related scientific and engineering subjects that are required for the useful application of semiconductors; (2) the development of new and more efficient design and manufacturing technologies for semiconductor devices; and (3) an increase in the number of scientists and engineers that are proficient in research, development, and manufacture of semiconductor devices. An equally important SRC task is to efficiently communicate the results of its research to its industrial members.

THE TAB

Even before the SRC occupied its new offices, its new Technical Advisory Board (TAB) met, on September 8-9. Twelve companies were represented. Their purpose was to define procedures, strategies, and plans for initiating the research program. The TAB's responsibilities had been defined as "to advise on and oversee the technical program of the Semiconductor Research Corporation" including the:

- selection and awarding of research contracts,
- identification of industry research needs,
- creation and location of research centers, and
- rapid transfer of research results to members.

The initial members of the SRC TAB were strong industry technologists throughly steeped in competition. They did not normally cooperate with their rivals. They preferred directing to advising. But the new full-time SRC staff, experienced in R&D and knowledgeable in semiconductors, knew that they, not the part-time TAB would be responsible for SRC's success or failure. The future hinged on leading the TAB while listening carefully to it. This 'lead and listen' method for managing cooperative research is a key ingredient of success. It has become more difficult to follow as SRC's output has increased in value to the members. There arises a natural tendency for each member's representatives to try to focus more SRC research on his company's special needs rather than on the

Table 4-2 INITIAL TAB MEMBERSHIP

(At September 1982 Meeting in Research Triangle Park)

Dr. C. Neil Berglund	INTEL Corporation
Dr. Robert M. Brill	Harris Corporation
Dr. Robert M. Burger	SRC
Dr. Michael J. Callahan	Monolithic Memories, Inc.
Dr. Billy L. Crowder	IBM Corporation
Dr. James M. Daughton	Honeywell, Inc.
Mr. J. Phillip Downing	Advanced Micro Devices, Inc.
Dr. James Dyer	General Instrument
Dr. Ronald J. Gutmann	National Science Foundation
Dr. L. David Sikes	Motorola, Inc.
Dr. Kenneth Slater	Digital Equipment Corp.
Mr. Lloyd M. Thorndyke	Control Data Corp.
Mr. Andrew Veradi	National Semiconductor Company
Mr. Michael Winbrow	Silicon Systems, Inc.

needs of all members. There are many often discordant voices for the SRC to listen to, ergo, a challenge. The organization of the TAB and its responsibilities were discussed with recognition that shared decision-making between the TAB and SRC management would evolve. This is a key issue in cooperative organizations. It is closely related to another issue - how to prevent the more aggressive TAB members from unbalancing the research program to their company's advantage and, sometimes, to the detriment of the research. To the credit of the TAB, these issues were resolved in this early period and the TAB rapidly became a productive and essential component of the SRC.

RESEARCH INITIATION

The research program dominated the first TAB meeting. Contracts for SRC Centers-of-Excellence at Cornell University for microstructure sciences and the University of California-

Berkeley and Carnegie Mellon University for computer-aided-design were endorsed. The initial request for proposals was discussed and the TAB's participation in the evaluation of responses organized. Programmatic issues were addressed; short versus long-range research, support of universities with existing semiconductor research versus establishment of new programs, large versus small universities, and centers-of-excellence versus small projects. The consensus was to include all of the above but to base selection primarily on merit and potential for high productivity.

The discussion brought out an important insight: university research in spite of its well deserved aura of success is not the primary purpose for which universities exist. Their purpose is to provide an education. Research is largely carried out by inexperienced but very capable part-time and highly motivated students with limited tenures. This dictates that university research be directed to non-urgent needs and that current needs should be met by full-time dedicated researchers. Even in longer range research, there are needs that require attention from teams with longer tenures than graduate students. In these two areas, short-range and big issues, universities do not provide the solution.

In September, after the TAB meeting, SRC issued the Request for Proposals (RFP) shown in Figure 4-1. This was sent to deans of engineering at all universities in the U.S. with a school of engineering. The expectation was that these individuals were in the best position to identify the appropriate faculty and would do so. This proved to be an imperfect process. SRC responded to a number of faculty requests for copies of the RFP at schools to which it had been previously sent but where it did not emerge from the dean's office. In addition to responses to the RFP, unsolicited proposals were received from universities that became aware of the SRC program through the University Advisory Committee. or through industry associates. These included proposals from the three universities already identified for research centers.

By early November, the competitive solicitation resulted in about 166 proposals from 63 universities most, but not all, of which were responsive to the RFP. These proposals were separated by the nature of their content into three areas: 1) microstructure sciences, 2) systems and design, and 3) production and engineering for evaluation by three committees of the TAB. Proposals that were clearly non-responsive were removed from consideration by the SRC staff.

With the approval of is Board Chairman, SRC decided to make a small number of awards prior to the TAB evaluation in order to provide an early start and increased visibility to the SRC program. Thus, in November, three universities proposing research centers; Cornell, Carnegie-

Mellon, and the University of California at Berkeley, and five universities that submitted proposals in response to the RFP were selected and negotiations for research contracts were initiated. These early awards are shown in Table. 4-3. In the first half of 1983 and with TAB evaluation of the 166 responses to the RFP, forty additional contracts were awarded to 26 universities for research. In three of these contracts, 37 proposals from two universities, Rensselaer Polytechnic Institute and MIT, and one university group, the Microelectronics Center of North Carolina, were removed from

SEMICONDUCTOR RESEARCH COOPERATIVE
Request for Proposal 82-1
Innovative Research Related to Silicon VLSI

Introduction

This is the initial Request for Proposal of the Semiconductor Research Cooperative. Subsequent requests are planned and may be different both in scope and in the area of research addressed. Initial awards made as a result of this solicitation will have a one-year period of performance and will not exceed $100,000. Dependent upon the promise exhibited by the specific area of the proposed research, upon performance, and upon the availability of funds, SRC plans to continue and expand the funded research efforts. Multiple awards are contemplated; however, SRC reserves the option of making one or no awards.

Area of Research

This RFP addresses the broad area of silicon VLSI. All areas of research that are relevant to the speed, reliability, yield, cost, producibility, or useful application of silicon VLSI are included with the specific exceptions of lithography and of the design of specific functional VLSI chips. A nonexclusive list of possible research areas included in this solicitation follows: processing, phenomena, devices and device concepts, packaging, interconnections, metallization, silicon and related material systems, design techniques, CAD tools, generic topography and layout, thermal design, surfaces and interfaces, testing, fault detection, failure mechanisms.

Proposal Format

Clear statements of the problems being addressed, the relevant goals of the research, and the research plan for reaching these goals should be included in the proposal. Lengthy proposals should be avoided. Cost proposals should be sufficiently detailed as to fully justify the requested funding. This solicitation is not directed to facility enhancements or acquisitions, thus costs not relating directly to the proposed research should not be requested. Information on the qualifications of the proposed investigators and of the available facilities should be included.

(Note "Cooperative" in the title. This would be replaced by "Corporation" because, in California where the SRC was incorporated, "cooperative" is reserved for agriculture related organizations.)

Figure 4-1 SRC'S FIRST REQUEST-FOR-PROPOSALS

the competitive evaluation to serve as a basis for three well-focused research programs. Except for the early contracts, selection was based on TAB evaluations and budget allocations for the three areas of research with only minor changes by the SRC.

The result is that 80 of the 166 proposals were funded either individually or as part of a program awards. The SRC has consistently attempted to limit the number of rejected proposals in

order to minimize the unproductive labor used in preparing these proposals while maintaining the quality of the results. The forty-eight percent funding rate for proposals in this initial solicitation is good for a well-targeted competition, but high for a solicitation with broadly defined objectives. These initial awards formed the foundation for SRC's research agenda. Continuations of more than half of these research efforts were supported fifteen years later in the 1996 SRC research program. In the thirteen year life of these research efforts, many changes were made. This ability to advance in step with the technology is a primary reason for their longevity.

TABLE 4-3 INITIAL RESEARCH AWARDS - 1982

SRC Center-of-Excellence in Microscience and Technology*
Cornell University (J. Frey and N. MacDonald)

SRC Center-of-Excellence in Computer Aided Design*
University of California, Berkeley (D. Peterson)
Carnegie-Mellon University (S. Director)

Performance Enhancement of VLSI Using Advance Cooling Techniques*
Stanford University (F. Pease)

Transfer of Software Methodology to VLSI Design
University Of North Carolina (F. Brooks)

Low Resistance Ohmic Contacts for VLSI
University of Minnesota (G. Robinson)

Multilevel Interconnections and Reactive Ion Sources
Mississippi State University (T. Wade)

Interactions During Vapor Phase Film Growth*
University of Illinois (J. Greene)

* Continuously supported by SRC through 1996

THE BOARD

During 1983, the Board of Directors of the SRC welcomed 12 new members and addressed a variety of start-up issues. The TAB reorganization into committees that would guide each of the technical areas of the research agenda was approved. An information distribution system for the SRC was adopted. Information Central, as it was originally called, was the first in a series of developments for report and information distribution of research results to SRC members that led to full electronic distribution through the Internet and the World Wide Web in 1996. Information distribution remains a continuing challenge to the SRC. Getting research results into the hands of

those who can use them and getting them to use the results is essential to the SRC and very difficult. The methods used for technology transfer, government participation in the SRC, and measurement of research performance were among the topics addressed by the Board.

At the end of 1983, SRC had 35 members, the budget had grown from $6 million in 1982 to $11.5 million in 1983 and was approved at $15 million for 1984. Technical workshops had already been held on III-V Digital Research Strategy, Deposition Processes, Multilevel Simulation, and Advanced Packaging Strategies. The SRC was well underway. The accelerated pace of the first several years had resulted in the establishment of a research program that was strong and growing. Early in 1983, Business Week had described the SRC as shown in Fig. 4-2.

While the subsequent history of the SRC is discussed in the following chapters, the table below lists some of the highlights in order to give a perspective on the events to come.

"Typifying this new approach is Semiconductor Research Corporation (SRC), which is emerging as the coordinator of the nation's chips research. The not-for-profit company was founded just a year ago by a handful of chipmakers to organize and sponsor basic research. It now includes most of the top tier chipmakers and nearly all leading U.S. computer makers.....SRC will plow $11 million into research this year and about $15 million next year. This may not seem a lot but Erich Bloch, SRC chairman and a vice-president of International Business Machines Corp., notes that it represents a healthy increase in funding. He explains that the National Science Foundation last year anted up $7.5 million for basic research in semiconductor technologies, and all semiconductor companies combined spent only an estimated $20 million to $25 million. "So," says Bloch, "we are adding a significant amount of dollars to the total research effort."

P. 84, Business Week, May 23, 1983

Figure 4-2 A SNAPSHOT OF THE SRC IN 1983

Table 4-4 U. S. INTEGRATED CIRCUITS AND THE SRC, 1983 - 2000

1983
SRC - 24 members, $12M in research - organized into Three. primary thrusts
Microstructure Sciences, Design Sciences, Manufacturing Sciences
First industry technology goals established by SRC

1984
VHSIC, Phase 2, 0.5 micron chips, 3 contractors
(IBM - CMOS, TRW/Moto - CMOS/bipolar, HW/Moto - bipolar)
SRC Information Central and summer study initiated

1985
Reduction in world semiconductor market to $22B from $26B in 1984
Semiconductor trade deficit with Japan approaches $1B with six of top 10 suppliers in Japan
SRC launches ¼ -micron research thrust, $17 M budget, & 43 participating universities
CMOS becomes dominant semiconductor device technology

1986

SRC membership - 35 companies, government participation initiated
Defense Science Board Task Force addresses semiconductor dependency
U.S.- Japan semiconductor trade agreement

1987
Successful SRC initiatives established - SEMATECH and the
National Advisory Committee on Semiconductors (NACS)

1988
Over 200 SRC supported students graduate with >½ joining SRC member companies
First SRC general meeting - TECHCON '88

1989
Semiconductor competitiveness discussions take spotlight

1990
SRC revenue tops $35M and supports >100 research contracts
Half of top semiconductor equipment manufacturers are Japanese
R. Noyce, IC pioneer and SEMATECH CEO dies

1991
NACS sponsored Microtech 2000 Workshop produces first industry-wide roadmap
SRC cited as model for cooperative research

1992
Over thirty key research products of SRC in first decade
First SIA semiconductor technology roadmap workshop held

1993
U.S. regains world semiconductor market leadership

1994
Second SIA workshop and roadmap prepared

1995
IC production exceeds $100 billion

1996
ICs with 0.18 micrometer dimensions reach market
3.5 million transistor logic arrays appear without fanfare
discrete component circuits have become almost passe'
Industry assumes full funding of SEMATECH

1999
SRC opens door for foreign membership

CHAPTER 5

THE AGENDA

Independent researchers tend to address too many topics;
fortunately, few researchers are really independent.

There have been and are many mechanisms for support of research and development (R&D). In the US, support comes primarily from industry and the Federal government. As shown in Table 5-1, R&D support totaled about $79 billion in 1982. Industry funding was 10 percent more than that of the government, but both far exceeded any other source. Industry expenditures were six times greater than those of the government. It could easily be argued that the federally funded R&D Centers should be included in the government expenditure totals. These data are for all R&D.

Table 5-1 1982 R&D FUNDING IN THE U.S.

Sector	Funding Provided ($ billion)	Funding Spent ($ billion)
Federal Government	36.5	9.1
Industry	40.1	58
Universities / colleges	1.7	7.2
Federally funded R&D Centers	0	2.5
Other	1	2.5
Totals	79.3	79.3

Electrical equipment R&D, of which semiconductors are just a part, constituted about 20 percent of the total. R&D in semiconductors, particularly for silicon semiconductors, was a small part of the total. SRC estimated that, in 1982, $69 million was provided to U.S. universities for semiconductor related R&D but that only about 10 percent of this was associated with silicon integrated circuits. About 80 percent of this support was provided by the Federal government and the remainder by industry. Three years later, in 1985, it was estimated that support for silicon related research in universities had increased from about $7 million to $22.5 million/year with over 50 percent coming from the SRC. SRC funding resulted in a fifty percent increase in funding for silicon device research funding from other sources.

It is noted that in that same year, the Very High Speed Integrated Circuit (VHSIC) Program of the Department of Defense was budgeted at over $100 million and was focused on silicon devices. Little of this was directed to university research because of security concerns. Even though VHSIC was focused on defense, from 1980 to 1990, it made important contributions to industrial integrated

circuit technology at a very crucial time for the industry.

In the early years of the SRC, its leveraging effect was very evident large. This resulted when university faculty responded to the increased opportunity for research support in silicon technology and shifted their research direction in response. This resulted in an increase in successful integrated circuit-related proposals directed to research funding sources with broadly defined missions. Leveraging continues to the present, although the larger research base and other changes that have occurred make it less obvious.

In 1982, government support for semiconductors came from a variety of sources including the NSF, DoD (>12 different sources within DoD led by DARPA), DoC (primarily NIST), DoE (including the national laboratories), and state governments. The mechanism is as often a 'grant in support of research' as it is a contract to address a research need.

Industry support of university semiconductor research flows primarily through the SRC although direct grants and contracts from both SRC members and nonmembers are significant.

SRC is not a research grants agency and, in particular, only supports research that addresses its stated goals, however laudable other proposed research may be. At the beginning, some researchers had difficulty adjusting to this goal oriented methodology having become accustomed to the bottoms-up agenda-defining methods of many government agencies. SRC carries out a directed research program in response to the needs of its industry members through research contracts with universities. Unlike many other research funding agencies, the SRC continually monitors and evaluates the research for the purpose of deriving immediate benefits as well as assessing its value. On the infrequent occasions when grants are employed, the expectations do not differ materially from the contracts.

Targeted research in universities requires an understanding of the idiosyncrasies of the university environment. Although universities provide what is, in many ways, an ideal setting for research, that setting can be frustrating for an industry looking for results. This is because university researchers typically believe that they are the best judges of where their research should be directed and value their right to do this. When an organization like the SRC defines goals for the research and tries to coordinate research at different universities, they tend to interpret this as usurping their academic freedom. This is a lesser issue in the pragmatic engineering departments than in the basic sciences.

This academic freedom issue is alleviated by providing university researchers with

background information and obtaining their participation in the decision processes. The SRC research goals have helped focus this participation. However, research tasks must still be allocated among the universities to assure coverage of the needs and to manage redundancy. SRC must, and does, assume responsibility for this. Other factors included in this research management are the quality of research, takeoffs between education and research, and maintaining university research at the cutting edge in a fast-moving technology. These are discussed in the following sections.

In 1982, when the SRC was created, university semiconductor research was focused on computer-aided-design (CAD) and on compound semiconductor devices directed to defense applications. Those were the areas in which funding was available. The SRC was created to broaden the university research agenda to include more of the interests of the mainstream industry. The creation of core research efforts in silicon materials, phenomena, and devices was relatively easy. These subjects were already familiar and were being addressed in the education of engineers. Integrated-circuit-computer-aided-design research had originated in universities (notably UC-Berkeley), was responding to industry needs, and was spreading. On the other hand, university research relating to integrated circuit reliability, packaging, testing, manufacturing, and increasing levels of integration did not exist. SRC set out to change this, and did, while augmenting the important CAD research.

The means by which the SRC has dealt with some of these technology issues in developing its agenda is described in the following sections. It includes, in order, discussions of the resource, quality, students, keeping up, and the technology agenda.

NATURE OF THE RESOURCE

The first priority of a university is education. Dependent on the university, the arts, athletics, extension services, and research may follow. The priority varies. Research may focus on esoteric areas - cosmology, topology, herpetology, or the structure of matter - usually influenced by availability of financial support. In the big picture, the study of semiconductors and their applications is a small part of the university research agenda and, in most instances, attracts equivalent attention from ‘management.’ In the context of the U.S. university community, the dollars spent on semiconductor research are small potatoes. Well over $100 billion is spent on higher education in the U.S. while around $40 million is spent in universities on semiconductor research. 0.04 percent of the budget does not normally attract a lot of attention.

When the SRC started in 1982, the number of graduate students in U.S. universities performing research directly relevant to the silicon semiconductor industry was small. Less than 100. Thus, it is not surprising that one of the first tasks of the SRC was to increase the presence of 'silicon,' and its applications, in university research.

University research environments are marked by diversity; all areas of human knowledge, all levels of expertise, and all levels of quality. In engineering, first class research is performed by loosely supervised graduate students in well-equipped laboratories at one university, while senior faculty perform routine engineering tasks that masquerade as research at another. Similarly, intellectual environments vary widely. Some engineering schools are defining the future while others are trying to understand the past. Focusing the best while upgrading the weak - in semiconductor research directed to industry needs - is the goal of the SRC and its raison d'etre.

Beyond the diverse academic environments, lies a diaphanous management. First, there is little top-down leadership. This may be appropriate for universities and clearly distinguishes their research from that of industry. Direction for university research arises either from 'curiosity' or from the outside, e.g., the SRC. In today's competitive environment it appears that increased priority setting will be mandated by resource limitations. In essence, that is what the SRC does.

Coordination of university research is difficult at all levels; task, contract, program, center, department, or between universities. Individuality is its nature. Shared research facilities help but don't often solve the problem. (The important scientific breakthroughs for which the list of authors of the seminal paper sometimes exceeds the length of the text are the notable exceptions.) The reward system in universities is strongly tuned to individual performance and is difficult to change. Coordination and cooperation seldom appear prominently on the academic 'curricula vitae'.

This academic individuality is suitable for many areas of university research where interdependencies are managed through journal publications. However, modern science and technology are becoming increasingly complex and require a higher degree of coordination as well as continuity beyond that provided by an individual student or faculty member. The clear answer is the creation of high productivity research teams. Reward systems must encourage the existence of these teams if teamwork is to prosper. The SRC has addressed this issue with its research centers and programs, and with the recently initiated 'focus research centers.' Inroads are being made, but success is elusive.

SRC, fortunately, is working primarily with engineering departments in universities where

the emphasis is on useful applications of knowledge. The challenge has been to focus research on the utilitarian objectives of the SRC, the industry needs. In some universities; Stanford, Berkeley, Carnegie-Mellon, and Cornell where the SRC established its initial research centers, this focus was in place. In other cases, research agendas were refocused. In some cases, it was found that the research support of the SRC was insufficient to reorient research agendas to industry needs. This was not a big problem because sufficient numbers of researchers were both able and eager to participate in the new paradigm - research in support of the needs of the US semiconductor industry. Of the 41 universities participating in SRC research in 1985 that are shown in Table 5-2,about two thirds are state-supported universities in which engineering programs are more viable.** SRC supported research at 30 of these 41 universities in 2000. Eleven universities had stopped participating in SRC research while 35 universities entered the program. (Table 5-3). The 1985

Table 5-2 THE 41 SRC PARTICIPATING UNIVERSITIES IN 1985

Arizona, Univ. of	Arizona State Univ.
Auburn University	Brown Univ.*
California at Berkeley, Univ. of	California at Los Angeles, Univ. of
California at Santa Barbara, Univ. of	California Inst. of Technology*
Carnegie-Melon Univ.*	Case Western Reserve Univ.*
Clemson Univ.	Colorado State Univ.
Columbia Univ.*	Cornell Univ.*
Duke Univ.*	Florida, Univ. of
Florida State Univ.	Georgia Institute of Technology
Illinois at Urbana/Champaign, Univ. of	Iowa, Univ. of
The Johns Hopkins Univ.*	Lehigh Univ.
Massachusetts Institute of Technology*	Michigan, Univ. of
Minnesota, Univ. of	Mississippi State Univ.
Nebraska at Lincoln, Univ. of	North Carolina, Univ. of
North Carolina State Univ.	Notre Dame, Univ. of*
The Pennsylvania State Univ.	Purdue Univ.
Rensselaer Polytechnic Institute*	Rochester, Univ. of*
Southern California, Univ. of *	Stanford Univ.*
Texas at Austin, Univ. of	The Texas A&M Univ.
Vermont, Univ. of	Wisconsin, Univ. of
Yale Univ.*	

* Private universities - some of which get some form of continuing state support.

geographical distribution is shown in the Figure 5-1. The sites of the SRC membership are also shown so that the natural coupling is evident. The SRC, and the semiconductor industry of which it is a part, have recognized the strengths and weaknesses of universities and have adapted to them.

**Academic engineering departments are expensive. They require financial resources beyond the reach of most private universities. Thus, the majority of engineering schools are in state universities

The success of the research program has demonstrated that the strengths far outweigh the weaknesses. It is also clear that university research, as it is now configured, does not meet all research needs of the industry. It is limited both by the nature of the productive workers, graduate students with little prior experience and short tenures, and by the rapid growth in complexity of the industry products; integrated circuits now include multimillion transistor microprocessors, 16-megabit memories, and complex controllers. Universities are poorly equipped to deal with this level of complexity. The industry needs, and the SRC continues to seek, new institutional patterns that reduce these limitations while preserving the valuable university advantages.

QUALITY OF RESEARCH

How does one measure the quality of research? By its nature, research is exploration of the unexplored, a process for which no real measures of quality exist. Failure to achieve a given

Table 5-3 UNIVERSITIES JOINING SRC RESEARCH PROGRAM, 1985 - 2000

Albany-SUNY, Univ.of	Boston Univ.
British Columbia, Univ. of	California, Davis, Univ. of
California, Irvine, Univ. of	California, San Diego, Univ. of
California, Santa Cruz, Univ. of	Central Florida, Univ. of
Cincinnati, Univ. of	Clarkson Univ.
Colorado at Boulder, Univ. of	Dartmouth Umiv.
Duquesne University*	Hawaii, Univ. of
Massachusetts, Univ. of	Maryland, Univ. of
New Hampshire, Univ. of	New Mexico, Univ. of
New Jersey Institute of Technology	Northwestern University*
North Texas, Univ. of	Ohio State Univ.
Oregon State Univ.	Pennsylvania, Univ. of
Polytechnic Univ.	Portland State Univ.
Princeton University*	Rochester Institute of Technology
Rutgers University	Southern Methodist Univ.
Stoney Brook, SUNY	Tennessee, Univ. of
Texas Institute of Technology	Texas, Dallas, Univ. of
Toronto, Univ. of	Utah, Univ. of
Vanderbilt University*	Virginia Institute of Technology
Washington, Univ. of	Washington (St Louis), Univ. of
Wayne State Univ.	

* Private universities (3 of 22)

objective can have as much or more value than a success, but seldom attracts recognition. Usually, quality is identified through the eyes of peers whose reviews are based upon originality, thoroughness, correctness, and depth. SRC accepts these criteria but adds relevance. as one of its over riding measures. It argues that relevance, though spurned by some purists, is an

attribute that does not detract from, but rather adds to the quality of the research. In fact, originality and depth are much more difficult to achieve with relevance than without.

A compilation of SRC results at the end of its first decade is shown in Table 5-4. The specific results illustrate the diversity of the research program but with careful examination show its limitations. It is apparent that many of the results address near-term needs. This is a weakness of SRC's research. The TAB has an awareness of short-term needs and sometimes pushes the SRC to address them in competition with industry efforts that move ahead much faster. There will be successes for university research in this competition but, in the long run, industry will out-distant university efforts and make them appear ineffective. Only by moving out ahead of industry to address future needs will the universities demonstrate their strengths and define an appropriate role. The 'quality' measure employed in some government research support is the peer-review associated with refereed publications. This practice equates the length of the publication list to high productivity. For the SRC's industry research, publications are a good dissemination mechanism but the quality of the research is measured more accurately by its usefulness than by publications.

On the other hand, measuring quality continues to challenge the SRC because of the pragmatism of industry participants in research reviews. To the reviewers, quality often correlates

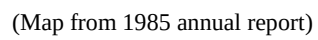

Figure 5-1 LOCATION OF SRC MEMBERS AND ASSOCIATED UNIVERSITIES

Table 5-4 SRC RESEARCH RESULTS CITED IN 1992

GENERAL	
model for cooperative research	joint industry technology planning
university-industry partnerships	silicon research in universities
relevantly educated new-hires	applicable research results
working technology transfer	intellectual property
education/curriculum improvements	a research community
SPECIFIC	
lateral overgrowth epitaxial transistor	hot-carrier suppressed MOSFETs
oxynitride gate dielectrics	ion implantation models
2-d aerial image simulator	yield-defect models
gas purification/filtration techniques	chemometrics for thin dielectrics
scatterometry to measure resist exposure	x-ray lithography models
thermal imaging, microflow, gas sensors	nature of oxide & interface traps
asymptotic waveform estimation simulator	integrated pressure gauge
particle deposition in liquids	plasma resistant photoresist
VLSI reliability simulation/modeling	new fault detection technique
accelerated ion doping	cobalt silicide technology
rapid interconnect circuit evaluator	mixed mode simulator
hot-carrier/oxide reliability simulator	CVD copper process
test generation & fault simulation	1/4 µ MOSFET transistor model
logic synthesis system	system architect's workbench
plasma processing	packaging design tools

directly with near-term utility. This pushes the research toward the very short-range - overlapping with development. Using the research program to fill gaps in development decreases the flow of innovations and new knowledge from research, i.e., it sacrifices the future for the present and detracts from the value of the effort.

EDUCATION VERSUS RESEARCH

Some companies joined the SRC primarily because of their interest in improving the supply and quality of the students who would become their future employees. The microelectronics industry was growing rapidly and its manpower requirements were increasing. Finding the engineers required for this growth was difficult, and often entailed expensive in-house training of new hires. It was planned that the SRC, by involving large numbers of students in relevant research, would ease this manpower situation. These same companies saw little potential in university research providing results that would add to those of their existing R&D activities. In that view, the primary objective of the research was to provide a relevant research experience for the students. Assuring an adequate supply of well-qualified students in integrated circuit technologies continues as an important purpose of the SRC. When, an oversupply of graduates occurred in the early nineties, several member companies recognized the superior qualifications of students who participated in

SRC research by limiting their recruiting to these students. SRC also responded to the oversupply by formulating a mechanism for students to participate as post-docs in SRC supported research. This oversupply was short-lived and a healthy competition for 'SRC graduates' quickly reappeared.

The number of member companies who discounted the value of SRC research results dwindled over the years. This was evidenced by increased participation in the Technical Advisory Board and in technology transfer activities of the SRC. Examination of the SRC research agenda usually convinces even the larger companies that cooperative research is essential for meeting technology needs. Cooperatively, research coverage is more comprehensive and thorough. A snapshot of the research program in 1985 is shown in Table 5-5. In today's competitive environment, no one company can bear the cost of a comparable research program by itself. In universities, the average annual cost per research task was less than $78,000 in 1985. SRC's research budget in that year was about $14.7 million.

The cost of the research would be irrelevant if it were of poor quality. It is not.

THE CHALLENGE - KEEPING UP

Those who participate in university research are challenged by the rapid pace of the microelectronics industry. Since Gordon Moore of Intel stated his law, every company seems challenged to beat the 'doubling every three years pace,' and since the SIA issued its 'Roadmap', the drive is to exceed its expectations. At this pace, universities with their part-time researchers who try to compete with current integrated circuit fabrication technology will forever lag the industry. The challenge is to define the role of the universities and to perform it well.

SRC's initial research agenda was defined by the response of the universities to the RFP. Proposal selection was not based entirely on merit but included allocation of resources among the various defined needs. This allocation was initially determined in the first 1982 TAB meeting as shown in Table 5-6. These research priorities were retained for a remarkably long time. The 1984 program structure in Table 5-7 provided only a few word changes and some fleshing out of the research agenda. From 1984 to 1992, the structure remained largely the same although the subheadings revealed changing priorities. During this period, 'manufacturing sciences' was divided into 'manufacturing systems' and 'manufacturing processes' in recognition of the distinctly different personnel addressing these technologies in the industry. I n 1992, 'packaging' was split off as a science area to reflect its increasing importance.

After 13 years, in 1995, the SRC research program was restructured to conform to the SIA

Table 5-5 TASK COMPOSITION OF SRC 1985 RESEARCH AGENDA

Research Area	# of Tasks	
DESIGN SCIENCES		75
Synthesis	8	
Simulation and modeling	13	
Verification	3	
Testing and Theory	11	
Design Environment	6	
Layout and Design Systems	15	
Design Aids and Methods	5	
CAM/IC Processing	6	
Graphics	4	
Reliable VLSI Systems	4	
MICROSTRUCTURE SCIENCES		82
Microscience and technology	24	
Advanced Beam Systems	9	
Novel Processing Technologies	9	
GaAs Digital IC Research	8	
Advanced Bipolar IC Technologies	9	
Materials and Phenomena	4	
Device Structures and Behavior	6	
Interconnections and Contacts	6	
Processes	7	
MANUFACTURING SCIENCES		30
Manufacturing Science & Technology for VLSI	7	
IC manufacturing Technology	7	
Automated Semiconductor Manufacturing	6	
VLSI Reliability	4	
VLSI Packaging and Interconnection	6	
Total number of research tasks		187

Table 5-6 SRC RESEARCH PROGRAM STRUCTURE IN 1982

Microstructures: Materials, Phenomena, and Fabrication
CAD, Design, and Packaging
Manufacturing, Packaging, and Reliability*

(*originally 'Production and Engineering')

'technology roadman.' This structure is shown in Table 5-7. Even these changes were more cosmetic than substantive. In any case, the roadmap-based-technology structure reflects short-term industry needs rather than long-range research. It does provide an excellent basis for long-term research that is directed to the knowledge needed for future industry products and processes. This

includes both addressing the challenges of continuing integrated circuit advances to the end of the 'shrink' and defining alternative paths on which technology can advance beyond that point, the paradigm shift.

With U.S. industry spending on its development efforts about 200 times as much it spends on the entire SRC research program, the challenge to the SRC and the university research community is to keep tuned to the rapidly advancing technology so as to assure relevance to industry product and process development but far enough ahead so as not to compete with industry developments. To date, the response to this challenge has been successful. SRC research results are well received.

SEMICONDUCTOR RESEARCH ENVIRONMENT

The three main components of SRC's research program have had distinctly different technology environments. Microstructure Sciences addresses materials, devices, and phenomena and, better than either of the other research areas provides university researchers with a research agenda with which they are familiar. At the same time, this area of SRC research is most challenged by industry advances. Researchers in the four research areas that are derivatives of Microstructure Sciences are threatened by the tendency to explain past technology advances rather than identify those of the future.

In contrast, Design Sciences research is relatively new to the university. It is a creature of the increasing complexity of integration. In the first several decades of the integrated circuit, design did not require a new discipline. When the number of transistors on a chip increased into the hundreds, it became obvious that increasingly sophisticated design aids would be required. The engineering time and cost required for manual design was rapidly getting out of control. The $100/gate design cost for an integrated circuit (Robinson,A.L.; "Giant Corporations from Tiny Chips Grow"; Science 208,480-484 2 May 1980) was too much as ICs with 10,000 to over a million gates were being developed. The insight that would respond to this challenge first surfaced at the University of California at Berkeley in the 1970ties and, largely through Berkeley graduates, spread to other universities. The product is integrated circuit computer-aided-design or IC-CAD and is a major focus of SRC research. Even though the products of this research are near-term, the university research community has been a significant participant for over two decades. Only now, as the technology matures is the industry taking the lead.

The response of the universities to the relatively immediate IC-CAD needs has diverted both support and interest from the longer term issues associated with system design. The SRC has

Table 5-7 RESEARCH PROGRAM STRUCTURE

1984	1992
Microstructure Science	
- silicon materials, phenomena, and device physics - microscience - device fabrication	- advanced devices - multilevel interconnect - advanced technology - Technology CAD
Design Sciences	
- design automation - system component interactions - design techniques - test and testability - design verification	- design environment - system level design - physical design - design synthesis
Manufacturing Sciences - reliability, quality assurance and testing - packaging - manufacturing	Manufacturing Process Sciences(89) - reliability -plasma etch -metrology -contamination control -deposition -lithography
Manufacturing System Sciences(1989) - factory automation/management - rapid yield learning - automation/process control	Packaging Sciences(1992)

recognized the need for research dealing with system architecture, partitioning, physical design, testing and repair, and design verification, but its response has been limited by both the availability of resources and the low level of university interest.

SRC's third area of research; Manufacturing Sciences, was focused on the compelling industry need to respond to the fab line proficiency of the industry's Japanese competitors. In 1982, there was no university research in this area and it was difficult to identify potential contributions of the universities. Industry R&D related to manufacturing was confined to a few large corporations. In

Table 5-8 1995 RESEARCH PROGRAM STRUCTURE

Microstructure Sciences	
	Process Integration and Device Sciences
	Lithography Sciences
	Materials and Bulk Process Sciences
	Interconnect Sciences
Design Sciences	
	Design Sciences
Manufacturing Sciences	
	Factory Sciences
	Packaging Sciences

addressing this need, SRC emphasized its 'intellectual content' by firmly including 'sciences' in its title and seeking to address the increasingly complex aspects of controlling, integrating, monitoring, and optimizing IC fabrication processes as they advanced from art to science. While 'Manufacturing Sciences' is defined by the methods, machines and processes employed in IC fabrication facilities, strict application of this definition would have resulted in no research contract awards in the initial rounds. Realizing this, SRC expanded the definition of Manufacturing Sciences to include research in packaging, reliability, and testing which were associated closely with manufacturing and were also important subjects for SRC research. The focus of contracts awarded in the Manufacturing Sciences from the initial solicitation are shown in Table 5-8. They included few that could be classified as manufacturing related research. By 1992, however, Manufacturing Sciences had developed to where when separated into the the new research areas shown in Table 5-7, a substantial research program existed in Factory Sciences.

The research program of the SRC that was set in the 1982-83 time period has been the basis of its subsequent growth. It gathered the significant research resources of the US universities to focus on the needs of the semiconductor industry. Over the subsequent eighteen years this program been constantly improved and reexamined but it has not changed radically. Many of the original research leaders remain as major participants. Their research careers are tied to the SRC program. The changes brought about by the roadmaps have impacted technology developers more than the researchers. The more competitive world of the nineties is causing increased pressure to target research as contrasted with exploration. Such changes represent progress.

TABLE 5-9 INITIAL AGENDA OF MANUFACTURING SCIENCES

CLASS	SUBJECTS OF FUNDED PROPOSALS	
Testing/Analysis	acoustical microscopy	digital SEM
	fault detection	reliability
	testable circuits	E-beam testing
Packaging	ohmic contacts	cooling
	interconnects	package models
	bond interfaces	thermal spraying
Miscellaneous	mask repair	E-beam resists
	adaptive process control	silicides
	thin insulators	

Table 5-10 TECHNOLOGIES COVERED IN 1982 SRC RFP RESPONSE

MICROSTRUCTURE SCIENCES PROPOSALS (84)

Beam Lithography	Bipolar Devices	Capacitors	Carbon Films in VLSI
Carrier Dynamics	Cluster Ions/Beams	Compound FETs	Complimentary MESFETs
Constraints on MOSFETs	Defect Microscopy	Denuded Zones	Dielectric Isolation
Extrinsic Gettering	GaAs ICs/VPE	Ge for VLSI	Heterojunction
Bipolars	Heterostructure.Devices	Interface Defects/States	Ion Beam Processing
Ion Implantation	Lamp Annealing	GaAs - Laser Annealing	Laser Photochemistry
Laser Recrystallization	Lo-T Epi/MOS/SOI/Oxides	MBE	Metallization
Microdevices	Microwave Processors	Modulated Solids	Interconnects
Nitridation	New Transistor	Optical Properties	Oxidation Resistance
Parasitic Models	Plasma CVD/Etch/Reactors	PolySi/Amorphous Films	Polysil Emitters
Polysilicon	Proximity Corrections	Quantizing Effects	Radiation Effects
Shottky Contacts	Si MBE	Silicides	Silicide CVD
Si MESFETs	SiN Gate FETs	Soft Failures	Solid Phase Epitaxy
Stress Models	Stacked CMOS	Surface Effects/Defects	Switching in PolySi
Synchrotron Source	TEM	Thermal Donors	Thermal Nitridation
Thin Film Dielectrics	Thin film Transistor	Thin Insulator	Thin Oxides

SYSTEMS AND DESIGN PROPOSALS (34)

Analog CAD	Architecture	Architecture/Testing	Area Optimization
Arrays	Auto Generated SLAs	Automated Design/Layout	Automatic Algorithms
Bit Map Processor	CAD and CAD Models	Cellular Machines	Custom Architectures
Design Data Management	Fault Tolerance	Integrated Design	Layout
Low Cost Workstation	Network Design	Signal Processors	Silicon Compilation
Software Methodology	Speed Dependent VLSI	Splice Enhancements	Symbolic Layout
Testable Processors	Testability	Test Pattern Generation	Timing Simulator
VLSI Technology	Verification & Testing	VLSI Design Tools	Wafer Scale Integration
3-d Simulator			

PRODUCTION AND ENGINEERING (41)

Acoustical Microscopy	Adapt. Process Control	Anisotropic Etch	Bond Interfaces
Ceramic Chip Carriers	Digital SEM	E-Beam Resists	E-Beam Testing
Electromigration	Epoxy Resins	Fault Detection	High Pressure Oxide
Image Extraction	In Situ FAB	Interconnects	Ion Etched Surfaces
Laser Redundancy	Mask Repair	Metallization Failures	Metal-Ceramic Packaging
Microprofiling	Mobile Ions	Ohmic Contacts	Package Mechanics
Package Models	Production Scheduling	Production Testing	Polymers in Packages
RBS	Reliability	Resistors	Silicides
Solders	Synchrotron Analysis	Testing - Testability	Test Structures
Thermal Management	Thermal Spraying	Thin Insulators	

Table 5-11 SNAPSHOT OF SRC HISTORY

1982	SRC established
1985	Reduction in world semiconductor market to $22B from $26B in 1984 Semiconductor trade imbalance with Japan approaches $1B with six of top 10 suppliers in Japan SRC launches ¼ -micron research thrust, $17M budget, & 43 participating universities CMOS becomes dominant semiconductor device technology
1986	SRC membership - 35 companies, government participation initiated Defense Science Board Task Force addresses semiconductor dependency U.S.- Japan semiconductor trade agreement
1987	Successful SRC initiatives established - SEMATECH and the National Advisory Committee on Semiconductors (NACS)
1988	Over 200 SRC supported students graduate with >½ joining SRC member companies First SRC general meeting - TECHCON '88
1989	Semiconductor competitiveness discussions take spotlight
1990	SRC revenue tops $35M and supports >100 research contracts Half of top semiconductor equipment manufacturers are Japanese R. Noyce, IC pioneer and SEMATECH CEO dies
1991	NACS sponsored Microtech 2000 Workshop produces first industry-wide roadmap**1992** Over thirty key research products of SRC in first decade First SIA semiconductor technology roadmap workshop held SRC cited as model for cooperative research
1993	U.S. regains world semiconductor market leadership
1994	Second SIA workshop and roadmap prepared
1995	IC production exceeds $100 billion
1996	ICs with 0.18 micrometer dimensions reach market 3.5 million transistor logic arrays appear without fanfare Discrete component circuits have become almost passe' Industry assumes full funding of SEMATECH
1997	Anniversaries - SRC 15, Sematech 10 Third NTRS
1998	MARCO initiated 1-billion transistor mainframe announced Roadmap goes international

CHAPTER 6

GOALS, ROADMAPS, and OBJECTIVES

a la Webster's New Collegiate Dictionary:
goal - the end toward which effort is directed
roadmap - not defined
objective - something toward which effort is directed
VIVA LE DIFFERANCE!

Goals focus the energies and efforts of organizations. Not-for-profit organizations relinquish the most important goal of the for-profits, profit, and obtain their direction from less substantive parameters; needs, opportunities, progress, and ideas. It is important to keep these in order, i.e. for the SRC 'needs' is always first. In it's priorities, opportunities, progress, and ideas are only important if they relate to needs.

The technology strategy of the SRC is based upon a planning process derived from participants views of future semiconductor products or production processes, and the technical capabilities required for their achievement. For SRC members, future products are the integrated circuits of the next decade and beyond, and the capabilities are the conception, design, testing, processing, device, patterning, interconnection, materials, packaging, and manufacturing skills required for these products.

The antecedents of SRC's research goals were the individual technology plans of SRC member companies plus some marginally accurate forecasting. One must note their shortcomings. Both plans and forecasts place emphasis on technical barriers as then seen. The end of integrated circuit advances as dictated by lithography or other technology barriers have been described a number of times (c.f. J.T.Wallmark, in Microelectronics, E. Keonjian, Ed. New York: Mcgraw-Hill, 1963, ch. 2). Each such description became an artifact as technology moved rapidly beyond the perceived barrier. However, these forecasts were useful in that they identified formidable goals on which to focus the efforts of the research community which than proceeded to achieve them in short order. Having learned that barriers become goals, the technical challenges described by the SRC provided the first goal-set for the industry while the 'roadmaps' outlined a reasonably detailed set of needs.

Formidable physical barriers will prevent extension of Moore's law beyond the second decade of the next century because of the difficulties in making and operating such small devices. (It is again noted that all past statements of this nature have been wrong.) The crystalline structure of silicon is a diamond cubic lattice in which the edges are a little over 0.5 nm long. Should the present

trends continue, by 2010 the channels of the MOS transistors in integrated circuits would be between 100 and 200 atoms long. At these dimensions, IC performance will begin to degrade due to the spread in the characteristics of the millions of transistors that would be included in the designs. This is assuming that ICs with those dimensions would be affordable. It becomes more apparent with each device generation that the costs of future fabrication tools may provide a practical limit on integration before the limits defined by device physics are reached.

This chapter traces semiconductor technology goal-setting from the inception of the SRC forward to the industry roadmaps now in vogue. Goal-setting is a process and function necessary in applied research and, as is often pointed out, is a process that can both benefit and encumber the research. Benefits accrue when goals focus research on real problems or needs and, in the process, remove unwanted redundancies, while encumbrances result when goals inhibit consideration of viable alternatives.

There is a very close relationship between goals, roadmaps, and needs. Goals provide the objectives for the research while roadmaps describe the expected pathways for their achievement. Goals are a subset of needs modified for consistency with the capabilities of the research performers.

INITIATING THE RESEARCH AGENDA

In its formative period, the mission and objectives of the SRC were stated in a variety of ways in the search for the most effective. A definition from the minutes of the second SRC Interim Board meeting stated the mission of the SRC as "Basic research including scientific study and experimentation directed towards increasing knowledge and understanding in those fields of engineering and physical sciences related to the semiconductor field". Since then, SRC goals have been stated in several forms and with a structural granularity that tends to increase monotonically with each new edition. The descriptions of this goal setting given in this chapter are not meant to be exhaustive but to give the flavor of an activity that is central to cooperative research.

In 1981, after the idea that 'cooperative research is essential for the U.S. semiconductor industry' took hold, it was important to define goals for that research. SRC was not intended to be another NSF with its very broad goals and few milestones. These goals of the SRC were targeted at defined industry needs. They have, over time, extended from the broad and general to the detailed and specific; from the initial half-page outline of goals to those framed in 167 pages of The National Technology Roadmap for Semiconductors (NTRS-199-). In all of these, opportunity is preserved

to venture beyond the well defined pathways and explore new options.

Like artillerymen, those who venture into technology planning are soon made aware of the relationship between range and precision. Short-range targets can be described with great precision, e.g., a building or a bridge, and the targets are usually destroyed. Long-range targets, when defined more broadly, e.g., a city, also can be achieved. Success depends on appropriate definition of targets. Should the long-range target definition become more specific, a specific structure within the city for example, its achievement becomes less likely. Precision weapons with midcourse corrections, although expensive, provide a superior targeting solution with a much high success probability.

A mid-course correction for semiconductor R&D is also very costly. Thus, setting research goals requires careful attention to range, i.e., the time period in which they are intended to be met. By their nature, research goals address a future need and are less specific than development goals.

In microelectronics technology, achieving goals before their targeted time can have one of two results. It can change the time-line and accelerate development, or they can be useless if the customers are not prepared to use them. The latter is more common.

The 1981 goals of the SRC are shown in Table 6-1. In recruiting SRC members in 1981, these goals were buttressed by identifying the major thrusts for the research described in Table 6-2. These thrusts provided a pragmatic tone to the member recruiting effort. Note the absence of key words like integrated circuit and transistor, and of modifiers like fundamental, basic, and long-term in this

list of goals. The perspective for these goals came from industry leaders, many with technical backgrounds but now several levels removed from the technology wars. Their focus was on long-term needs. Their goals defined a research program that could serve the industry well but which

Table 6-1 STATED GOALS OF THE SRC - 1981*

- to carry out basic research including scientific study and experimentation directed towards increasing knowledge and understanding in those fields of engineering and physical sciences related to semiconductors;
- to provide fundamental knowledge for solution of semiconductor technical problems;
- to perform research in key semiconductor technology areas; processes and tools, materials, design techniques/design automation, and failure mechanisms to enhance the reliability and availability of products; and
- to encourage increased efforts by manufacturers and universities in long-term semiconductor research and to add to the supply and quality of degreed professional people.

* Erich Bloch in addressing the SIA Board of Directors on December of 1981.

would do little to solve the practical problems confronting the line managers in the industry who were to constitute SRC's Technical Advisory Board (TAB). These managers needed help in solving current problems and later restated their, and thus the SRC's goals, appropriately.

Table 6-2 ORIGINAL TECHNOLOGY THRUSTS FOR THE SRC

design automation	materials, phenomena, and device physics
device fabrication	ultra high-speed structures
manufacturing	advanced system architectures
reliability	packaging and interfaces

SCOPE OF THE RESEARCH

SRC's research agenda as molded by its members extends from knowledge-creation to problem-solving in the full spectrum of integrated-circuit related technologies with a heavy bias toward highly-relevant but shorter-range problem solving. Translation of this agenda into a productive university research program is accomplished through goal-setting. Making this process work is a triumph of the SRC.

The horizons for SRC research vary from subject area to subject area. In design sciences, for example, results from university research find rapid application in design tools for the industry. In contrast, in the microstructure sciences, results find application in future circuits and processes but often lose association with their origins in the process. This may be because many incremental improvements are made in device, material, and process related technologies and have to be thoroughly tested before being applied to products. This requires considerable time. Most contributions lose any identity with their origins. These are important differences in the application paths for the different technology areas. More on this issue is found in Chapter 14.

Before SRC, academic research usually provided the freedom to pursue truth in whatever direction it might lead. Results were unpredictable. University research tended toward the newest fads - III-V compound semiconductors, magnetic logic devices, or superconductivity - often to avoid direct competition with industry research. This trend was aided and abetted by the incentive of government support that was directed toward needs of military systems that were not being addressed by the commercial industry. At that time, industry research ranged over a range of relevant technologies as companies sought the keys to their future success in the market. In 1960, the integrated circuit had, itself, appeared as a fad.

Goal-setting puts fads in perspective. Judgements applied to possible futures and investments are based on needs and logic. From its inception, SRC with its industry participants has articulated the goals for its research. The National Technology Roadmap for Semiconductors (NTRS) is intended as the quintescent expression of these goals. It now provides the framework for the SRC research program. The attainment of this level of goal-setting requires perseverance not because of the complexity of the goals but more because of the need to educate those involved on the need and on their proper application. But there is another perspective on goals.

Detailed goals can have a negative effect on research. They may define futures that will never be and prevent investigation of latent breakthroughs. The essence of research is exploring the unknown; its results cannot be predefined but must be discovered. They should often surprise. Detailed definition of goals can result in research inappropriate for the SRC. It can constrain results to fit preconceptions. The history of research is replete with costly examples: perpetual motion, oil shale, and dirigibles are examples.

The SRC values goals, but must remain ultra-cautious so as not to preordain solutions. It strives for an appropriate balance. From this perspective, SRC seeks goals that define broad needs in the field of research defined by the silicon integrated circuit. It recognizes that changes will come as technology nodes are encountered but discounts new approaches not integrated or integratible with the ongoing silicon technology mainstream.

STATING THE GOALS

The first annual report of the SRC, for 1983, was distributed in the spring of 1984. In it, SRC stated the broad goal given earlier in this chapter. A specific goal was a scientific and technical data base for future industry development efforts, and in the course of this to:

1. provide a clearer view of limits, directions, opportunities, and problems in semiconductor technology
2. decrease the fragmentation and redundancy in U.S. semiconductor research;
3. establish above-threshold research efforts for critical areas requiring resources beyond the reach of individual companies;
4. enhance the image of the semiconductor industry; and
5. strengthen university-industry ties.

In the same annual report, the technical goals shown on the left side of Table 6-3 were displayed. These were formulated by the TAB for each of the three research program areas that comprised the

1994 program. Most of these goals are modified extrapolations of technology trends. The modifications provided an acceleration of the pace. These goals were independent of the research program that was then in place.

The first twenty SRC research contracts are listed in Table 6-4. These did not reflect the industry's needs or goals. Instead they reflected interests and capabilities of the university research community in 1982 as adapted to integrated circuit needs.

Table 6-3 RESEARCH GOALS OF THE SRC

Early 1984	Late 1984
Microstructure Sciences	By 1994, members will be able to
Integratible high-speed logic elements with state discrimination capability in the 5 - 10 fJ range	• increase complexity 250X(~256 Mb DRAM) • increase performance 10,000X (to 5 X 10^{15} gate-hertz/cm^2), and
Compatible interconnection technology • mixed technologies • low-Z conductors • low-Z contacts • wafer-scale integration	• decrease cost/functional element 500X as compared to 1984 levels; while • maintaining chip reliability of no more the capability to fabricate chips with . - 2 X 10^7 transistors/cm^2
High density DRAMs	• 50 picoseconds logic-gate delay
Logic chips with >10^6 gate equivalents	• 5 fJ gate power-delay products, and
Accurate 16 bit A/D and D/A conversion	• 16-bit A-D conversion at 100 MHZ (Processes to provide ¼ µm features, 10 nm thick layers and 4 levels of interconnects with accuracy of 25% of feature size.)*
Field-reconfigurable chip technology	Attain capability to design:
Design Science	• with <6 mm design effort for chips with 2X10^8 transistors while mapping from high-level description to error-free layout, • to allow economic testing to assure < 1 in 10^6 rejects, and with >95 percent fault coverage
Chip functional designs with 10X performance advantages over existing state-of-the-art	• work stations with 100X more computational power. (Design methods to support 10 FITs reliability, architectures to support an FTR of 5X10^{15} gate-hertz/cm^2, 1000 chip systems)*
Chip functional designs with reduced interconnection requirements	
Design capabilities at 10^8 logic element, 10^{11}-bit memory level	
Affordable generic testability methods	
Reconfigurable and/or fault tolerant design methodologies	
Hierarchical design systems that require <6 engineering man-months between system specification and error-free layouts	
Manufacturing Sciences	Attain:
Quality controls that permit production of chips with defect densities <0.25/cm^2	• defect levels of <0.25/cm^2,
Process automation permitting wide product mix from same fabrication lines and a 5X improvement in productivity	• 5X greater productivity with acceptable capital costs, and
Reduction in fabrication line capital costs for a given production level	• 100 W packages with 400 I/Os and port•hertz products of 10^{12} while maintaining current reliability with 250-fold increase in number of devices/chip.
Real-time correlation of process, device, and circuit models in the production environment	(<1 ppm customer-reject level, with reliabilities of <100 FITs without burn-in and <10 FITs with burn-in)*
Cost-effective package technologies that extend to: • 100 W dissipation • High-speed interfaces • Optical input/output • 400 ports	
Product quality and improvement in chip reliability of 2X without burn-in	
Materials and controls that eliminate yield degradation due to material variables	
Metrology techniques and accuracies that support other manufacturing sciences goals	

* Additions in 1985

Table 6-4 INITIAL SRC RESEARCH PORTFOLIO

TITLE	P.I.	UNIV.
Microscience and Technology	J. Frey	Cornell
Performance Enhancement Using Cooling	R. Pease	Stanford
Transfer of Software Methodology to VLSI Design	F. Brooks	UNC
Low Resistance Ohmic Contacts	G. Robinson	MN
Multilevel Interconnection & Reactive Ion Sources	T. Wade	Miss. St.
Vapor Phase Film Growth	J. Greene	Ill.
Center for Computer Aided Design	S. Director	CMU
Computer Aided Design	D. Peterson	Berkeley
Heterostructure Semiconductor Devices	M. Lundstrom	Purdue
VLSI Circuit Layout	O. Wing	Columbia
Speed Independent VLSI Circuits	S. Reddy	Iowa
Interactions in VLSI Bond Interfaces	B. Livesy	Ga Tech
Algorithms for Symbolic VLSI Layouts	J. Rosenburg	MCNC
Interconnections/Contacts for Submicron VLSI	K. Saraswat	Stanford
CVD of Refractory Metals and Their Silicides	J. Fordemwalt	Az
Incoherent Light & Laser Annealing	R. Kwor	Notre Dame
Complementary MESFET Devices	J. Plummer	Stanford
Thermal Nitridation of Silicon & Silicon Oxides	R. Tressler	Pa. St.
Polysilicon in IC Processes	D. Greve	CMU
Bipolar Transistor Structures	B. Wilamowski	Az

Neither the SRC staff nor the TAB were satisfied with the initial qualitative goals. They were determined to continued to seek improvements. The results were the quantitative statements given on the right side of Table 6-3. These reflect the difficulty in articulating quantitative technology goals for microelectronics. In particular, this became a recurrent issue in the design sciences research area which tends to state its goals as 'being able to design what the technology can make.' Some goals are qualitative, some relative, and others absolute. Perhaps that is a feature of research goals. However, they can be evaluated from the record. By 1994, a high percentage of the goals had been attained but others remained unmet, even in 1997. These included the 256 Mbit DRAM, mixed technologies, error-free layouts, and optical input/output. That may be the nature of goals. If all are met, than they were not sufficiently challenging.

The ten-year 1994 goals were accepted for the purpose of guiding SRC research and disseminated through contract reviews, the Newsletter, and presentations at technical meetings. Particularly in the early years when many university faculty and students began participating in SRC's research, the existence of the goals and their nature was welcomed. The university community that participated in the SRC found the absence of technical goals associated with their research support made the research more difficult. The surrogate goal of peer-reviewed publication

did not meet this need for recognizing value in their efforts, however, the existence of a community of users for their research results provided this value. The process of replacing the 1994 research goals was started in the 1988 Summer Study by presentation of introductory papers prepared for that purpose and shown in Table 6-5. In the subsequent discussion, the need to transition technology goals from those of the SRC to a more encompassing national microelectronics strategy under the aegis of the National Advisory Committee on Semiconductors was recognized.

In 1989, when the new SRC research goals took shape, they were largely an update of the

Table 6-5 PRESENTATIONS AT 1988 SUMMER STUDY PREPARATORY TO SETTING NEW RESEARCH GOALS FOR THE SRC

"Future Research Agenda, Technical Goals for 2001,"
"Role of the SRC: Corporate Goals for 2001,"
Organizational Aspects for 2001: TAB, SEMATECH, Others,
"Government Participation and Role," and
"Technology Transfer in 2001."

1984 goals as given in Table 6-3 obtained through scaling; finer lines, more transistors/chip, improved design tools, etc. Goals for 2001 were set but before long they would be replaced by the broader goals then emerging.

TECHNOLOGY ROADMAPS - MICRO TECH 2000 (1990 - 1991)

The National Advisory Committee on Semiconductors(NACS) was established by Congress in 1988 (at the suggestion of the SRC) to devise and promulgate a national semiconductor strategy. It consisted of industry leaders and government officials and, among other purposes, was an effort to merge the often divergent efforts of these two camps. The membership is shown in Table.6-6. In April 1991, NACS and the Office of Science and Technology Policy (OSTP) cosponsored he MICRO TECH 2000 Workshop to discuss the challenges involved in creating an aggressive technical roadmap for US semiconductor technology development over the next decade. The goal was for a competitive 0.12 micron semiconductor manufacturing process, to identify the:

1) requirements for achieving it ahead of current projections,
2) critical efforts required for producing engineering samples, and
3) resources required for reaching that goal in the year 2000.

This process would be focused on establishing a capability for building 1 gigabit SRAMs three years

Table 6-6 NATIONAL ADVISORY COMMITTEE ON SEMICONDUCTORS (NACS) MEMBERSHIP (1988-1992)

Dr. Charles E. Adolph	DoD	Dr. Ernest Ambler	DoC
Dr. John A Armstrong*	IBM	Norman R. Augustine*	Martin Marietta
Hon. Frederick Bernthal	NSF	Hon. Erich Bloch	NSF
Hon. D. Allen Bromley	OSTP	Hon. Robert B. Costello	DoD
Dr. James C. Decker	DoE	Hon. Donna R. Fitzpatrick	DoE
Dr. William R. Graham	OSTP	Dr. William Happer	DoE
Dr. Charles M. Herzfeld	DoD	Robert W. Galvin*	Motorola
Dr. Robert O. Hunter, Jr.	DoE	Jerry R. Junkins*	TI
Dr. Alan Marty	DoD	Hon. Walter E. Massey	NSF
James C. Morgan*	Applied Materials	Dr. Gordon E. Moore	Intel
Hon. Thomas J. Murin	DoC	Dr. Ian M. Ross*	AT&T
Charles E. Sporck*	National	James G. Treybig*	Tandem
Dr. Robert M. White	DoC	Dr. Eugene Wong	OSTP

* Full term participants

before current forecasts predicted they would appear. Following a series of planning meetings, approximately ninety experts from semiconductor manufacturers, equipment makers, material suppliers, research institutions, universities, and Federal government agencies participated in the workshop. The Workshop concluded that no fundamental technical obstacles were likely to prevent reaching the stated goal but that a continued rapid pace of semiconductor technology advancement through both evolutionary incremental advances and revolutionary innovations was required. The technology issues that would have to be addressed to achieve that goal were defined in roadmaps for advances in lithography, wafers, metrology, processes and materials, simulation, manufacturing.

To achieve these would require the efforts of hundreds of engineers, however much of this effort could be achieved by better coordination of existing efforts at many companies. The SRC organized and participated in the MICRO TECH 2000 WORKSHOP and in preparation of its report. While the results were not integrated with the R&D agendas of any single organization, they led directly to the evolution of a definitive industry roadmap through the subsequent SIA semiconductor technology workshops.

INDUSTRY ROADMAPS - (1992)

NACS recognizing that it was not in a position to implement the Micro Tech 2000 roadmap asked the Semiconductor Industry Association (SIA) to assume that responsibility. The SIA, in turn, assigned consideration to the Technology Committee of its Board of Directors. This committee,

Table 6-4 TECHNOLOGIES REQUIRING ACCELERATED DEVELOPMENT FOR MICRO TECH 2000

A. LITHOGRAPHY	B. PROCESSING
Mask technology	Micro-contamination
Overlay technology	Process control
Metrology	Process/tool development
Resist, resist technology	Ion implantation
Lithography tools	Chemical vapor deposition
Optical	Physical vapor deposition
X-ray proximity	Pattern transfer (etch)
X-ray projection	Thermal treatment
E-beam direct write	Large diameter wafers
E-beam projection	Integrated process equipment clusters
E-beam proximity	Metrology
Ion beam	
C. SIMULATION	D. DEVICES AND CIRCUITS
Factory models	Interconnection technology
Physical 3-d process models	1 Gb SRAM cell technology
Tool models	Device design
0.12 micron device models	Device technology
Design, layout, and simulation tools for board, module, & chip	Design for test
	Computing frameworks and standards
E. ARCHITECTURE	F. ECONOMICS
High-speed interconnects	Manufacturing education
High-performance packaging	Manufacturing economics
Flat panel displays	Factory/product cost models
	Market simulation

chaired by Dr. Gordon Moore of Intel, after considerable discussion decided that the defining the technology goal in terms of the gigabit SRAM would not be appropriate for many of its members. A technology goal applicable to a broader range of products would be more appropriate. This would require refocusing the roadmap. The Technology Committee asked Bill Howard, an industry consultant, and Bob Burger of the SRC to undertake this revision.

Committees of industry experts were organized to formulate the plans and objectives for a second workshop. The first SIA sponsored semiconductor technology workshop took place in November 1992 with a participation level just under 200. Its results are succinctly displayed in Table 6-5. Entries in the table are by date of production start-up but the values are for each technology generation at maturity. The development roadmap is expressed in terms of technology needs that must be met to achieve the product capabilities identified in the roadmap. The research that supports these capabilities must be accomplished up to ten years prior to the date given in this table. SRC's research in 1997 is directed to and beyond the 20 million gate integrated circuit with 0.1 micron features and six levels of interconnect that operates at 1 gigahertz speeds.

In 1994, a revised roadmap was created with a number of differences in the parameters and

a more complete technology plan. It is organized in ten roadmaps with a Scope-Status-Needs-Potential Solutions-Priorities-Crosscuts format for each. The roadmaps are;

Design & Test	Process Integration, Devices, & Structures
Lithography	Environment, Safety, & Health
Interconnect	Materials & Bulk Processes
Factory Integration	Assembly & Packaging

with cross-cutting technologies identified as;

Materials	Contamination-Free Manufacturing
Metrology	Modeling
Standards	Quality and Reliability.

and set of grand challenges identified as;

Productivity improvement	Complexity Management
Funding	Advanced Technology Programs

The details of these roadmaps are provided in the reports so are not repeated here. A second update of the SIA roadmap was issued in 1997. The roadmaps do not provide detailed direction for research, nor should they. By outlining the expected technology trends for the next fifteen years, the directions to the research community have to be 'provide the knowledge we need to meet these goals.' Equally important is the clear direction to the SRC to use some of its resources to do research off-the-roadmap, but again, with the resources available there are more than enough research challenges. The tendency is to address the more evident needs with exploratory research finding little support.

CONCLUSIONS

The process that began with the creation of the SRC led to increased cooperation in the semiconductor industry, the most important example of which is the 'roadmap'. The roadmap has catalyzed the continued orderly advancement of the integrated circuit. The integrated circuit is, without doubt, the highest impact development of the last half of the 20th century. The enormous costs of its continued development are essentially shared by the roadmap process throughout the world-wide industry creating a paradigm for other industries with escalating challenges. This process may be the most important product of semiconductor industry cooperation.

Table 6- 5 OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

	1992	1995	1998	2001	2004	2007
Feature size (µm)	0.5	0.35	0.25	0.18	0.12	0.10
Gates/chip	300K	800K	2M	5M	10M	20M
Bits/chip						
- DRAM	16M	64M	256M	1G	4G	16G
- SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm^2)	4	3.9	3.8	3.7	3.6	3.5
Chip size (mm^2)						
- logic/µprocessor	250	400	600	800	1000	1250
- DRAM	132	200	320	500	700	1000
Wafer diameter(mm)	200	200	200-400	200-400	200-400	200-400
Defect density(defects/cm^2)	0.1	0.05	0.03	0.01	0.004	0.002
No. of interconnect levels - logic	3	4-5	5	5-6	6	6-7
Maximum power (W/die)						
- high performance	10	15	30	40	40-120	40-200
- portable	3	4	4	4	4	4
Power Supply Voltage (V)						
- desktop	5	3.3	2.2	2.2	1.5	1.5
- portable	3.3	2.2	2.2	1.5	1.5	1.5
No. of I/Os	500	750	1500	2000	3500	5000
Performance (MHz)						
- off chip	60	100	175	250	350	500
- on chip	120	200	350	500	700	1000

CHAPTER 7
THE RESEARCH

Useful research requires rigor and discipline. The designation of an activity as "research" is all too often employed to conceal unproductive and expensive meandering. On the other hand, excessive accountability reduces product value. The 'right' level of research management is a rare jewel.

Semiconductor research attained its most productive level in U.S. corporate laboratories of the pre-competitive fifties and sixties. Even though their advances were rapidly disseminated, more than sufficient value accrued to the benefit of the originators to sustain the efforts. However, in the seventies and eighties, research in these laboratories gradually declined as the new Asian production cartels forced U.S. companies to expend more of their resources on next generation products. The creation of new knowledge that would lead to future products was left to 'others'.

The only others available in the U.S. were universities, government laboratories, and not-for-profit research institutes. The latter are closely aligned with current needs for which they are paid to perform research and thus, not structured for exploratory long-range research. Government laboratories are aligned with missions and thus also oriented toward short-range research. The result is an increasing dependence on universities for long-range research. SRC was established by the semiconductor industry to create and maintain a long-range but relevant research activity in universities. This research was intended to provide results supporting semiconductor industry development of both techniques and products.

Universities have long been recognized for performing innovative research but their involvement in mainstream semiconductor research in the 1980's was not significant before the SRC appeared. The required financial support was not available. Government research programs focused on compound semiconductors and technologies beyond the range of the silicon integrated circuit. In 1982, even though industry and government were investing over $79 billion for R&D (Table 7-1) with $7 billion being invested in university research, only a small portion supported university R&D in engineering and the physical sciences, and an even smaller fraction was used to support semiconductor research relevant to the industry. An early SRC estimate was that, in 1982, support for university research in silicon-device-related research was less than $5 million/year with relatively little coordination or planning. Government funding came through agencies that were primarily interested in specifying the general area of research and letting the publication review procedures determine its quality. 'Relevance' was not relevant in the funding decision processes.

The SRC, as it became an active participant in the academic research community, entered into

research contracts in which the goals were defined - usually with major inputs from the performers - to address as many of the industry's needs as possible. Furthermore, in reviewing research projects, emphasis was placed on attainment of mutually defined goals. It was not possible to impose this degree of accountability on the university research community all at once. It was

Table 7-1 U.S. R&D Funding - 1982 (billions of dollars)

Sources		Performers :	
Federal Government	36	Federal Government	9
Industry	40	Industry	58
Universities	2	Universities	7
Other	1	FFRDC's *	2
		Other	3
Total	79		

* Federally-funded R&D Centers

phased in. Intellectual property issues were not an important issue in the initial stages of SRC's research program. SRC research contracts required that member companies have a royalty-free right to use results of research being funded. This approach was developed in discussions with the SRC University Advisory Committee and, at that time, most universities accepted it. Later, attitudes would change.

As noted in the previous chapter, universities were eager to participate although only a few were well equipped to do so. Those with applicable capabilities had benefitted from industry and government support. This did not deter the SRC from issuing a broad competitive solicitation to initiate the program although, direct sole-source negotiation was employed when there was a clear capability that was appropriate for the research.

. The 1984 research portfolio that resulted from the competition and negotiations is shown in Table 7-2. The remainder of this chapter consists of short descriptions of those research efforts that were created in 1984 and continued through 1994. These research efforts are not precisely defined having never been characterized by a single contract and several times involving changes in the project leadership. They have all been reviewed a dozen times or more by the SRC Technical Advisory Board, changes have often occurred, and the research has advanced. The key distinguishing features are that in these universities, the research team has proven to be productive and capable, has remained as part of the SRC program for over 14 years, and the participants have made important contributions to the SRC not only in their research but in defining SRC's research

agenda. These research programs are identified in bold type in Table 7-3.

First, however, several general parameters of the SRC research program will be described. The 51 research contracts that were in effect in 1984 were distributed among 34 universities. Productivity required focusing the research in those universities with clear capabilities and the required facilities. Opportunities were always provided for smaller efforts that were more exploratory in nature and when these demonstrated value for the SRC community they were continued. The cumulative funding of the major participating universities through 1999 is shown in Table 7-2. Theses have been arbitrarily defined as those with cumulative funding exceeding $16 million. The total funding for these major participants has been over one-half of the approximately $500 million of SRC revenues through 1999. Other universities with continuous funding from 1984 through 1994 include Clemson, Florida, Lehigh, Michigan, Purdue, UCLA, and Yale.

About 2200 students have participated in SRC research and graduated with advanced degrees. In 1990, over 900 students and almost 300 faculty participated in the research at the 65 research institutions with SRC research contracts..

In 1982, the number of dissertations produced by U.S. universities in which 'silicon' was a descriptor was 162. In 1990, it was 470. For the key word 'integrated circuits' the corresponding numbers are 31 and 110. Clearly, this research has had a major impact on this technology in the U.S. and has been a major factor in the competitiveness of the semiconductor industry in this country. The purposes of the SRC have been realized.

Table 7-2 SRC SUPPORT OF SEMICONDUCTOR RESEARCH AT TOP TEN UNIVERSITIES - THROUGH 7/1/95*

1. Univ. of California at Berkeley	$54,400,000
2. Stanford University	42,500,000
3. Carnegie-Mellon University	34,800.000
4. Cornell University	30,200,000
5. Massachusetts Institute of Technology	29,100,000
6. Univ. of Arizona	26,700,000
7. North Carolina State University	24,200,000**
8. Rensselaer Polytechnic Institute	20,300,000
9. Univ. of Texas/ Austin	19,800,000
10. Univ. of Illinois; Urbana-Champaign	16,700,000
Total	$298,700,000

* estimates

** includes 50% of MCNC contract for 1983 - 1989 in which NCSU was the major participant

Table 7-3 RESEARCH PORTFOLIO OF THE SRC IN 1984

MICROSTRUCTURE SCIENCES

Centers and Programs

Cornell - Microscience and Technology
RPI - Beam Technology
MIT - Multilayer Integrated Circuit Technology
UC/Santa Barbara - Digital Gallium Arsenide Research

Materials and Phenomena

Yale - Thin Insulators
Illinois - Interactions During Vapor Phase Growth
Yale - Process Induced Radiation Effects
Stanford - Origin of Interface States

Device Structures and Behavior

Florida - Polysil Emitters
Purdue - Heterostructure Devices
Stanford - Complementary MESFET's
CMU- Polysilicon in IC Processes
Arizona - Bipolar Transistors
Vermont - Low Temperature VLSI
Stanford - Models for GaAs HEMT Devices
Illinois - Reliability Physics

Interconnections and Contacts

Arizona - Silicide CVD
Wisconsin - Silicide Metallization
Colorado St. - Low Resistance Ohmic Contacts
Mississippi St. - Multilevel Interconnections
Stanford - Multilevel Interconnections and Contacts
UCLA - MBE Silicides

Processes

Penn State - Plasma and Reactive Ion Etching
Johns Hopkins - Cluster Ion Beams
Notre Dame - Annealing in Silicon
So. California - Laser Mask Repair
Penn State - Thermal Nitridation
Minnesota - Low Temperature Epitaxy

DESIGN SCIENCES

Centers and Programs

Carnegie-Mellon - Design Automation/CAD Center
UC-Berkeley - Design Center in CAD/IS's
Illinois - Reliable Chip Architectures

Chip and Circuit Design

Arizona - MOS Simulations for CAD
Iowa - Speed Dependent VLSI
Texas A&M - Analog CAD
Brown - Silicon Compilation

Testability, Verification, and Simulation

Carnegie-Mellon - Testable VLSI
Arizona State - Three-dimensional Simulator

Chip Layout

Columbia - VLSI Circuit Layout
Rochester - CAD for Layout

Chip Architecture

South Carolina - Signal Processors

MANUFACTURING SCIENCES

Centers and Programs

Clemson - VLSI Reliability
Arizona - VLSI Packaging & Interconnections
Michigan - Automation in Semiconductor Mfg.
Stanford - Manufacturing Science & Technology
MCNC - IC Manufacturing Technology*

Yield Enhancement

MIT - Defects & Internal Gettering

Analytical Techniques

North Carolina - Digital SEM
Minnesota - Acoustical Microscopy

Packaging

Cornell - Defects in Ceramic Substrates
Georgia Tech - VLSI Bond Interfaces
Stanford - Cooling Techniques

Note: Where university name is in **bold** type, either the research or the researcher, or both, were part of the SRC in 1996.

* The continuation of this research occurred at NCSU which constituted about half of the original project.

CORNELL UNIVERSITY - SRC CENTER FOR MICROSCIENCE AND TECHNOLOGY
- SRC CENTER FOR SILICON-BASED NANOELECTRONICS

N. MacDonald, J. Mayer, J. Ballantyne November 1982 -

The center at Cornell University was the first research contract of the SRC. The original 21 tasks are listed in Table 7-4 and those for 1994 are listed in Table 7-5. Cornell has provided a high quality research program for the SRC focused on understanding and application of current technology but with longer-range tasks always included. Its goal has been to develop the fundamental understanding required for producing silicon-based nanoelectronics in the following thrust areas: advanced devices, multilevel interconnect, advanced technology, technology CAD, and lithography. In 1987 the major thrusts were to 0.25 micron BiCMOS, in-situ processing, gallium arsenide devices, and quantum devices. In 1994, the focus had shifted to 100 nanometer minimum feature devices and circuits, use of germanium in silicon technology, advanced resists electron-beam technology, and copper interconnect technology. The SRC provided about $21 million in support of the Cornell Center of Excellence. A significant factor in the original selection of Cornell was the existence of an NSF supported nanofabrication center that had positioned itself to contribute to submicron device investigations. In 1997, the SRC trend toward task management divided the Center-of-Excellence among several SRC research areas.

Table 7-4 1984 RESEARCH AGENDA - Cornell

Monolithic Optoelectronics for Interchip Communications	Transmission Lines for High Speed VLSI
Technology and Physics of MOS Devices with Ultra-Short Gate Lengths	Multilevel Integrated Circuits
Dual Surface Thin Silicon Devices	Electron Microscopy of Submicron Devices
Damage Induced During Reactive Ion Beam Etching	Defects and Morphology at Interfaces
RIBE and Electromigration of Submicrometer Interconnect Metallization	Metallization, Interconnects and Bonding
Structural Studies of Polyimide Films	Vacuum Low Temperature Oxidation
Materials Deposition and Processing Using Laser Photochemistry	Periodic Submicron Structures
Electron Microscopy of Integrated Circuit Cross-Sections	High Frequency Noise
Physics of Metal-Array-Oxide-Semiconductor Structures	Conduction Noise
High Density Memory Cell Evaluation and Design	Thin Oxide Layers
Heat Development in Thin Films and Its Removal	

Table 7-5 1994 RESEARCH AGENDA - Cornell

N_2O Gate Oxide	Proximity Effects in E-Beam Lithography
High Resolution Resists with High Sensitivities	Block Copolymers for Bilayer Resists
Copper Interconnect Technology	Interconnects, Silicides, and GeSi Alloys
Ultra-High Resolution STEM Analysis	Defect Control in Epitaxial Ge/Si Films
Light Emission from Silicon Nanostructures	2.5 D MOSFETS
Ultra-Small Channel Area MOSFETs	Massively Parallel EB Direct Write Tool
PZT Ferroelectric Films	Laser Assisted Epi of Ge-Si-C Alloys
Si-Ge Surface Chemistry	Elastic Properties of SiO_2
Silicon Based Germanium Alloys: Electronic and Transport Properties	
Computer Simulation of Strain Relaxation in SiGeC	

RENSSELAER POLYTECHNIC INSTITUTE - ADVANCED BEAM SYSTEMS
- NY SCOE: MULTILEVEL METALLIZATION INTERCONNECT SYSTEM

-CENTER FOR ADVANCED INTERCONNECT SCIENCE AND TECHNOLOGY

A. Steckl, S. Murarka, R. Gutmann, and T. Lu

May 1983 -

The Rensselaer Polytechnic Institute (RPI) research program was initiated in May, 1983 with a focus on application of ion and electron beams in VLSI processing.. With the initiation of the Sematech Center of Excellence (SCOE) program in 1989 the emphasis changed to Multilevel Metallization and when SEMATECH funding was phased out in 1996, RPI became an SRC Center of Excellence for Advanced Interconnect Science and Technology with shared funding from the State of New York. Funding, through 1999, has totaled over $19 million. The agendas of these three generations of this research are given below.

Table 7-6 1984 RESEARCH AGENDA - RPI

Proximity Correction for Electron Beam Lithography	Electron-beam Transient Processing
Ion Cluster Beam Deposition	Focused Ion Beam Processes and Sources
Resist Mechanisms in Ion, X-ray, and E-beam Lithography	Mass Separated Ion Cluster Beams
The Role of Nitrogen Ion Implantation in Si Thermal Oxidation	

Table 7-7 1988 RESEARCH AGENDA - RPI

Copper interconnect Technology	Chemical - Mechanical Polishing for Planarization
Interlayer Dielectrics	Process Integration

Table 7-8 1996 RESEARCH AGENDA - RPI

Metallization:	Interlayer dielectrics:
Alternative Doping Strategies for Al	High temperature stability of vapor deposited parylene
Formation of Liners by Diffusion	Synthesis and vapor deposition of polynaphthalenes
Integrated CVD/PVD Liner and Cu CVD Metal (SUNY)	Low-K ILD modeling
Reactor and Gigascale Modeling of Metal CVD	UV-Curable/direct write low cost polymers
Dielectrics and interfaces characterization:	Etching and planarization:
Xerogel films characterization (SUNY)	Via etching / cleaning and characterization (SUNY)
Metrology and materials for low-K dielectrics (Texas)	Al and Cu CMP
Metallization of polymers/metal-polymer bonds (N. Texas)	Scratch-free CMP modeling
Metal / low k interaction and stability	Low-k CMP
Nano-indentation study of surfaces and interfaces	Cu/low-k CMP for gigascale integration
Design and performance prediction / evaluation	Effects of non-ionic surfactants on CMP slurry (Clarkson)
Interconnection for gigascale integration (GaTech)	Post CMP cleaning (Clarkson)
Development of performance estimator	Metrology and reliability testing/evaluation
IC interconnect electrical component extraction	Development of x-ray imaging for thin films
High performance interconnect design	Performance limits/extendability on nanoscale lines(SUNY)
Advanced interconnect schemes:	X-ray and bending beam stress methods (Texas)
Optical interconnect	Stress/electromigration test structures and database (Texas)
Metallization:	Methodology for statistical reliability tests (Texas)
Electroless copper and barriers (Cornell)	Stress voiding/ electromigration in sub-interconnect (Cornell)
Multilevel copper interconnections for ICs (Stanford)	Ultrafast optical pulse testing of thin films and circuits

MASSACHUSETTS INSTITUTE OF TECHNOLOGY	- MULTILAYER INTEGRATED CIRCUIT TECHNOLOGY (1984-86) - NOVEL PROCESSING TECHNOLOGIES (1987-92) - SINGLE WAFER PROCESSING FOR FLEXIBLE IC MFG (1989-99) - MICROSYSTEM TECHNOLOGIES (1992-99)
P. Penfield, R. Rief H. Sawin, D. Antoniadis	June 1983 -

SRC's research at MIT has focused in four broad areas and has been supplemented by the closely related research in the Massachusetts SCOE. As seen in Table 7 - 9, the initial emphasis was on material and process technologies and on extension of device designs into the third dimension. In a few years, the research was broadened to include circuit level design, pattern formation, and A/D converters. When the SEMATECH program was established in the 1988 time period, the Massachusetts SCOE in which MIT was the principle organization, emphasized manufacturing systems and processes while the SRC program continued to focus on advanced processes and devices. An SRC Center-of-Excellence was established at MIT in 1993 with a focus on research on microsystem technologies as shown in Table 7 - 12. SRC support for this research at MIT has been in excess of $23 million.

Table 7-9 1984 RESEARCH AGENDA - MIT

Stacked CMOS devices and architectures	Ultra-thin dielectrics
Liquid phase recrystallization of Si on SiO_2	Plasma assisted CVD
Structural and transport aspects of plasma assisted CVD	Laser induced CVD
Plasma etching of polycides	Graphoepitaxy
Grain growth in ultra-thin films of Si and Ge	Dense-interconnect ceramic packages

Table 7-10 1987 RESEARCH AGENDA - MIT

High-resolution high-speed A/D converter	X-ray lithography
Ultra-thin gate dielectrics	Plasma enhanced CVD
Thin/narrow interconnect & contact technologies	Dry etching
Multilevel interconnects	

Table 7-11 1989 RESEARCH AGENDA - MIT

Equipment modeling and process control	Single wafer low temperature selective epitaxial reactor
Pattern independent dry etching processes	Lithography: generation of known resist profiles
Multiple-process equipment (Northeastern)	3-d modeling of thermal fabrication processes (Boston U.)

Table 7-12 1994 RESEARCH AGENDA - MIT

Silicon wafer bonding for micromachined devices	Microsensor interface electronics
Modeling of microstructures and materials with MEMCAD	SOI buried oxide quality and reliability
SiGe-based HBT for RF Low Noise Amplifier	Anisotropic plasma etching processes
RF bandpass filter using thin film resonator	Microphotonic waveguides and modulators
Silicon light emitter and driver circuit	Extreme submicron SOI MOSFETs for CMOS
Reliable interconnects, vias and contacts	

UNIVERSITY OF	- THEORETICAL AND EXPERIMENTAL INVESTIGATIONS OF THERMAL AND

ILLINOIS ACCELERATED DOPANT/SURFACE INTERACTIONS DURING VAPOR PHASE FILM GROWTH IN VLSI DEVICE FABRICATION
- ACCELERATED-BEAM AND PHOTO-STIMULATED REACTIONS DURING VLSI FILM GROWTH

J. Greene 1983 -

The goal of this research has been to develop a detailed understanding as well as a general model for the prediction and analysis of elemental incorporation probabilities and depth distributions of dopants in vapor-phase-deposited films as a function of experimental parameters such as film material, dopant, film growth temperature, growth rate, and the flux and kinetic energy of dopant species incident at the growing film surface. This research has remained focused on its initial objectives throughout its sixteen year history. The total SRC investment through 1999 has been about $1.6 M.

Table 7-13 1984 RESEARCH AGENDA - Illinois (Greene)

Incorporation probabilities and depth distribution for vapor phase deposited dopants

Table 7-14 1994 RESEARCH AGENDA - Illinois (Greene)

Low temperature processing
Atomic layer epitaxy
Control of microchemistry and microstructure at the atomic level

YALE UNIVERSITY - PROCESS INDUCED RADIATION EFFECTS IN MOS DEVICES
- RF PLASMA ANNEALING THIN GATE OXIDES
- THIN GATE OXIDE AND INTERFACE RELIABILITY

T. P. Ma April 1983 -

This research began with a focus on properties of thin gate oxides as affected by processing, ionizing radiation, hot carriers, and high field and interfacial stresses. Gate dielectric reliability was a concern with scaling and increased levels of integration. Methods for minimization of degradation both through design and processing have been investigated including incorporation of chlorine and fluorine ions in the oxide. The goals were to develop a self-consistent defect generation model incorporating the effects of strain and impurities, to build the a practical guide for minimizing these degradation effects, and to explore promising new gate dielectrics and device structures for future applications. Modified charge pumping, channel resistance, and random telegraph signal (RTS) measurements were employed. A modified charge pumping technique allowed probing of lateral distributions of hot-carrier and radiation induced damage in MOSFETs. Oxide damage was found to be non-uniformly distributed with concentrated damage near the source and drain. Fast RTS in the drain current are a function of the oxide defects close to the $Si-SiO_2$ interface. Alternative gate dielectrics including silicon nitride films formed by jet vapor deposition have been investigated. Through 1999, SRC has provided funding of about $2.6 million for this research..

Table 7-15 1984 RESEARCH AGENDA - Yale

Radiation induced interface traps and interface stress
Radiation induced carrier reduction in the junction space charge region

Table 7-16 1994 RESEARCH AGENDA - Yale

Hot-carrier and radiation effects in MOS devices
Fluorine-enhanced gate oxides
Jet vapor deposition of oxides

PURDUE UNIVERSITY

- PHYSICS AND MODELING OF HETEROSTRUCTURE SUBMICRON SEMICONDUCTOR DEVICES
- SCATTERING MATRIX SIMULATION OF ADVANCED DEVICES

M. Lundstrom and S. Data June 1983 -

For fourteen years, this research has been focused on carrier dynamics in submicron semiconductor devices. The objective has been to improve the device models and understanding, and to provide CAD tool models with increased validity at small dimensions. Phenomena such as velocity overshoot, electric field variations, and non-local transport effects are included. A scattering matrix approach was used that made the calculations tractable and applied successfully to the calculations. Through 1999, SRC has provided over $2 million for this research.

Table 7-17 1984 RESEARCH AGENDA - Purdue

Computer models for heterostructure devices using carrier matrix
Current transport in pn heterojunctions
Monte Carlo simulation of electron transport in inhomogeneous electric fields

Table 7-18 1994 RESEARCH AGENDA - Purdue

One- and two-dimensional scattering matrix simulation
Application to bipolar transistor design
2-dimension full band simulations of model structures

STANFORD UNIVERSITY

- COMPLIMENTARY SILICON MESFETs
- ADVANCED BIPOLAR DEVICES FOR VLSI
- POWER ICs BASED ON SOI TECHNOLOGY

J. Plummer July 1983 -

Research focused on transistors in integrated circuits has been carried out under the direction of Prof. Plummer. Who has also participated extensively in other SRC supported research at Stanford however this series of contracts beginning in 1983 have maintained a separate identity. They contracts have provided over $1 million of support for

research on complimentary metal-gate field effect transistors, low temperature operation of bipolar devices, and integration of digital and analog functions in power integrated circuits.

Table 7-19 1984 RESEARCH AGENDA - Stanford (Plummer)

Complementary MESFET technology
Schottky barrier gate technology for p-channel MESFETs
MESFET device simulation
Sidewall spacer, self-aligned source-drain silicidation

Table 7-20 1994 RESEARCH AGENDA -Stanford (Plummer)

Integration of digital/analog functions on same chip
Modeling and fabrication of DMOS/IGBT devices on SOI substrates
Planar dielectrically isolated device technology on bonded wafer SOI material
BiCMOS power IC technology

UNIVERSITY OF CALIFORNIA AT LOS ANGELES - MBE SILICIDES FOR VLSI APPLICATIONS
- PROPERTIES & DEVICE APPLICATIONS OF SI-BASED SUPERLATTICES

K. Wang June 1983 -

Professor Wang was successful in the original SRC competition and over the subsequent fourteen years has performed innovative research in silicides and superlattices for which the SRC has provided a total of approximately $2.8 million of funding. The focus has been on innovative materials and structures obtained through MBE for application to integrated circuits. Originally, transition metal silicides were investigated for novel device structures with emphasis on those formed epitaxially. Subsequently, germanium-silicon short-period superlattices and quantum well CMOSFETs have been the focus. Photon emission from zone-folded Si-Ge was observed. The goal is to form clusters of interacting devices as a basis of cellular automata. This research has been closely coordinated with that of Nicolet at the California Institute of Technology where the completed structures are analyzed.

Table 7-21 1984 RESEARCH AGENDA - UCLA

Low temperature cleaning of silicon surfaces Contact structures and devices
Growth of laterally uniform $CoSiO_2$ layers on silicon

Table 7-22 1994 RESEARCH AGENDA - UCLA

Coupled delta-doped quantum wells fir bipolar transistor applications
Mobility enhancement in short-period superlattices
Band edge luminescence in zone-folded silicon-germanium
Coulomb blockade devices

CARNEGIE-MELLON UNIVERSITY - CENTER OF EXCELLENCE IN COMPUTER-AIDED-DESIGN

S. Director, R. Rohrer, and R. Rutenbar November 1982 -

The CMU Center of Excellence was initiated in November of 1982. In the ensuing seventeen years, the SRC has invested over $25 M in this research effort. The CMU CAD Center has addressed design methodology, tools, and systems with the focus on translation of performance specifications into circuit designs with the objective of creating a comprehensive design automation environment that enables a 6 man-month design cycle. The approach has been to use high-level behavioral descriptions of chips to generate mask sets. Research has emphasized the behavioral, functional, logic, circuit, layout, and process levels of design. Both digital and analog design issues have been addressed. A major emphasis was subsequently developed in Design for Manufacturing. Thus research was integrated with research in the Pennsylvania SEMATECH Center of Excellence the focus of which was a computer-aided manufacturing system for yield management and rapid yield learning. Many products of the CMU research are found in industry design suites and the graduates are productive members of the design community. The programs and students from this Center have played a major role in the advancement of CAD.

Table 7-23 1984 RESEARCH AGENDA - CMU

Statistically based simulation program merging:	
circuit extraction	statistical process simulation
fast RC delay extractor	mixed circuit-level logic-level simulator
User-machine interface	
Data path synthesis that merges:	
heuristic for data path synthesis	expert system for data-path synthesis
behavioral level simulator	data path optimization
Interchange language to link low-level and high-level design programs	

Table 7-24 1994 RESEARCH AGENDA - CMU

Handling manufacturing constraints in the equation-free analog synthesis style	Low-power signal processing circuits
Design process management for product/process co-design	Automatic analog topology selection
Device-level layout of high-performance analog and digital cells	Equation-free analog circuit synthesis
Substrate-aware thermally-aware mixed signal floor-planning	High-performance digital cells
Simulation of substrate noise-limited performance in mixed-signal VLSI	Storage architecture synthesis
High-level partitioning & hardware/software trade-offs in digital system design	Accurate timing verification
Interfaces between concurrent hardware and software processes	Clock distribution routing
Formal verification based on symbolic trajectory evaluation	Silicon implementation strategy advisor
Extraction of gate-level representations from transistor circuits	Performance based layout
Formal verification applied to hardware/software co-design synthesis	Test strategy advisor
Defect and design error oriented diagnosis of VLSI circuits	Automatic learning for design process
Encapsulation enhancement: Intelligent resource selection	Statistical parameter extraction

UNIVERSITY OF CALIFORNIA AT BERKELEY (UCB) - SRC CENTER OF EXCELLENCE IN CAD/IC

D. Pederson, R. Brayton 1982 -

CAD, computer-aided-design, was first defined at Berkeley before the SRC was established. SRC recognized the importance of this research and provided key support to sustain it beginning in 1982. The objective was to develop improved CAD tools and to extend capabilities for IC design as the complexity of ICs escalated rapidly. The research was very responsive to industry needs. Hundreds of graduate students from Berkeley have carried the results in to the

industry. As is seen in the tables below, the research agenda has changed as the needs have changed. Products like SPICE, BSIM, SIMPL, OCT, and other design software from this research are pervasive in the industry. This research led to the funding of a MARCO Focus Center at Berkeley which brings the total funding provided by the SRC in support of Berkeley's CAD research to over $29 M.

Table 7-25 1984 RESEARCH AGENDA - UCB

Design for testability and test generation	Layout
Graphics - Geometric modeling and rendering	Simulation and modeling
Network reliability and energy consumption	Optimization algorithms
Computer aided manufacturing and robotics	IC design workstations

Table 7-26 1994 RESEARCH AGENDA - UCB

Application-specific parallel system design	Complexity management in formal verification
Formal design verification	Alternating RQ timed automata

Computer-aided design of heterogeneous hardware/software systems
Synthesis of state machines from behavior
Behavioral transformations for the real time DSP applications
A formal model and methodology for hardware/software co-design

UNIVERSITY OF ILLINOIS - RELIABLE CHIP (VLSI) ARCHITECTURES

T. Trick, J. Abraham, J. Patel August 1984 -

This research program has received over $7.2 M in SRC support since 1983. The objective has been to develop tools, methodologies, and concepts that are cost effective for the design of reliable VLSI architectures. Emphasis has been on testability, reliability, and manufacturability consistent with the growth in complexity of VLSI systems. A wide range of design issues from fault simulation and design-for-testability to symbolic design verification and reliability modeling have been addressed. These are summarized in the following tables.

Table 7-27 1984 RESEARCH AGENDA - Illinois

Automatic test generation	Fault Simulation
Design of a pipelined floating-point multiplier	Built-in self-test
MOS fault simulator with waveform information	Hierarchical fault simulator
Multiple instruction stream shared pipeline processor	Switch-level fault simulation
Timing verification	Channel routing algorithms
General routing of multiterminal nets	Network partitioning
Fault tolerance in highly concurrent computing structures	Self-checking checkers
VLSI computing arrays	Global layout techniques
Design rule check and circuit extractor	Fault tolerant systems
VLSI computing arrays	Array layout techniques
Design verification	

Table 7-28 1994 RESEARCH AGENDA - Illinois

Portable parallel algorithms for VLSI CAD	High level test generation

Mixed analog/digital design verification	Design for testability
System level simulation of analog ICs	Fault diagnosis

Modeling simulation and design guidelines for VLSI reliability
Simulation and design for VLSI circuit reliability enhancement

CLEMSON UNIVERSITY - VLSI Reliability Research
J. Lathrop, J. Harrison 1983 -

Reliability requirements for VLSI devices and their complexity has required that integrated circuit reliability research focus on potential failure mechanisms as opposed to testing and burn-in. Clemson focused on identifying and characterizing these mechanisms. Funding exceeded $3.2 M when the research was completed in 1995,

Table 7-29 1984 RESEARCH AGENDA - Clemson

Electrostatic discharge effects
Electromigration effects
Charge injection effects

Table 7-30 1994 RESEARCH AGENDA - Clemson

Oxide wear out/breakdown - charge injection
Early failure CAD tool

UNIVERSITY OF ARIZONA - VLSI PACKAGING AND INTERCONNECTIONS
J. Prince 1983 -

Packaging research was initiated at Arizona after a survey of universities by the SRC Technical Advisory Board and has continued for over sixteen years with an agenda that is virtually unchanged. The agenda, packaging and interconnections, is different from that normally associated with academic research but it has been successfully demonstrated that intellectual challenge can be found in this technology. Over time, this subject area has become among the most important as the complexity of chips and systems has advanced rapidly. The results from Arizona have been in the form of a series of widely applied software tools that have been assimilated rapidly by the industry. The electrical and thermal models have been continually updated to address the new packaging requirements as they have evolved and have been extended from two- to three-dimensions as the technology has evolved. SRC has provided funding of over $7.6 M for this research.

Table 7-31 1984 RESEARCH AGENDA - Arizona

Electrical modeling and simulation - capacitance and inductance
Thermal modeling/simulation of VLSI packages
Electrical and thermal characterization

Table 7-32 1994 RESEARCH AGENDA - Arizona

Electrical modeling and simulation - capacitance and inductance
Thermal-mechanical modeling and characterization
Package design support environment

UNIVERSITY OF MICHIGAN - AUTOMATED SEMICONDUCTOR MANUFACTURING
K. Wise 1984 -

The goal of this research was to improve productivity in VLSI wafer fabrication through automation with a focus on sensing and control in a closed loop environment. The focus has been on pattern transfer at submicron dimensions using reactive ion etching as the process. Advanced sensor development, machine vision, process and equipment modeling, expert systems, and the networking of process and inspection stations into a fully working facility have been included in the research agenda. The program evolved into an SRC research center and was unusual in that two of the research tasks remained the same through over a decade of research although other research tasks were added and completed during the decade. SRC funding has been over $13 million.

Table 7-33 1984 RESEARCH AGENDA - Michigan

Sensors and advanced instrumentation
Semiconductor facilities modeling
Chip failure modes and end-process testing
RIE process and equipment modeling and control
Machine vision

Table 7-34 1985-1993 OTHER RESEARCH TASKS - Michigan

Test techniques and process control
Circuit techniques for end-process testing
In-process test techniques
RIE process modeling
Expert systems
Integration networking and simulation
Expert systems and machine learning
Cell automation and control
Image processing
Optical metrology

Table 7-35 1994 RESEARCH AGENDA - Michigan

Sensors and advanced instrumentation
Laser-based optical metrology
RIE process and equipment modeling and control

STANFORD UNIVERSITY - MANUFACTURING SCIENCE AND TECHNOLOGY FOR VLSI

J. Meindl, K. Saraswat 1984 -

This research was directed to accurate simulation and control of computer-integrated manufacturing of ultra large scale integrated systems through creative application of computer science and software engineering thus obtaining a better understanding of the numerous individual process technologies as well as the important device, circuit, and system limitations. Major efforts have focused on the programmable factory, the virtual factory, a manufacturing automation framework, and the instrumentation, test tools, and methodologies required to support their development. To achieve this objective, the SRC has invested over $12 million in the fifteen years of support.

Table 7-36 1984 RESEARCH AGENDA - Stanford (Mfg S&T)

Factory modeling and management
Manufacturing automation
Manufacturing line simulator
Semiconductor manufacturing equipment modeling
Testing and yield modeling

Table 7-37 1988 RESEARCH AGENDA - Stanford (Mfg S&T)

Factory automation and simulation
Equipment and process modeling
Measurement science
Advanced processes

Table 7-38 1992 RESEARCH AGENDA - Stanford (Mfg S&T)

Manufacturing automation
Virtual factory
Programmable factory

Table 7-39 1994 RESEARCH AGENDA - Stanford (Mfg S&T)

Process synthesis
Semiconductor process representation
SPEEDIE - profile emulator for etching and deposition
Simulation tool integration
Rapid thermal multiprocessor
Acoustic temperature and thickness measurement

NORTH CAROLINA STATE UNIVERSITY

- LOW TEMPERATURE PROCESSING
- AUTOMATED SEMICONDUCTOR MANUFACTURING TECHNOLOGY
- SINGLE WAFER MANUFACTURING/SUBMICRON TECHNOLOGIES

- NORTH CAROLINA SCOE / CLUSTERED PROCESSES

N. Masnari, J. Hauser 1983 -

This research has a unique history in that it actually began as part of an SRC contract with the Microelectronics Center of North Carolina (MCNC) in which NCSU was a key participant. In 1988, in support of a proposal for an NSF Engineering Research Center, the NCSU research was separated from the other components in a separate contract. Initially the focus was on manufacturing technology for one-micron CMOS devices, was subsequently modified to address the enabling technology needs for high-yield low-cost manufacturing of scaled semiconductor devices, and finally was modified to manufacturing issues associated with single-wafer processing for sub-micron devices and clustered processes. In 1994, this research was carried out under two integrated contracts, one as a SEMATECH Center of Excellence (SCOE) and the second as an SRC program. It is estimated that over $20 million has been provided by the SRC for this research. This does not include funding for a number of separate contracts with NCSU that were not directly related to the above.

Table 7-40 1984 RESEARCH AGENDA - NCSU (MCNC)

Transient enhanced diffusion during rapid thermal annealing
Effect of Ge preamorphization on mobility & sheet resistance of implanted Si
Very low temperature anneals
Defect engineering using epitaxial misfit dislocation
Plasma assisted low-temperature oxidation, film formation, and epitaxy
Integration of low-temperature processing into 1 micron CMOS technology

Table 7-41 1989 RESEARCH AGENDA - NCSU

Equipment modeling and computer-aided processing
Manufacturability issues in rapid thermal processing
Manufacturability issues in rapid thermal CVD
Selective metal deposition
Heat transfer in rapid thermal processing

Table 7-42 1994 RESEARCH AGENDA - NCSU SCOE

Integrated processing and device demonstration
Advanced gate dielectrics
Source/drain engineering

Table 7-43 1994 RESEARCH AGENDA - NCSU

Physical and process modeling of RTP systems
Temperature measurements in RTP systems
Contacts to ultra-shallow junctions using rapid thermal processing
Ultra-thin gate dielectrics using rapid thermal processing
Ultra-thin film characterization methodologies

STANFORD UNIVERSITY - PERFORMANCE ENHANCEMENT OF VLSI THROUGH USE OF ADVANCED COOLING TECHNIQUES
- SUBMICRON OPTICAL LITHOGRAPHY

- SYSTEM LEVEL PACKAGING
- MICROMINIATURE THERMAL MANAGEMENT FOR SYSTEM LEVEL PACKAGING
- OPTICAL LITHOGRAPHY

F. Pease 1982 -

Beginning in 1983, a series of SRC research contracts with Prof. Pease as the principal investigator have addressed a variety of packaging, interconnect, and optical lithography related research needs that were notable for their diversity. The lithography research was supported as part of the California SEMATECH Center of Excellence program. The funding for this research has exceeded $3.1 M through 1999.

Table 7-44 1984 RESEARCH AGENDA - Stanford (Pease)

Microchannel heat sink
Microcapillary attachment

Table 7-45 1987 RESEARCH AGENDA - Stanford (Pease)

Close-packed microscopic transmission lines
Transient metal reflow for interconnect
Active interconnect substrates
Microcantilever contacts

Table 7-46 1994 RESEARCH AGENDA - Stanford (Pease)(SCOE)

Mask errors and metrology
Twin-mask structure for increased depth of focus
Overlay and alignment

Table 7-47 1994 RESEARCH AGENDA - Stanford (Pease)

Mechanical properties of thin-film multilayer interconnect structures
Active array probe card
High density, high temperature superconducting interconnects
Pressure microcontacts
Microminiature thermal management for system level packaging

Chapter 8

FINANCES

In cooperative activities
participants who do not either provide or receive money
seldom really participate

Money is one of the best indicators of success, approval, interest, or value. However, its accuracy as an indicator is diminished when there is a disconnect between those who gain value from the product and those who pay for it. In commerce, disconnects are rare because competition forces value and cost to be closely correlated. However, in cooperative organizations value and cost can be poorly connected, resulting in participation being determined by other factors such as:

- management support based on short-range objectives or non-quantitative factors,
- total cost of effective participation (estimated at 2X fees),
- cost allocation methods employed within the member corporation,
- current profitability of the prospective member, and
- ability to obtain and apply external research results.

Such factors provide formidable challenges to cooperative organizations. Obtaining and maintaining participation can consume the available energy of a cooperative.

SRC's membership is primarily motivated by needs for a continuing flow of creative research results and for relevantly educated graduates. However, sometimes the decision-makers in potential members are sufficiently separated from these needs to where the SRC's value is not recognized, or they choose to let others fill the need. Obviously, in SRC's industry members, this problem does not exist.

RETURN ON INVESTMENT

The basic tenet of cooperative research is that the cost of participation is a small fraction of the value of the research results. Ideally the fraction would be the ratio of the company fee to the total income of the cooperative (1/10 for the larger members, as little as 1/300 for associate and affiliate members). In reality, the cost advantage for an SRC member is less, closer to 1/5 for those members who have done the analysis. One reason is that their research priorities are different from those of the SRC. This is partially offset by the relatively low cost of university research but is exacerbated by its part-time second-priority nature. .

The advantages ensuing from cooperative research extend beyond the research products that

are obtained and the leveraging of funds. An improved awareness of technology status and issues, and of a company's relative position is derived from cooperative planning and evaluation of SRC research. This has escalated to a new level in the "The National Technology Roadmap for Semiconductors," a direct product of cooperative planning and needs forecasting that began with the SRC. The 'roadmap' is discussed in Chapter 6.

Cooperative research allows staffs of member companies to become directly involved to where they can sometimes steer the research to issues of specific interest to their companies. This is potentially troublesome in that universities are not equipped to deal with current technology issues effectively and, if they attempt to respond to current problems, their commitment to long-range research is weakened. When company-specific problems are addressed, the results are available to and thus benefit all member organizations.

Member companies also obtain important value from the facilitated access to students involved in SRC research. Most of these students, upon graduation, are hired by the members. The most important benefits of participation are listed in Table 8-1.

TABLE 8-1 BENEFITS OF PARTICIPATION IN COOPERATIVE RESEARCH

Leveraging of research funding, i.e., more 'bang for the buck'
Improving awareness of relative technology status
Gaining advantage from planning and performing cooperative research
Increasing number of relevantly prepared students
Facilitating access to superior students with relevant backgrounds
High quality research results

These benefits provide competitive advantage. Other motivations for joining SRC are associated with broader goals - national security, economic status, quality of life - that are important but less focused. Advantages of SRC membership are diminished by the costs as listed in Table 8-2.

As previously noted, members of the SRC have estimated their real costs to be greater than their fee. The maximum fee paid by any company was limited to 1/10 of a total budget as set by the Board of Directors. The actual cost of participation is nearly twice the fee. Even so, SRC is one of the best investments a company can make. Cooperative research provides sufficient advantages to where fully involved members find it essential to their continued competitiveness in semiconductor markets.

A factor with a potentially important impact on the SRC is related to the rights of members

Table 8-2 COSTS OF PARTICIPATION IN COOPERATIVE RESEARCH

SRC's fee,
Added internal costs of identifying, monitoring, obtaining, and applying research results (estimated to be as large as the fee),
Different technology agendas of the cooperative and the company, and the
Dilution of competitive advantage from sharing of results,

to use the research results that SRC provides at no additional cost. Residual rights are held by the the university where the research is performed, or by its assignees. Several universities have claimed that their research results are dependent on background intellectual property not funded by the SRC and that they cannot separate these. These universities have threatened to refuse SRC research support that requires them to identify background intellectual property which might interfere with members rights to use research results from SRC supported research. This rights issue continues to cause difficulties for the SRC.

FUNDING THE SRC

In the early spring of 1982, the initial SRC Board of Directors established a fee algorithm (the formula for determining a participating company's membership fee) that places the major burden of support upon the semiconductor manufacturers who established the SRC and set its agenda. Although this fee schedule remained virtually the same through 1996, the upper limit or cap has increased.

The 1995 SRC fee schedule is shown in Table 8-3 below. The fact that the maximum fee is almost 50 times the minimum fee recognizes the intent to include as many U.S. semiconductor companies as possible without creating a burden on the operation of the cooperative. Also, the fee was based either on sales or on twice integrated circuit production costs so as to include captive manufacturers on an equitable basis. The fees of integrated circuit users, as well as semiconductor equipment, material, and software suppliers, were the same schedule but applied to 50% of sales.

As a net percentage of company revenues, the fee structure for companies with annual revenues of $25 million is about twice that of companies with annual revenues exceeding $600 million. When these fees were graphed against company revenues, the curve shows a bulge that has inhibited some potential members from joining the SRC. This is shown in Figure 8-1. The fee algorithm required a small company with annual revenues of $25 million to pay a membership fee

Table 8-3 1995 MEMBER FEE SCHEDULE

1. Membership in the SRC is held by the parent corporation on behalf of any subsidiaries.
2. The SRC Full membership fee is related to ICs produced in a silicon fabrication facility either owned or through a contracted service for commercial sale or captive use. It is calculated from the Fee Schedule below. It is based on world-wide sales of integrated circuits, or twice production costs for captive producers. For companies that fab for both sale externally and for captive use, their fee is based on their total fab activity, i.e., external sales plus twice cost of production for internally consumed ICs.
3. The minimum SRC membership fee is $65,000.
4. The maximum SRC membership fee is $3,130,680.
5. Year-to-year variations in a member's fee are limited to 30% unless caused by sale, merger, or acquisition.
6. Fees are payable in quarterly installments at the beginning of each quarter.
7. A company may join any time during the calendar year and pay pro-rated fees on a quarterly basis.
8. In the event membership fees fail to match the requirements of the approved SRC Budget, the Board of Directors may establish a special assessment to cover the shortfall. The assessment will consist of a surcharge levied on the individual member fees and shall be calculated as a fixed-percentage adder.

FEE SCHEDULE

IC Sales and/or twice production costs		Total Fee		
		Base Fee	+	Percent x Amount Over Base Amount
Base Amount	to			
Under $25,000,000		$ 65 K		--
$25,000,000	to $49,999,000	65 K		0.312%
50,000,000	to 99,999,000	143 K		0.208%
100,000,000	to 199,999,000	247 K		0.169%
200,000,000	to 299,999,000	416 K		0.130%
300,000,000	to 399,999,000	546 K		0.104%
400,000,000	to 499,999,000	650 K		0.078%
500,000,000	to 599,999,000	728 K		0.052%

Over $600,000,000 = 0.130% (to the maximum fee of $3,130,680)

that was twice or more the percentage rate of a company with revenues of $1 billion with an anomaly in that the percentage actually rose for revenues between $25 and $50 million. This recognized that some incremental costs to the SRC associated with a member are the same regardless of the size of the company.

SRC income through 1999 is shown in Table 8-4 along with data on the sales of the U.S. semiconductor industry. It is apparent that the cap on the funding algorithm has prevented the SRC budget from growing with the industry, and thus limits the research being performed. This issue is been addressed by the SRC membership. An aggressive interpretation of these data would note that

Figure 8-1 1995 FULL-MEMBER FEE SCHEDULE FOR THE SRC

in less than a decade after its founding, SRC's university research program had reversed the erosion of semiconductor market share of the U.S. industry and provided skilled personnel and research results that enabled a rapid expansion of the U.S. industry. This success was unrecognized as SRC's funding stagnated while the revenues of the industry more than doubled.

Table 8-4 also provides data on government and SEMATECH funding of the SRC as a function of time. In addition to the funding that in 1988 was almost 20 percent of SRC's income, government participation in the SRC has provided a new and useful technology interface between government and industry supported semiconductor research. This has led to increased coordination and a more efficient accommodation by the industry of variable government support. SRC's annual income from the government totaled just over $12 million, averaged about $1.2 million/year, and

was only about 4 percent of SRC's income in a decade of government participation. This would not have been manageable were it not for the fact that in this decade, SRC industry support provided a funding base that allowed the SRC to adjust to the instability of government funding and preserve the continuity of the research programs. Government participation was implemented through a Memorandum of Understanding and a Grant from the National Science Foundation. If it had entailed the burden of Government contractual conditions, it would not have been affordable for the SRC.

Government and the SRC have worked well together but to a limited extent. Coordination has been made more difficult by a number of factors including the;

- changing nature of government (mostly, Department of Defense) participation in semiconductor R&D,
- variability in the level of support provided to the SRC by the government,
- effort required by the SRC to sustain meaningful interactions, and
- complexity of securing and maintaining funding from multiple agencies.

As government participation in semiconductor R&D has decreased, the question is whether the effort required to obtain limited coordination exceeds its benefits. Agencies that do not provide funding, in general, do not participate in the SRC.

Aside from R&D funding, the Government is a consumer of integrated circuits. Its participation in the SRC enables input from the users. Furthermore, government provides the major support for fundamental research that is the knowledge base for SRC's applied research efforts.

Coordinating SRC and government R&D activities is justified by the valuable feedback provided. These benefits accrue only to those government agencies that participate. More effective Government-SRC cooperation could be provided by involving all government agencies that participate in semiconductor R&D, and providing a single point of contact for this participation and for funding. The only point in the government where all semiconductor R&D comes together is the Office of Science and Technology Policy which has only limited influence on the efforts.

Sematech is an outgrowth of the SRC. The SRC recognized the need for semiconductor manufacturing technology R&D and helped define and sell the concept to both the industry and the government. These events are described more fully in Chapter 11. Once created, SEMATECH funded research through the SRC that was critical to its manufacturing technology objectives. This support amounted to thirty one percent of the SRC budget in the six years from 1990 through 1995 at an average level of $11 million/year. When the government participation in SEMATECH ended

in 1996, this research support decreased rapidly. In 1997, it was $400,000. In that year, industry increased its support of the SRC in order to compensate for the loss of Sematech funding. Sematech has continued to share in the support of university research of particular relevance to manufacturing technology.

SUMMARY

The funding of the SRC grew to $34 million in its first 9 years and has remained at about that level for the subsequent 9 years. With its budget almost constant in this latter period, the SRC has had to adopt a different management style in order to assure a continuing productive research program.

Table 8-4 SRC FINANCIAL METRICS

DERIVED FROM ANNUAL FINANCIAL REPORTS

Year	A Total SRC Expenses (Million $)	B SRC Research Expenses (Million $)	C US Industry Shipments (Billion $)	D SRC Fees /Industry Shipments (D=H/C) ($X10^{-3}$)
1999	37.3	36.0		
1998	34.9	30.6	63.4	0.57
1997	33.4	28.4	70.0	0.49
1996	38.0	32.5	62.0	0.48
1995	38.4	33.2	50.8	0.49
1994	34.5	29.7	44.2(43.3)*	0.52
1993	36.5	31.1	33.3	0.72
1992	35.6	3O.4	25.5	0.95
1991	35.5	29.9	21.4	1.12
1990	34.1	29.8	20.1	1.08
1989	27.2	23.5	18.5	1.11
1988	22.8	19.5	17.3	1.07
1987	19.1	16.6	13.6	1.18
1986	19.3	17.0	11.4	1.44
1985	16.8	14.7	10.6	1.86
1984	13.4	11.7	14.0	0.85
1983	7.0	6.1	19.7	0.63
1982	0.7	0.3	8.0	0.49
Totals	484.5	421.0		Average 0.89

	E Total SRC Revenue (Million $)	F SRC Grant Funding (Government) (Million $)	G SEMATECH Funding of SRC (Million $)	H Fee Based Revenue H = E-F-G (Million $)	I SRC Income /US Industry Shipments I=E/C ($X10^{-5}$)
1999	44.0	0.3	1.8	41.9	
1998	38.7	0.1	2.0	36.1	0.61
1997	36.1	0.2	0.4	34.1	0.52
1996	39.7	0.5	9.0	29.9	0.64
1995	36.5	0.3	11.3	24.8	0.72
1994	35.2	0.4	12.0	22.8	0.80
1993	34.8	0.8	10.1	23.9	1.04
1992	35.0	0.8	9.9	24.3	1.37
1991	35.2	0.9	10.3	23.9	1.64
1990	35.4	1.3	12.4	21.8	1.76
1989	28.0	0.6	6.8	20.6	1.51
1988	26.6	5.0	3.0	18.6	1.54
1987	17.6	1.5	0	16.1	1.29
1986	16.7	0.3	0	16.4	1.46
1985	19.7	0	0	19.7	1.86
1984	11.9	0	0	11.9	0.85
1983	6.1	0	0	6.1	0.63
1982	3.9	0	0	3.9	0.48
Totals	499.1	13.0	89.0	397.1	Average 1.10
Percent	100	2.6	17.8	79.6	

* In 1994, IBM semiconductor shipments were included in the merchant semiconductor market for the first time. The (43.3) entry in column C for 1994 is the estimated market shipments without IBM in order to provide a direct comparison with prior years.

D is the ratio of member fees to industry shipments. I is the ratio of total SRC revenues to industry shipments.

Chapter 9

THE ADVISORS

Cooperative activities benefit from collective inputs
but, if care is not taken,
collective criticism can reduce the best to the average

The success of any enterprise depends on effective relations with its constituencies, whoever they may be. A commercial organization has three constituencies: investors, employees, and customers. SRC also has three, but they are different: members, staff, and research performers. It looks to its members for resources, direction, and utilization. It's staff manages and coordinates the research, disseminates the results, and represents industry's collective research interests. The research performers provide a relevant education for future employees of the industry and also provide useful results in the form of new knowledge on the design, synthesis, and technology of integrated circuits. Without these three constituencies the SRC would cease to exist. SRC also works with government and other organizations without becoming dependent on them. Relationships are created, become productive, and sometimes disappear with the participants continuing on their separate courses. Interactions with these organizations require mutual benefits to become lasting, and the benefits are proportional to the participation in the SRC activities.

The success of cooperative organizations, like the SRC, is highly dependent on effective linkages to its members and research contractors. SRC's Board of Directors and its advisory committees are among the most important linkages. These bodies exist to guide the SRC. This chapter reviews their forms, functions and roles in SRC's cooperative semiconductor research.

Some argue that the SRC gets in the way - that it is an unnecessary middle-man in the structure of semiconductor research. In that view, industry could fund university research much as it did before the SRC, with the expense of the intermediary organization, the SRC, eliminated. The counter view is that the SRC is necessary to coordinate and direct the support of university research in order to eliminate undesirable redundancy and to assure effective use of resources. Without such management, much of the investment would be wasted. The most compelling purpose of the SRC is to provide each member access to results of research supported by all members and thus, through cooperating, to provide substantially more than if each member acted independently.

Again, it is key that for many participants, the SRC provides their only direct contact with semiconductor device research. For the few members that still perform research themselves, the SRC provides the opportunity to participate in research areas that they are unable to address

internally and to maintain essential awareness of the trends and results in those areas.

SRC has three advisory bodies; the Technical Advisory Board (TAB), the Government Coordinating Committee (GCC), and the University Advisory Committee (UAC). Of these, the TAB is largest and most important. It provides the essential inputs from SRC members to the research program. The GCC and the UAC have functioned as programmatic and operational advisory committees, meeting less regularly and responding to issues raised by their constituencies and by the SRC. The GCC, as it name implies, consists primarily of representatives of Government organizations participating in the SRC and, in addition, provides an interface between SRC and government microelectronic research activities. The UAC is a quasi-independent, self-perpetuating committee of university participants in the SRC. The history and functioning of these committees are discussed in the following sections.

THE TECHNICAL ADVISORY BOARD (TAB)

Today, the TAB consists of representatives of SRC members on an Executive Committee and eight (sub)committees, one for each of the science areas in the SRC research program and for student services and technology transfer. The Technology Transfer Committee monitors the effectiveness in the transfer of research results from the universities to SRC members. Each science area committee is concerned with reviewing and advising SRC management in one area of the research program with respect to: 1) the quality, productivity, and relevance of research funded by the SRC, 2) the research needs of SRC members, and 3) the performance of the SRC with respect to addressing these needs.

Throughout the history of the SRC, the TAB has had an increasingly important role. It advises on both the content and the quality of the research program. Member representatives on the various TAB committees provide the primary technical contacts between member organizations and the SRC. At the first SRC Board of Directors meeting in March of 1982, the TAB was described as follows;

> "A key role in advising on the strategy, content of programs, and effectiveness will be performed by a Technical Advisory Board. It will consist of between 6 and 20 members appointed by the Board of Directors. They will be selected primarily from the academic and government communities, and from the members' employees. While not intended to be full-time assignments, the Technical Advisory Board membership will be heavily relied upon for their expertise in the planning and evaluation of all of the work supported by the Cooperative."

and from the SRC By-laws published at about that same time:

> "Section 6.2 Technical Advisory Board
>
> (a) The Board of Directors may, by resolution adopted by a majority of the Directors then in office (provided a quorum is present), create a Technical Advisory Board for the Corporation. The Technical Advisory Board (the "Advisory Board) shall consist of not less than six (6) and not more than twenty (20) members, who shall be selected by a majority of the Board of Directors (provided a quorum is present). The Advisory Board may include, but shall not be limited to representatives from the academic and government communities, as well as from among the Members' employees. Persons who are not Directors may serve on the Advisory Board.
>
> (b) The Advisory Board shall advise and oversee the technical performance of the projects conducted by the Corporation."

From its initial meeting in September of 1982, the SRC TAB has provided the essential interface to industry technology in goal-setting, research-reviewing, prioritizing, transferring technology, and mentoring. It has guided and advised the SRC through interactions with government and industry. In notes from the June 1982 Board of Directors meeting, the 'main group' of the TAB is designated as SRC's technical advisor for the purpose of identifying research thrusts, evaluating proposals, transitioning research results to industry, and establishment of subcommittees as needed. The subcommittees would be the technical advisors to the SRC managers in the several research areas that constitute the SRC research agenda.

Soon after the founding of the SRC, the limitations on member participation in the TAB were modified to allow each member to participate in every TAB committee in order to provide full access to all research results. This was key. The larger member companies have participated in all of the TAB committees while the smaller companies participate only in their interest area. Although seldom exercised, there remained a limitation of one-vote per member when formal actions are taken.

In addition, the TAB is a 'member' committee with the interests of university and government participants addressed through the UAC and GCC. At its first meeting, in September of 1982, the TAB divided itself into technical subcommittees for the purpose of evaluating proposals. This process has continued to evolve to where a total of eleven TAB committees are now active; the ETAB (executive TAB), eight science TABs, the Technology Transfer TAB, the Student Services TAB, and a special TAB for the Center for Semiconductor Modeling and Simulation. Even though the TAB is viewed as an entity, its confluence is nebulous. Each committee has a full agenda in its assigned area with coordination with the ETAB and other technical TABs lower in the priority.

An early issue was whether the TAB made decisions or advised the SRC. This issue arose

when, with the Chairman's approval, five research project awards were made by SRC management in December 1982 without TAB review in order to accelerate SRC's start-up. When the role of the TAB, advisory or decision maker, was discussed until in January 1985, George Scalise, then Chair of SRC's Board stated emphatically that "The generation of new research directions and thrusts is the responsibility of the SRC (staff). They should not depend on the TAB for this." This decision was based on the full-time involvement of the staff with the research as opposed to the once per month involvement of most TAB members.

Over time, this issue has faded as TAB inputs to contractual decisions were routinized and deviations from TAB advice became infrequent. Most importantly, issues relating to who is responsible for the program disappeared when TAB science committees and the SRC research program directors worked closely enough together to evolve consensus program management decisions. This has worked well. Care is required to prevent program decisions from becoming too strongly focused in the TAB science committees with little input from the SRC Program Managers. Even though all decisions are reviewed by SRC's Research Management Committee before being implemented, a strong role is required from Program Managers to insure integration of the research across the boundaries of the research areas and a uniformly high quality program.

As noted, the first meeting of the TAB took place on September 10, 1982 in SRC's soon to be occupied quarters in the Research Triangle Park of North Carolina using borrowed furniture. It was fundamentally a get-acquainted meeting in which the newly appointed TAB membership and SRC staff explored their relationship and made plans for the evaluation of proposals resulting from the broad proposal solicitation then underway. The establishment of the initial SRC research centers in design and microstructure sciences were also discussed. This was the first of many TAB meetings taking place in the subsequent in the subsequent 18 years.

For all of the TAB Committees, there were a total of forty meetings in 1997, which is typical. The number of meetings has been reduced by conducting multiple contract reviews at one meeting rather than reviewing each contract separately. The normal practice is to rotate the review site among the major participating universities. There are however benefits in visiting with each of the university research teams and interacting with the faculty and students. The size of the research program has prevented this.

The 1997 TAB organizations are identified in Table 9-1.

THE TAB SUMMER STUDIES

Cooperative research is dependent on establishment of common boundaries for the

Table 9-1 TECHNICAL ADVISORY BOARD COMMITTEES

	Began	Ended
Technical Advisory Board	1982	
Executive Committee	1985	
Microstructure Sciences	1985	1994
Design Sciences	1985	1999
Manufacturing Sciences	1985	1989
Technology Transfer	1987	
Manufacturing System Sciences	1990	1994
Manufacturing Process Sciences	1990	1994
Packaging Sciences	1990	1999
Lithography Sciences	1994	1999
Factory Sciences	1995	1999
Interconnect Sciences	1995	1999
Process Integration and Device Sciences	1995	1999
Environment, Safety, and Health Sciences	1995	1999
Student Services	1998	
Nanostructure and Integration Sciences	1999	
Packaging and Interconnect Sciences		
Back End Processes		
Materials and Process Sciences	1999	
Computer Aided Design and Test Sciences	1999	
Integrated Circuit and System Sciences	1999	

technology which the research would seek to extend. In the early eighties, defining common boundaries was awkward because it revealed a company's technical knowledge base that was believed to be a strong factor in competition. There was much uncertainty as to how much information and insight should be shared. Each highly competitive SRC member was convinced that his company's know-how provided competitive advantage. They were cautious in doing anything that might decrease that advantage.

As information was gradually disseminated in research reviews and workshops, it became increasingly evident that there was much in common among these supposedly private knowledge bases. With little to protect, protectionism decreased. SRC members began to cooperate closely in their discussions of SRC research. This increased cooperation led the Executive Committee of the SRC Technical Advisory Board to recognize that its responsibility for guiding the research

required more input than could be obtained in one-day meetings every other month.

The 'Summer Studies' became the answer. From these 2½ day annual meetings, the nature, scope, and methods of cooperative semiconductor research evolved. Originally intended to merge the findings of its technical committees, deal with overlaps, and advise the SRC on the broad and general aspects of its research, the summer studies evolved to focus most strongly on the latter. Define issues were selected as the theme of the meeting. These themes are listed in Table 9-2.

The format of the summer study was to have papers presented by SRC staff, TAB members, and others to provide in-depth perspectives on selected issues. These issues are subsequently addressed in general discussions. recommendations derived, and the focus of the meeting was defined. A small number of questions on the theme and the group separated into smaller working groups to propose answers to these questions. From 25 - 50 people have participated in the summer studies. In the beginning, it was primarily the ETAB and the SRC technical staff. At various times, the Government Coordinating Committee and the University Advisory Committee were invited to participate as were members of the Board of Directors.

The first SRC Summer Study was held in Minnesota and focused its attention on the broad aspects of SRC research. The structure of the meeting is given in Table 9-3 where the objectives, goals, and recommendations are given. The SRC was instructed to report on the implementation of these recommendations at a later meeting. It was estimated that about half of the eighteen recommendations were implemented.

Table 9-2 THEMES - SRC TAB SUMMER STUDIES

1984	Minnesota	Research Goals and Priorities
1985	Denver	SRC Research Priorities/Industry Needs
1986	Vail	Roadmaps
1987	Park City	SEMATECH, SRC Growth, Tech Transfer
1988	Sun Valley	SRC Organization & Operations
1989	Charleston	2001 Research Goals
1990	Keystone	Changing Technology and Operations
1991	Port Ludlow	Repositioning, Consortia, Technology Insertion
1992	Sante Fe	National Labs & Long-term/High-risk Research
1993	Park City	Enhancing the University Research
1994	Scottsdale	Achieving Customer Satisfaction
1995	Le Chateau Montebello	Resetting the Research Agenda
1996	(Techon '96 - SRC Research Review)	
1997	Lake Tahoe	Strategic Planning
1998	(Techon '98 - SRC Research Review)	
1999	Vancouver	Technology Roadmaps, Focus Centers, Students
2000	(Techon '2000 - SRC Research Review)	

Table 9-3 SUMMER STUDY 1984

Objectives:

1. Examine in depth the research agenda of the SRC,
2 . Identify/prioritize research objectives and identify needs not now addressed in the research agenda,
3. Critique the existing mechanisms for evaluation of SRC research,
4. Increase the effectiveness of information dissemination and technology transfer, and
5. Provide recommendations to improve the utility of the research results data base.

Planning Committee Goals:

1. Updating the industry research goals for 1994,
2. Deriving a research program strategy to address these goals,
3. Disseminating information and technology transfer,
4. Defining the functions and structure of the TAB,
5. Developing the broad statement of purpose of the SRC,
6. Agreeing on procedures by which the SRC research projects are initiated,
7. Continuing the review and evaluation of SRC research contracts, and
8. Establishing selection criteria for SRC Research Centers.

Recommendations

1. Define the research agenda as all technologies that advance integrated circuits.
2. Goals for 1994 were based on acceleration of development by two years as a result of SRC research.
3. Define three major areas for SRC research -- Microstructures, Design, and Manufacturing -- processing -related research remaining a part of Microstructures.
4. Allocate research funding by 1987 in the ratio of 40:30:30 among Microstructures, Design, and Manufacturing.
5. Define research priorities consistent with the contemplated growth of the research budget including new research opportunities.
6. Apply budget increases up to $50M/year to expansion of the research budget and/or to enhancement of facilities/equipment at universities. It did not recommend use of such funds for fellowships.
7. The SRC proposed statement of purpose for the TAB was endorsed.
8. Each SRC member should be able to appoint a TAB member and two alternates, each of whom would serve on a different technical committee.
10. TAB members should serve as the "gatekeeper" for his company unless other means for information dissemination within his company are available.
11. Research initiation procedures were accepted that recognized the SRC Program Manager as having the primary responsibility.
12. The University Advisory Committee should appoint a member to participate in the TAB Executive Committee as a non-voting member.
13. Review procedures for evaluation/renewal of research contracts were endorsed.
14. Operational improvements for the highly successful industrial mentor program were recommended.
15. To promote assignment of industrial assignees from the member companies to the SRC for information dissemination, contract monitoring, and research program evaluation, it is recommended that the President request the Board of Directors to consider a 5% fee surcharge for those companies that do not provide an industrial assignees and that these surcharges be assigned to the SRC administrative budget,
16. An intermediate technology development activity to transfer SRC university research results to member companies was endorsed. It was concluded that this should be closely associated with industry so that results would be "application driven" and should not be a function of the SRC.
17. Criteria recommended for designation of a university or group of universities as a Center include:
    (1) two years as an SRC program,
    (2) funding in excess of $1M/year, and
    (3) a focus toward a major SRC goal.
18. It was concluded that annual and ad hoc planning meetings should be held, and that the attendees should

include both the outgoing and incoming TAB officers.

At the second summer study in 1985, the participants identified the issues listed in Table 9-4 on which to focus ETAB and Summer Study attention. The redundancy with the 1984 agenda highlights the more significant topics. The research goals of the SRC became a recurring subject for the summer studies. A characteristic of long-range goals guiding research is less specificity than the short-range goals that guide development. With each new generation of the goal-setting processes the structure and quality of the resultant goals were improved,

The issues, identified in 1985, could be applied almost equally well today although there has been significant progress in the SRC as well as in the technology. In fact, from 1982 to 1996, the IC line width decreased by about one order-of-magnitude, from 2.5 microns to 0.25 microns and DRAMs have grown from 64K to 256 megabits, an increase of 4,000X. Many of the issues associated with manufacturing competitiveness, equipment, and time-to-market are now addressed by SEMATECH. The primary flow of results emanating from the summer studies has related to the research goals and to the SRC research portfolio. The introductory presentations given at the summers studies are listed in Table 9-5.

Table 9-4 ISSUES IDENTIFIED AT 1985 SRC SUMMER STUDY

1 How can SRC help improve manufacturing competitiveness?
2 What is optimal distribution of the SRC budget among the research areas?
3 How can SRC research results obtain optimum use by member companies?
4 What is role of SRC in attaining manufacturing parity and leadership?
5 Assessment of SRC research re state-of-the-art, competitiveness, and redundancy
6 Measurement of SRC program effectiveness
7 Integration of SRC research areas to obtain leadership in manufacturing
8 Scope of the SRC
9 Realism of SRC goals, what should they be, and what resources would be required
10. Harmonization of university and industry goals
11. Participation from additional scientific disciplines in SRC research
12. SRC's role in cooperation between IC makers and equipment suppliers
13. How to make 'time-to-market' less than 'product lifetime'
15. Process, device, and manufacturing technology needs for future competitive products
16. University ability and cost for research relevant to manufacturing
17. What can participants expect from SRC?
18. Company scenarios for exploiting strengths and shoring up weaknesses - implications?
19. How to get graduate students directly involved in SRC

Table 9-5 INTRODUCTORY PRESENTATIONS FOR THE SUMMER STUDIES

(Not in order)

TAB, UAC, etc.

- Design - K. Slater, DEC
- Manufacturing - S. Jaskolski, Eaton
- Technology Assessment - C. Skinner, National
- Effective Linkages for Cooperative Research - Parker , DEC
- Long Term/High risk Competitive Research - Tim Trick, Illinois
- NIST and University Research - F. Oettinger, NIST
- Design Sciences - T. Costen, Harris
- Microstructures - C. Skinner, National
- Integrated CAD/CAM/CAT - D. Hodges, UCB
- Encouraging Innovation - W. Oldham, UCB
- Manufacturing Process Sciences - W. Starks, Varian
- Packaging Sciences -K. Brown, DEC
- Technology & Knowledge Transfer - A. Tasch, U Texas
- Microstructure Sciences - Moss, Delco
- Government view - Jim van Fleet, DoE
- University Research in the SIA Framework - J. Ballantyne, Cornell
- Market Pull: The Technical Workstation Market - K. Pocek,. - Intel
- Market Pull: The Supercomputer of 2005 - J. Key, CDC and R. Burke, SRC
- Market Pull: Automotive & Industrial Markets - E. Whitaker, Delco/ J. Gragg, Motorola
- University Access to an Insertion Manufacturing Facility - N. Masnari, NCSU
- The NSF and Research for the Semiconductor Industry - L. Salmon, NSF
- SRC Activities: How to Evaluate Them - W. Finan, Technecon, Art Link, UNCG
- Research Process Differences between Universities & Industry - C. Nuese, Consultant
- Technology Research Opportunities in Research Integration - D. Bartelink, HP
- Role of Infrastructure in the SRC's Research Agenda - G. Alcott & J. Carruthers, Intel
- Role of National Laboratories: Industry view - S. Knight, AT&T & J. Carruthers, Intel

SRC Staff

R. Burger, J. Freedman

- SRC Research Environment
- SRC and Government Programs
- Research Prioritization
- SRC's Extended Planning Horizon
- SRC, SEMATECH, & Semiconductor Strategy
- Roadmaps, µTech 2000, SEMATECH II, & SRC
- Organization for 2001: TAB, SEMATECH, Etc.
- Technology Push: Technology Trends Assessment
- SRC Long Range Plan
- Technical Goals for 2001
- Minimizing the Research-to-Commercialization Cycle
- The SRC's Role and Operational Structure

W. Holton

- SRC and National Planning for Semiconductor Technology
- Research operations
- The SRC's Growth

R. Cavin

- Enhancing the University Research Program
- Software Portability
- Technology Roadmaps

H. Phillips

- Technology Roadmaps
- Corporate Goals for 2001, International and Domestic
- Funding Growth - Recruiting New Members
- Manufacturing Competitiveness
- Inventions and Innovations

E. Holland - Government Participation and Role

R. Lucic - Technology Transfer in 2001

J. Cox - Tech Transfer, Communications, and Data Acquisition - Organizational Interfaces

N. Foster, P. Verhofstadt - Manufacturing System Sciences - Critical Challenges and Research Efficiency in IC Design

L. Gardner - Technology Transfer Best Practices

Table 9- 6 RECOMMENDATIONS FROM SUMMER STUDIES

Establish summer study as annual event
Increase emphasis on manufacturing sciences
Continue to improve operations and administration
Undertake competitiveness initiatives
Identify critical needs for high volume manufacturing
Redefine TAB membership.
Identify design sciences needs and SRC role
In microstructure sciences stress in situ, sub µm, unit processes, and lithography
Establish video links to members and researchers
Continue Manufacturing Competitiveness Panel
SRC focus on long-range research, understanding, new concepts
Increase attention to intellectual property
Increase role of University Advisory Committee
Make technology goal-setting #1 priority
Consider role of National Laboratories
Include government agencies on TAB
Reward effective technology transfers
Prepare white papers on technologies
Prepare white paper on industry usage of SRC graduates
Adopt technology accelerators
Find better ways to improve quality of information
Endorse and support NACS roadmap effort
Decrease administrative loads on SRC research directors
Improve efficiency of review by clustering
Make foreign students hireable
Improve cooperation among semiconductor research bodies
Increase use of electronic communications media
Establish 'Industry support activities', mission and budget
Improve dissemination and public relations
Integrate roadmaps
Establish research integration facility
Strengthen manufacturing research (J. Semi. Manuf. Resch)
Identify show-stoppers in roadmap
Focus on key technologies
In manufacturing sciences stress the image issue, viability as discipline, and a demonstration facility
Develop view of the future
Develop technology consensus
Continue roadmap integration and begin on 2001 goals
Address software hardening issue
Increase 'people exchanges' and stress on technology transfer
Work with National Advisory Committee on Semiconductors
Consider research integration with DoD
Use needs analysis to target technology products
Upgrade roadmap re systems interconnect, pattern transfer, and reliability
Identify research areas that need to be expanded
Find ways to use non-SRC research
Develop research 'sunset' policies/practices
Review foreign funding guidelines
Increase technology involvement of SRC directors
Develop list of SRC services to be discontinued
Improve TAB - BoD communications
Improve research reporting
Expand CoEs
Improved technology needs identification

Do white papers on:

aggregate capabilities	memory I-O limitations	high-level simulations	systems integration
fab-line training	neural networks	power ICs	system-level design
concurrent engineering	pervasive technologies	training/education for the fab line	

Technology efforts needed on:

metrology, patterning	optical interconnect	multilevel interconnect	packaging
process integration	packageless chips	eD-packaging	merged device technology
integrated software	errorless code	novel architectures	planarizing dielectrics
hi K	defect reduction		

Synchronize with academic calendars
Provide executive summaries in all reports
Provide summaries of research results
Encourage research partnerships
Develop united industry front on cooperative efforts
SRC agenda - university research, forums, NACS, gaps
Develop member recruiting strategy
Provide statistics on students and jobs
Include technology transfer in management plan
Provide statistics on member participation in SRC
Limit number of research consortia
Use consortia for leverage, to reduce redundancy, spread
Look into technology insertion manufacturing facility
Address strategic technology needs not being addressed elsewhere

THE GOVERNMENT COORDINATING COMMITTEE

Beginning in 1989, the Government Coordinating Committee (GCC) provided opportunities for various government organizations to obtain information about and to interact with the SRC. It recognized the Government participation in the SRC, implemented through a Memorandum of Understanding (MOU) with the National Science Foundation (NSF). The history of the government funding is given in Table 8-5. Other government agencies have provided funds through transfers to the NSF. Because of the nature of government funding and the fact that government and SRC fiscal years do not correspond, the government support of the SRC has been highly variable.

The GCC consists of representatives of the government agencies that provided funds as well as others with interests in semiconductor R&D. Its members are listed in Table 9-5. These are agency representatives that sat for some period on the GCC. The GCC met irregularly to review SRC's research and to promote increased information exchange. In addition, an NSF

Table 9-7 Government Coordinating Committee Membership

William R. Bandy Defense Advanced Research Projects Agency
James A. Cauffman Office of Naval Technology
Edwin B. Champagne Wright Research and Development Center
Lewis M. Cohn Defense Nuclear Agency
John C. Davis National Security Agency
William J. Edwards Wright Research and Development Center
Michael Fluss Lawrence Livermore National Laboratory
C. Edward Holland, Jr. Semiconductor Research Corporation
Frank L. Huband National Science Foundation
Harold L. Hughes Naval Research Laboratory
Gerald Iafrate Army Research Office
Tim Kemerley Wright Laboratory
Norman Kreisman Department of Energy
Richard D. LaScala Semiconductor Research Corporation
Ingham A. Mack Office of Naval Research
E. D. (Sonny) Maynard Jr. Office of the Undersecretary of Defense
Frank F. Oettinger National Institute of Standards and Technology
Irene C. Peden National Science Foundation
D. Howard Phillips Semiconductor Research Corporation
Daniel S. Prono Los Alamos National Laboratory
Thomas J. Russell National Institute of Standards and Technology
Kermit Speierman National Security Agency
Michael A. Stroscio Army Research Office
Michael C. Vella Lawrence Berkeley National Laboratory
Nancy Walker National Security Agency
Marvin White National Science Foundation
David S. Yaney National Institute of Standards and Technology

official has participated in SRC Board of Directors meetings. Other government representatives have participated in the SRC TAB including research program reviews and evaluations.

THE UNIVERSITY ADVISORY COMMITTEE

Since 1982, the UAC has advised the SRC on management polices, processes, and procedures, on the scope and limitations of university research, and on other program issues. The UAC was originally organized to advise the SIA in the creation of the SRC and has continued as an important source of guidance throughout its history.

Table 9-8 1985 UNIVERSITY ADVISORY COMMITTEE

Charles E. Backus	Arizona State	Ralph Cavin	SRC
Steve Director	CMU	Dave Dumin	Clemson
Bob Hexter	Minnesota	Dave Hodges (Chair)	UCB
John Linville	Stanford	Noel MacDonald	Cornell
Nino Masnari	NCSU	Jim Mertz	UCSB
Paul Penfield	MIT	Joe Stach	MTP
Andy Steckl	RPI	Ben Streetman	Texas
Tim Trick	Illinois	Ken Wise	Michigan

Table 9-9 INITIAL UNIVERSITY ADVISORY BOARD RECOMMENDATIONS

1. Royalty-free, non-exclusive license will be granted to SRC on patents based on SRC sponsored research.
2. At each university microelectronics center with major SRC funding there should be a specific person identified as manager or coordinator for the SRC program. A major portion of his responsibility should be technical liaison for the purpose of transfer of information to the participating SRC companies.
3. It is recommended that the SRC encourage and favor university programs which take a multi disciplinary approach. This can include multiple departments within one university or the joint participation of more than one university.
4. To optimize information transfer between the university group and the SRC members, the following steps are recommended:
    - SRC resident in each key university
    - Regular technical meetings for SRC members and sponsored universities
    - SRC computer network linking participants
5. It is recommended that SRC member companies make facilities, services, and technical advice readily available to the university microelectronics centers. This can include foundry service, joint projects, summer student employment, and faculty consulting. Conversely, the university group should endeavor to provide specialized educational and research services to the SRC. For example, universities can provide retraining programs, use of specialized facilities, and aid with corporate recruiting programs.
6. It is recommended that SRC entertain proposals to increase teaching capabilities in integrated circuit related areas, as well as research proposals. Specifically, instructional laboratories involving students from appropriate science and engineering departments are encouraged. We also recommend that SRC support formal continuing education programs for retraining of personnel for the semiconductor field.

Chapter 10

PUBLICATIONS

Efficient access to information is the key to a successful future

There was, and are, no more efficient means for communicating broad arrays of information to a large, busy, and diverse audiences then through the printed word. Electronic media, e.g., the INTERNET, are efficient replacements for some printed material; messaging, accessing data bases, and for individuals looking for, sending, or receiving specific information. Printed media however, provide an 'information smorgasbord': newsletters, magazines, and research reports that are more efficient for providing easy, convenient, and selectable access to information from which selections are made by the reader. In the electronic display, one sees one or two pages. In printed media, the reader scans many pages and selects only those items that in which he is interested. A priori, he may not have known the information was there, but he probably knew that the source being scanned often yielded useful nuggets. Formerly, SRC used its newsletter, annual reports, and other publications as its information distribution system and let the different users select to meet their needs. This chapter relates the history and important role of this 'paper' in the development of cooperative research.

Mind patterns of new generations may adapt to electronic media. For now, the differing perspectives of printed and electronic media must be recognized and appropriate use made of each.

The SRC, in 1996, converted to an electronic site on the World Wide Web through which it distributes both public and private information on its results and activities. This is a much more economical media for information distribution. Through the Internet connection, members can access the output of SRC's research program, choose and obtain detailed reports, review the history of the SRC, and access the event menu and arrange their participation. Electronic distribution requires that users have access to all SRC products and choose those they want. But they must log-on and search. The transition from scanning printed documents to searching the Web is necessary. Current limitations of electronic information distribution may be overcome by future advances. When computers can easily "riffle the pages," scan and select, jump backward or forward, focus on details, read the headlines, and interact with the user, then the use of the printed word may gradually become obsolete. Meanwhile, the predicted decrease in paper usage resulting from increased computer usage is yet to materialize, either in the SRC or elsewhere.

THE NEWSLETTER

The first SRC Newsletter appeared in June of 1983 with the banner headline "The Semiconductor Research Corporation." One-hundred and sixty-two issues later (through 1996), the newsletter continued to provide a running record of cooperative research in the SRC. A company newsletter, in contrast to the public press, provides primarily positive information about the organization's activities. It is a biased source. Newsletters provide little insight into trials and failures of the an organization. Contract terminations, personnel departures, budget reductions, and research failures are not discussed. Contract awards, new hires, budget increases, and research successes are.

Titles of front page SRC newsletter articles are listed in the following table to provide a "Newsletter" view of SRC and its history. Despite the bias, this is a reasonable and informative picture of the first fifteen years of the SRC. The Newsletter has been important in this period, providing an essential internal and external linkage. Each issue provided a list of available SRC publications, announcements of upcoming events, and current announcements regarding fellowships, requests for proposals, and other matters. The primary articles involved descriptions of various university research programs, SRC research program summaries, state-of-the-SRC articles, and other subjects relating to SRC and its mission. The newsletter was distributed to over 13,000 readers each month many of whom were interested in the SRC but not otherwise participating. However, employees of the members were its prime audience and the content was tailored for their use.

During its publication, the SRC Newsletter was the most important link between the SRC and many of the technologists in its member organizations.

Table 10 -1 TITLES OF FRONT PAGE NEWSLETTER ARTICLES

1983		
	June	The Semiconductor Research Corporation
	July	SRC/SIA Joint Conference
	August	Tax Advantages of Membership in the SRC
	September	The Role of SRC in Technology/Information Transfer
	October	Research in Microelectronics Systems and Design
	November	Manufacturing Sciences Research Program
	December	Deposition Processes Topical Research Conference
1984		
	January	Microstructure Sciences Research Program
	February	CoE in CAD/IC at UC-Berkeley
	March	Cornell-SRC CoE for Microscience and Technology
	April	SRC-CMU Research Center for Computer-Aided Design
	May	Information Central
	June	Member Companies/Election of SRC Board of Directors
	July	IC Manufacturing Technology Research at MCNC
	August	SRC-Clemson VLSI Reliability Research Program
	September	GaAs Digital Integrated Circuits at UC-SB

	October	Program in Automated Semiconductor Manufacturing

Table 10 -1 TITLES OF FRONT PAGE NEWSLETTER ARTICLES (continued)

	November	SRC-RPI Program on Advanced Beam Systems for VLSI
	December	Microelectronic Manufacturing Science and Technology
1985		
	January	Directors' Corner - Design Sciences Activities
	February	Manufacturing Sciences Activities
	March	Microstructure Sciences Activities
	April	Research Goals for the SRC
	May	Design Sciences
	June	Highlights of the Past Twelve Months A Newcomer's View of the SRC
	July	Strategic Planning and the SRC Mfg Sciences Moves Ahead
	August	Microstructure Sciences Activities
	September	Cooperative Invention of Technology
	October	TAB Summer Study
	November	SRC-Its Role in the Transition of the Semiconductor Industry
	December	Software Portability
1986		
	January	Program Managers in Residence
	February	Microstructure Sciences ¼-Micron CMOS Activities
	March	Review of Recent Technology Transfer Activities
	April	IC Packaging Sciences Research
	May	SRC Contract Operations
	June	Management of Research
	July	Berkeley Automatic Synthesis Project
	August	Microstructure Sciences Research Strategy
	September	Goals in Microelectronics
	October	Summer Study Report
	November	Packaging Research
	December	Computer-Integrated Manufacturing
1987		
	January	Tech Transfer-Strategies for Expediting the Process
	February	Microstructure Sciences ¼-Micron CMOS Activities
	March	Cooperative Research in Microelectronics in Japan Semiconductor Initiatives and National Strategy
	April	Senator Bingaman's Address Highlights Washington Meetings
	May	Legislation Introduced to Establish National Advisory Committee on Semiconductors
	June	Advances in Technology - Computer-Aided Design in Japan Bowers succeeds Scalise as Board Chairman
	July	Role of the SRC in SEMATECH
	August	Workshop on Computer-Integrated-Manufacturing
	September	SRC Activities Impressions of an SRC Industrial Resident
	October	TAB Summer Study
	November	SRC Activities
	December	SRC Technology Transfer Activities - New TAB Committee Formed
1988		
	January	Decade in Review: Semiconductor Science & Technology General Meeting - SRC TECHCON 88
	February	Data Management for IC Computer-Aided-Design
	March	SRC Manufacturing Research
	April	SRC Washington Meetings
	May	University Advisory Committee Report
	June	Generic Semiconductor Research by the SRC
	July	SRC Names Two University Centers-of-Excellence
	August	TECHCON 88
	September	Response to University Advisory Committee Report New SEMATECH COO to Speak at TECHCON '88
	October	Competitiveness Foundation Joins Industry's Arsenal, 1988 TAB Summary Study Initiating Goals for 2001
	November	TECHCON '88 - A Resounding Success
	December	Sea-of-Gates Technology Issues

1989		
	January	First SEMATECH Centers Established
	February	Awards for Tasch and Prince
		Analog Design Automation: Status and Research Needs
	March	Design for Manufacturing

Table 10 -1 TITLES OF FRONT PAGE NEWSLETTER ARTICLES (continued)

	April	Conference and Workshop on Plasma Etch SRC Annual Technical Meeting
	May	SRC/University of Michigan Center of Excellence for Focuses on Advanced Process Tools
	June	Silver Bullets and Silver Buds
	July	SRC Strategy Forum
	August	Educational Initiatives: Responding to a National Concern
	September	Trends in Semiconductor R&D
	October	Application of Chemometric Techniques to IC Manufacturing
	November	TAB Summer Study: Defining Research Goals for 2001
	December	Semiconductor Research and Government Support
1990		
	January	Reassignments at the SRC
	February	Research Directions for CAD Frameworks
	March	SRC's Research Program - 1989
		President Bush Hears SRC Concerns - Government, Industry
		Share R&D Responsibility
	April	The Government Role in Semiconductor R&D
		SRC Board Approves Canadian Membership
	May	NTU Broadcast on Technology Modeling
	June	Technology Transfer Best Practices Workshop
	July	SRC's TECHCON '90 To Showcase Research Program Results
		Robert N. Noyce
	August	Expanded International Role Sought for SRC
		Three Companies Become SRC Affiliate Members
	September	Industry Residents are Key Asset to SRC Research
	October	TAB Summer Study
	November	The SRC Competitiveness Foundation
	December	TECHCON '90 Reviews SRC Research, Looks to Future
1991		
	January	Expanded Research Agenda Demands Greater Resources
	February	Mentoring Links Industry to SRC Research
	March	NIST Semiconductor Electronics Division Works to Assist U.S. Industry
	April	Plenary Speakers Endorse National Technology Strategy
	May	Role of Consortia in Electronic Materials
	June	SRC-Delco-Purdue Relationship Fulfills SRC Mission
	July	Workshop on Real-Time Tool Controllers
	August	Course-Microcontamination and Control in ULSI Manufacturing
	September	Government Urged to Increase Cooperative Research Efforts
	October	1991 TAB Summer Study
	November	Reliability Workshop
	December	TCAD Conference
		Foundation Holds Fellowship Program Conference
1992		
	January	Preparing for the SRC's Second Decade
	February	Quality for Our Industry
	March	Decade of Collaborative Semiconductor Research
	April	National Survey Ranks Technology
	May	Semiconductors: Foundation for America's Future
	June	SRC Research Products
		Manufacturing Systems Science-Putting it all Together
	July	Williams Elected Chairman
		Tenth Anniversary Dinner SRC Offers New Membership
	August	Microstructure Sciences Research
	September	Current Trends in Design Sciences Research
	October	Summer Study 1992
		SRC Kicks Off Total Quality Program

	November	SRC Launches Power IC Thrust
		Seventh Annual SRC/DARPA CIM-IC Workshop
	December	SRC Research A Decade Ago
1993		
	January	SRC Manufacturing Process Sciences
	February	Call for Papers and Posters for SRC TECHCON '93
	March	Synthesis Experiment Blazes Trail for SRC Community
	April	SIA Semiconductor Technology Workshop Results
		Last Call for Abstracts for TECHCON '93

Table 10 -1 TITLES OF FRONT PAGE NEWSLETTER ARTICLES (continued)

	May	Siegle Elected Chairman
		James Burke to Speak at TECHCON '93
		SIA/SRC Joint Conference, Part I "Unifying Our Vision for Economic Competitiveness"
	June	TechFair at TECHCON '93
		SIA/SRC Joint Conference Part II
		Preprints Needed for Library Demo at TECHCON '93
	July	TECHCON '93: Showcase for SRC's Research program Results
		Sources Sought For High Bandgap Semiconductor Research
	August	SRC's Enhanced Mission Evening's Activities Honor Researchers
	September	Retroview of a Resident
		ASEE Honors Lundstrom with Terman Award
	October	1993 Summer Study
	November	Industrially Oriented Research in a University Environment
	December	TECHCON '93, Interaction and Cooperation
1994		
	January	1993 - SRC - 1994
	February	Fleming is 1994 Board Chair New R&D Center at Michigan Device Performance TCAD
	March	SIA Technology Advisory Structure Materializing
	April	The Changing Research Environment
	May	Industry to Benefit from DoE-SRC Cooperative Agreement
	June	Is the SRC Part of Your Company's Operating Strategy?
	July	Packaging Sciences Research
		Education Alliance Passes VISION's Baton
	August	SIA Workshop Attracts 240 Participants to Roadmap Process
	September	Enhancements from Mentoring-Linking Complementary Resources
	October	Summer Study 1994
	November	Board Prepares SRC for Future Challenges
	December	Lithography Research
1995		
	January	New Perspectives, A Rewarding Year
	February	Research Reassigned to New Science Areas
	March	Research in Design Sciences
	April	Washington Community Invited to NIST/SRC Meeting
		Semiconductor R&D: SRC Program Dynamics
	May	SRC Technology Transfer SIA Honors Professor Pederson
	June	Technology Policy and Social Factors NSF/SRC Partnership
	July	Factory Sciences Sensors for Advanced Equipment Control
	August	SRC Environment, Safety, and Health Research
	September	SRC Summer Study 1995
	October	SRC Research Strategy
	November	AMD Names Fellowship
		Sumney and Industry Members Honored
	December	The SRC in Evolution
		The Start of Countdown to Techon '96
1996		
	January	1995 Report from the SRC
	February	SRC Evaluates and Analyzes Member Satisfaction
		CSMS to Conduct First Annual Program Review
	March	While I've Been Away
	April	Mentors: The Bridge Builders
		Chairman Carinalli Guiding 1996 Board of Directors
		1996 Outstanding Mentor Award - Call for Nominations

May	A Tribute to Dr. Bob Burger
June	Join Your SRC Colleagues at TECHON '96
July	Center for Environmentally Benign Manufacturing
August	Critical Issues in Charged Beam Patterning
September	Technology Transfer "Best Practices" .. A Question of Expectations
	Continuous Quality Improvement the Scientific Method, and Excellence in Research
October	Rensselaer Establishing SRC Center of Excellence for Advanced Interconnect Science and Technology
November	SRC Community Gathers for TECHON '96
December	From Newsprint to Webprint

ANNUAL REPORTS

"The Annual Report of the Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC Research Program, present the formal financial report, and provide information on activities and events of the SRC industry/government/ university community for the previous calendar year."

(From the inside front cover of the 1995 Annual Report of the SRC)

SRC's first annual report was issued in 1984 for 1983. The most recent is for 1999. There are sixteen. All provide a 'state-of-the-SRC' letter by the Board chair and the President that record accomplishments and challenges of the organization for that point in time. Excerpts from these are given in Table 10-2.

The focus of the annual reports is on the integrated circuit research sponsored and managed by the SRC. Each year, highlights are noted and broad information on the direction of the research, its challenges, and significant accomplishments are reviewed. In addition, the annual report contains the required financial report and summaries of other SRC activities - roadmaps, goal-setting, government participation, meetings, patents, awards, etc. The design of the report has varied, reflecting different approaches to communicating effectively with the large SRC constituency. Annual reports are designed for the executive or the outsider, and as a tool for recruiting new members. They are distributed to SRC members and to others primarily upon request.

Table 10 - 2 EXCERPTS FROM SRC ANNUAL REPORTS

1983	"The SRC exists because of recognition by the industry that traditional responses in the United States to world competition were inadequate .." Erich Bloch
	"...SRC includes as its central core, a research program responsive to diverse industry needs, formed through cooperative assessment of capacities and roles, and implemented by contracts with appropriate research institutions." Larry Sumney
1984	".....I have seen and felt the effects of the SRC on the university research community and on our industry." George Scalise

"In 1984, ... $23 million will be spent on silicon research at universities, more than half of which is supplied directly by the SRC. Larry Sumney

1985 "..research agendas of universities are very much different..., internal activities of some member companies have been markedly affected by participation in the SRC, ...students who have participated in our university research are now working in industry, and barriers to cooperation have been reduced.....SRC is making a big difference." George Scalise & Larry Sumney

1986 "The SRC's role in the industry is solidifying and growing." George Scalise

Table 10 - 2 EXCERPTS FROM SRC ANNUAL REPORTS

"SRC has ... 10-year goals...and is evolving a research roadmap." Larry Sumney

1987 "The SRC has been a major participant ...in the creation of SEMATECH." Klaus Bowers

"SRC initiative - National Advisory Committee on Semiconductors." Larry Sumney

1988 "...the SRC Research Program produced 22 invention disclosures, 12 new patent applications, 1 patent, 850 new research reports/papers for distribution to member companies." Robert McMillin and Larry Sumney

1989 "...the SRC's being one of the most successful among cooperative organizations...challenged to enlarge footprint ... on the technology of this industry." Robert McMillin and Larry Sumney

1990 "In 1990, the SRC had 100 contracts with 60 research organizations that supported approximately 250 faculty members and 700 graduate student.....TECHCON"90...350 attendees." Frederic Schwettmann and Larry Sumney

1991 "What causes us to stop and think is that even with long-range goals and short-term graduate student researchers, the output of the SRC research program is finding immediate short-term applications." Gerhard Parker and Larry Sumney

1992 "... the SRC played a major organizing and planning role for the Semiconductor Industry Association's Semiconductor Technology Workshop in Dallas to (create) a long-tern technology roadmap for the industry." Owen Williamsand Larry Sumney

1993 "The Semiconductor Research Corporation (SRC), the industry"s first cooperative research venture, believes additional progress can best be achieved through strategic planning and continuous improvement in teamwork among industry, academia, and government." William Siegle and Larry Sumney

1994 "(SRC's) world-class research in fields as diverse as process technology, computer-aided design, and modeling and simulation software, helps assure the North American semiconductor industry's continued competitiveness, both now and in the next century." Owen Williams and Larry Sumney

1995 "In today's era of shrinking corporate and government research budgets, and increased global competitiveness, long-range semiconductor research - which provides the knowledge base for future generations o f products - faces formidable challenges." Owen Williams and Larry Sumney

1996 "At the SRC, we're helping to find solutions to technology roadblocks that lie ahead for our industry. While some issues, such as the need to reduce expenses, must confronted by almost every industry today, issues like whether the laws of physics will one day halt the advancement of transistors, are unique to our business." Larry Sumney

1997 "The SRC has and continues to provide dividends for its members. In passing our fifteen year mileston, we are at once evolving and rooted in the industry's landscape." Larry Sumney

1998 "During the past year, SRC's member companies, university researchers, and government partners, and our dedicated staff, have positioned themselves to begin the 21st century in an increasingly complex environment." Larry Sumney

1999 "SRC continues to realize Erich Bloch's extraordinary vision by conducting the largest continuous industry-driven university

research program in the US." Larry Sumney

RESEARCH REPORTS

Each year over 1000 research reports of one type or another are received from the research contracts and made available to SRC's membership. Many of these are early copies of research publications including dissertations while others have been required reports to the SRC concerning the research being performed. Until the year 2000, all SRC research contracts required the submission of technical reports as a benefit for SRC participants. The titles and abstracts of the reports were printed in the Newsletter and are now displayed on the SRC Web site. With further development of the SRC Web site the requirement for annual research reports has been discontinued.

The SRC distributed 12,471 reports in 1995, primarily to members of the technical staffs of SRC participants. In addition, the SRC provided reports to the libraries of participants where reproduction resulted in further distribution. This is a costly process that has now been replaced by electronic distribution system through the SRC site on the Internet as described in the following section.

Table 10-3 IMPACT OF THE SRC - DISSERTATION RESEARCH

Number of Ph.D. Dissertations in the U.S. With Given Key Word

	Year								
Key Word (s)	1982	1983	1984	1985	1996	1987	1988	1989	1990
silicon	162	186	206	213	280	352	407	416	470
integrated circuits	31	48	56	70	65	82	111	122	110
integrated circuits/CAD	2	3	6	10	3	11	10	10	7
Totals	195	237	268	295	348	445	528	548	587

Table 10-4 IMPACT OF THE SRC - 1991 IC/CAD PAPERS

	Country of Origin								
	US	CANADA	EUROPE	JAPAN	TAIWAN	KOREA	INDIA	JOINT	TOTAL
Academic	68	4	8	2	1	0	0	0	83
Industrial	9	0	4	9	0	1	0	3	26
Joint	8	0	3	0	2	9	1	6	17
	85	4	15	11	3	10	1	9	126

WEB-PAGE

With the objective of reaching a larger audience and reducing costs, the SRC newsletter was

discontinued in 1996 to be replaced by the Web page on the Internet as the primary media for distributing information on the SRC. The file structure of the SRC Internet site is shown in Table 10-5. These entries are backed up by extensive files of research publications and reports that provide a massive array of information for the members of the SRC. As with all WEB sites, the SRC site depends on providing a continually up-dated body of information that is readily accessed in order to attract users and thus succeed in its dissemination of the research results that are produced

Table 10-5 SRC INTERNET SITE STRUCTURE

- Find out about...
  - ○ The SRC
    - ° Vision and Mission
    - ° Member Value
    - ° Participating Universities
    - ° SRC Members
    - ° News
    - ° Organizational Charts
    - ° Address, Phone, Directions
  - ○ Funding Opportunities
  - ○ HR Needs Project
  - ○ MARCO Focus Centers
  - ○ Related Sites
- Explore ...
  - ○ Research Catalog
  - ○ Awards
  - ○ Portfolio
  - ○ Research Highlights
  - ○ Events
  - ○ Contracts Overview
  - ○ Intellectual Assets
  - ○ Publications
  - ○ Science Areas
  - ○ Students
- Targeted For...
  - ○ Board of Directors
  - ○ Advisory Boards
  - ○ University Researchers
  - ○ Industrial Liaisons
  - ○ Recruiters
  - ○ Students
- How do I ...
  - ○ Set Up Web Account
  - ○ Retrieve Password
  - ○ Set My Profile
  - ○ Contact the SRC

- Work with the SRC

Chapter 11

THE COOPERATORS

If we do not all work together to achieve our ends,
then we shall all work separately and not achieve our ends.

In the United States, it has not been easy for companies with common interests to cooperate because, over a century ago, large companies with dominate positions in their industry conspired to reduce competition and fix prices. The result was anti-trust legislation that addressed the problem but, in addition, restricted cooperation among companies without regard to purpose or merit. The triple damage penalty of that legislation led to excessive caution even with respect to cooperative activities that were not intended to be within its scope and limited almost any type of joint activity in U.S. industry for many years. Internationalization of competition now places a much different perspective on anti-trust enforcement with the advantage going to foreign competitors of the handicapped U.S. industry until a legislative remedy was enacted in 1983. Since then the legacy of anti-trust has been slowly decreasing and U.S. firms are expanding cooperative activities.

Since cooperation in support of university research was deemed exempt from anti-trust, even in 1982, SRC was not faced with legal barriers. Even then, questions were raised by cautious membership candidates. In fact, other cooperatives, the Microelectronics & Computer Technology Corporation (MCC) for example, that were focused on products were much more exposed. The result was the legislation relaxing the restrictions on cooperative R&D. This had no immediate effect on the SRC but has helped increase other forms of cooperation.

Even with the more open rules on industry cooperation, a government review of the SRC was conducted several years later. It had minimum impact. The only resulting advice was not to withhold research results from the public domain, something which the SRC had neither attempted nor intended. SRC's position was that publication was controlled by the participating universities and encouraged by the SRC. SRC retains for its members only the early access to research results that are a natural result of planning, managing, and directing the research; and the rights to use intellectual property that resulted.

As SRC established its core research program questions arose as to other forms of cooperation that could help its members. The workshops, meetings, and reviews required by the SRC research program provided ample opportunity for consideration of expanded cooperation.

Table 11-1 COOPERATION IN THE U.S. SEMICONDUCTOR INDUSTRY

1977	**SIA -** Semiconductor Industry Association
1982	**SRC** - Semiconductor Research Corporation
1983	**CERES -** Cooperative manufacturing development effort - not implemented.
1984	**LEAPFROG** - ½ micron production capability development - not implemented
1985	**MCP -** SRC Manufacturing Competitiveness Panel
1986	Defense Science Board Task Force on Semiconductor Competitiveness
1986	SIA/Sporck committee on semiconductor manufacturing competitiveness
1987	**Sematech** - Semiconductor Manufacturing Technology
1988 - 92	**NACS** - National Advisory Committee on Semiconductors
1992	SIA National Technology Roadmap for Semiconductors
1997	**MARCO** - Microelectronics Advanced Research Corporation

Over time, these discussions have borne fruit through new cooperative initiatives in the American semiconductor industry with profound positive effects on its competitiveness. Another result is the semiconductor technology roadmap which is discussed discussed in Chapter 6. This chapter focuses on the other cooperative initiatives arising from the SRC that are identified in Table 11-1.

SEMICONDUCTOR INDUSTRY ASSOCIATION (SIA)

The SIA was established in 1977 to provide a platform for communicating the U.S. semiconductor industry position on trade, technology, and economic policies to U.S. and foreign policymakers and to coordinate internal industry activities to more effectively resolve common concerns and develop a unified response to challenges facing the industry. The SIA provided the environment leading to the creation of the SRC and its Board elects the SRC Board of Directors each year and continues to have an important role in the creation of new initiatives such as MARCO and the International Technology Roadmap for Semiconductors. Its primary purpose and function has been to provide the interface to government for the many matters vital to the industry, and it has been very effective in that role.

CERES (1983)

Even before the first anniversary of the SIA announcement creating the SRC, expansion of cooperative R&D was being discussed. In the SIA Long Range Planning Conference in November of 1982, extension of SRC's agenda into technology development was discussed. The response was enthusiastic, rapid and, in less than one-year, led to preparation of a technical and business

plan for R & D on advanced semiconductor manufacturing processes and their demonstration with an advanced memory device. It was prepared by the SRC and referred to as the 'CERES PROJECT' after the Roman goddess of the harvest. It was described in an SRC document, 'CERES PROJECT SUMMARY' issued in September of 1983.

CERES was to be a cooperative development of a 1-megabit static-random-access-memory (SRAM) IC, a 4-megabit dynamic-random-access-memory (DRAM) IC, and ultra-large-scale-integrated (ULSI) logic chips along with the sub-micron complimentary-metal-oxide-silicon (CMOS) technology for their manufacture. CERES envisioned cooperative development of electron beam mask making, both x-ray and advanced optical lithography for patterning, low-temperature and dry processing technology, and an automated manufacturing process. This proposal was made at the time when 64 kilobit DRAMs were being produced in quantity and were viewed as the technology driver of the semiconductor industry.

Funding for CERES was expected to total $100 million over its four-year projected life. The SRC, as the general partner in a limited partnership, would contract for the device and process development with universities, research institutions, and commercial manufacturing organizations; and was to integrate the individual developments in a demonstrable, prototype fabrication line capable of producing the devices with viable yields. The results would be subsequently transferred to a manufacturing demonstration producing 1-megabit SRAMs and 4-megabit DRAMs for the U.S. Department of Defense.

A planning committee formed by the SRC concluded that CERES was both risky and necessary. Its stated purpose was to advance U.S. industry from being one product generation behind its Japanese competitors to being one generation ahead. These plans were presented to the SRC Board of Directors in September 1983. This was followed by a three-month effort to sign up companies for CERES. It was not successful. The planners were asked to change the plan from developing a 'product' to developing a 'process.' In early 1984, efforts got underway on what was to be called the 'new Leapfrog' proposal.

LEAPFROG (1984)

The objectives of Leapfrog were stated as follows:

- to develop a new generation of fabrication equipment for submicron applications on an accelerated time scale so that the equipment will be available two years earlier than would normally be expected, and
- to demonstrate that the new generation of equipment is manufacturing-worthy by implementing a prototype 0.5 micron CMOS demonstration/evaluation facility.

The participants would benefit by having ongoing access to technology developments; first refusal to resulting production equipment; royalties; shared costs; and tax write-offs. The effort would result in 'islands of automation' for lithography, etch, deposition, and ion implantation that would provide 0.5 micron processing for 8-inch wafers with three-level metal and 50 - 200 Å gate dielectrics. The SRC was proposed as the manager of the joint-venture project with close coordination with the DoD VHSIC Phase II program planned. Significant benefits from close coordination with the ongoing SRC research program were also envisioned. These plans were outlined in a business plan in July of 1984 which estimated that the total cost would be $99 million over a four-year projected life span.

Leapfrog was rejected in the fall of 1984 when it was presented to the SIA Board. The reasons appeared to revolve around a mixed attitude toward competition and cooperation in manufacturing technology; a desire not to divert SRC from its primary mission, i.e., research; and to the relatively high cost of Leapfrog. Fundamentally, industry leaders did not appear to be convinced that further cooperation was required at that time.

MANUFACTURING COMPETITIVENESS PANEL (1985 - 1986)

Shortly after the rejection of the Leapfrog proposal, a post mortem was conducted at SEMICON WEST by several industry participants. This was in May, 1985. It concluded that Leapfrog's demise was due to: 1) its large size, 2) too little insight and information, and 3) to too little experience in cooperation. The recommendation was that an Ad Hoc subcommittee of the SRC TAB's Manufacturing Sciences Committee be established to continue the discussions and develop approaches for addressing what the technologists viewed as an important need.

The activity that ensued began with a variety of names; 'Future of Microfabrication Committee', and 'Manufacturing Competitiveness Steering Committee', '.....Subcommittee', and '.....Panel'. Initially, it seemed that a different name was used for each meeting. 'Manufacturing Competitiveness Panel' or MCP was settled on by the end of 1985 by which time meetings were being held almost every month, usually in association with research contract reviews being carried out by the Manufacturing Sciences Committee of the SRC TAB.

The membership of the MCP is listed in Table 11-2. This group evolved to address the semiconductor fabrication equipment issue as a key part of the manufacturing competitiveness challenge to the U.S. integrated circuit industry and worked cooperatively to identify what was

necessary for U.S. equipment makers to assume the lead in functional performance and customer satisfaction.

Table 11-2 MANUFACTURING COMPETITIVENESS PANEL PARTICIPANTS

		INITIAL			
Dr. M. E. Beguwala	Rockwell	Dr. R. M. Burger	SRC	Dr. B. L. Crowder	IBM
Dr. R. C. Dehmel	Intel	Dr. S. Harrell	Micronix	Dr. S. V. Jaskolski	Eaton
Dr. Colin Knight	AMD	L. Kolito	SEMI	Dr. D. A. Peterman	TI
Dr. D. H. Phillips	SRC	W. Reed	SEMI	Jack Saltich	Motorola
Dr. C. Skinner	National	Dr. W. Snow	SEMI		
		SUBSEQUENT			
Shakir Abbas	SRC	Darrel Erb	AMD	Kurt Gsteiger	Harris
Norman Goldsmith	RCA	Tom Haycock	Harris	Ernst Hoyer	Eaton
Jack Kilby	Consultant	R. LaScala	SRC	Bob Luce	Signetics
Richard Lucic	SRC	Phil Lutz	SRC (GMC)	John Martin	Motorola
I. Pacheco	HP	Ray Roberge	Union Carbide	Ira Weissman	Varian
Stan Hancock	Micromanipulator Co	Gary Heckman	Ware and Freidenrich.		

In the second meeting of the MCP, it was concluded that;

1) U.S. competitiveness in semiconductor manufacturing is essential,
2) semiconductors are a key U.S. economic sector,
3) U.S. IC manufacturers must have the best know-how and tools,
4) chip-makers and tool-makers had to work in closer harmony,
5) the SRC should carry the ball,
6) the importance of manufacturing technology had to be broadcast,
7) a 'white paper' should be prepared to focus the effort, and
8) the importance of manufacturing engineers must be emphasized.

All of this was, in a sense, the lessons-learned from Leapfrog and provided the basis for understanding required for the next step.

The Manufacturing Competitiveness Panel (MCP) moved fast. On July 31 and August 1, 1985, an SRC Symposium was held in San Jose to discuss manufacturing technology issues with a broader group of concerned industry leaders. Over fifty people participated. The focus was on semiconductor fabrication issues as they impacted the competitiveness of the U.S. IC industry, on requirements for keeping U.S. equipment makers in the lead, and on a plan to make this happen. The opening premise of the meeting was that Japan would top the U.S. in IC sales by 1990 unless fundamental changes were made in practices and attitudes. (This was, in retrospect, conservative. Sales of Japanese semiconductor companies exceeded those of U.S. companies in 1988.) Concern was focused on leadership in advanced manufacturing equipment. Trade policy, cost of capital, and education were important issues excluded from the agenda because they were being addressed elsewhere. The agenda is in Table 11-3.

Table 11-3 MANUFACTURING COMPETITIVENESS WORKSHOP - July 31, 1985

Meeting purpose, goals and format		
	C. Skinner	National
The challenge in manufacturing competitiveness		
	R. Noyce	Intel
Panel - Japanese strategy and its impact on U.S. competitiveness in ICs		
Moderator	W. Ouchi,	UCLA
Panelists	J. Hutcheson	VLSI Technology
	W. North	IBM,
	D. Peterman	TI
Panel - IC maker issues		
Moderator	S. Jaskolski	Easton
Panelists:	D. Lando	AT&T
	G. Kern	MMI
	D. Sikes	Motorola
	J. Cunningham	AMD
	T. Malanczuk	NSC
Panel - Special observations:		
	K. Saraswat	Stanford
	T. Hartman	Intel
Panel - Equipment manufacturer issues		
Moderator	M. Beguwala	Rockwell
Panelists	E. Hoyer	Eaton
	Tom Halloran	Perkin Elmer
	P. Reagan	GCA
	W. Snow	SEMI
	I. Weissman	Varian
Attacking the key problems		
	R. Dehmel	Intel
Open discussion of possible priority solutions/implementation strategy		
Summary and recommended action		
	H. Phillips	SRC

Dr. Robert Noyce of Intel keynoted the symposium and provided valuable insight on the problem. He viewed it as a serious threat and saw parallels with the Japanese success in automobiles. Already, he observed, U.S. manufacturing was on a downward spiral with many American products being produced overseas. Dr. Noyce saw a valuable role for the SRC in providing the forum for discussion of the issues and for developing a plan for action. About two dozen other industry speakers addressed relevant issues. Some believed that U.S. had already irretrievably lost its leadership in semiconductors.

The meeting recommended that equipment user-vendor dialog be improved, that a video be prepared on the equipment supplier issue, that continued dialog between chip makers and equipment suppliers occur, that vertical integration and knowledge sharing be encouraged, that projects be selected for cooperative development, that the government intervene, and that communications on the issues be continued. One participant recommended that nothing be done

until a larger crisis evolved because it was felt that without a crisis, effective responses would not be possible. A strong consensus emerged for continuing the search for viable solutions through the SRC/MCP even though some participants believed that it was already too late.

Subcommittees were organized to address manufacturing processes, implementation concepts, user-supplier discussions, the importance of manufacturing technology, and improving the competitive edge of the U.S. chip industry. The subcommittees addressed these assignments and reviewed their recommendations and actions at meetings of the MCP over the next year. Significant actions resulted. One was an IEEE Journal that focused on semiconductor manufacturing. A second was a series of equipment user-vendor meetings in which the issues associated with US fabrication equipment were addressed. The third was organization of a Defense Science Board Task Force on Semiconductor Dependency described in the next section. A fourth was a heightened awareness of the issue by leaders in the semiconductor industry that resulted in a presentation by Charles SPORCK, President and CEO of National Semiconductor Corporation to the SIA Board of Directors in May of 1986. In his remarks, Mr. Sporck proposed to the executives of the industry the organization of a cooperative initiative to address the manufacturing technology issue.

The outline of a presentation evolved by the MCP to call attention to issues consisted of the following topics;

- Manufacturing Competitiveness Panel objectives and membership
- The current situation - decline of U.S. industry share of world semiconductor markets
- The Japanese strategy and threat - imitation, consolidation, and domination
- Prior U.S. response - product strategy versus manufacturing capability
- Recommendations re strategy for restoration of manufacturing competitiveness
    - Strengthen U.S. manufacturing engineering through education, research, awareness
    - Management commitment to equipment vendor relations and cooperative research
    - Major cooperative equipment and manufacturing process technology development
    - Industry-government semiconductor manufacturing technology initiative

In addition, the elements of a plan to address semiconductor industry competitiveness were described with a focus on:

- strengthened U.S. manufacturing competitiveness through education, research, and awareness of need for innovation,
- cooperative equipment development by better user-vendor communication, active user participation in standard setting and joint equipment development projects,
- use of U.S. strengths to enhance productivity through innovation taking advantage of our large sophisticated markets,
- competitive assessment and demonstration through industry staffed facility and equipment development projects,
- transfer of results, cooperative funding, and a defined schedule,
- the hurdles of funding, site selection, staffing, resistance to cooperation, and time.

The culmination of the efforts of the MCP were to be SEMATECH and the National Advisory

Committee on Semiconductors which are described in the following sections and each of which evolved directly from the MCP. Discussions and initiatives were continued into 1987 so as to observe the fruits of the efforts. The MCP then was dissolved.

SEMATECH

The actions of the MCP helped lead both industry and government into readdressing semiconductor industry competitiveness issues. The former was led by Charles Sporck, CEO of National Semiconductor Corporation, who, after being briefed on the MCP's findings and recommendations, made a convincing proposal for action to an SIA Board of Directors meeting in Boston in April of 1986. The Defense Science Board Task Force on Semiconductor Dependency was steered by Norman Augustine, a member of that body. These two activities arrived at similar conclusions and their recommendations merged. SEMATECH was the result. Some background on how this happened is both appropriate and interesting.

SRC's Manufacturing Competitiveness Panel solidified the industry position. It led to a finding that "The most prominent weakness of the U.S. industry lies in manufacturing. A realistic assessment is that the U.S. trails its Japanese competitors by at least two years in the ability to make high quality, cost-competitive products. A model is now being developed for this initiative in which government funding will be in an intensive effort to develop, demonstrate, and apply advanced manufacturing technology." (SRC Newsletter Vol. 4, No. 9, September 1986). The result was a decision by the SIA Board that, with Mr. Sporck's leadership, the planning of a cooperative manufacturing technology research effort should move forward.

In parallel, a Defense Science Board Task Force was organized in December of 1985 to assess the degree of dependence of military systems on semiconductor devices, the adequacy of domestic sources for such devices, the trends with respect to domestic supplies, fabrication capabilities for the required semiconductor devices, the ability of the U.S. industry to stay at the leading edge of the technology, and actions required to assure adequate supplies of semiconductor devices for defense systems. Norman Augustine, President, Martin-Marietta Corporation, a member of the Defense Science Board, was the chair. The SRC had two representatives on the task force, the members of which are listed in Table 11-4.

Table 11-4 DSB TASK FORCE ON SEMICONDUCTOR DEPENDENCY

Members and Advisors	
Chairman:	Norman Augustine, President, Martin-Marietta
Executive Secretary:	E.D. Maynard, Jr. OUSDRE
Members:	
Erich Bloch, Dir., NSF	Dr. Robert M. Burger, VP, SRC
Dr. Malcolm Currie, Pres., Delco	Dr. Richard DeLauer, Pres., Orion Group
Jack Kilby, Consultant	Gen. Robert Marsh (USAF Ret.)
Prof. James Meindl, Stanford Univ.	Dr. Walter Morrow, Dir., Lincoln Lab.
Lionel Olmer, Attorney at Law	Larry W. Sumney, Pres., SRC
Industry Advisors:	
W. Gianopulos, Dir. IBM Manassas Lab	Dr. George Heilmeier, Senior VP, TI
Dr. W. Howard, Jr., Sr. VP, Motorola	Adm. W.B. Inman, (USN Ret.),Pres.,MCC
Dr. R. Noyce, Vice Chair, Intel	M. Thompson, Ex.Dir. IC Proc., Bell Labs
Special DSB Advisor:	
Dr. Solomon Buchsbaum, Exec. VP, Bell Labs	
OSD Representatives:	
R. Donnelly, OASD/A&L	E. Westcott, USAF
Dr. W. Marquitz, OASD/C^{3}I	Lt. Gen. Emmet Paige, U.S. Army
Dr. Lawrence Gray, U.S.Navy	Col. Donald Fang, DSB
David Tarbell, OAS/ISA	
Working Group Members:	
Lt.Col. W. H. Freestone, OUSDRE	Dineene O'Connor, Palisades Institute
Tina Silverman, OASD/A&L	Dr. Richard VanAtta, IDA
Roderick Vawter, MDU	

The DSBTask Force responded with a series of hearings in 1986 during which industry and government representatives were heard and available information on defense requirements and industry status were considered. The conclusions were that the erosion of the U.S. leadership position in semiconductor technology was a serious problem that, if left unchecked, would limit defense capabilities in the future. Because technology leadership was (and is) fundamental to U.S. defense strategy, it was recommended that steps be taken to reverse the trends. It viewed the problem as being of the highest importance. The logic is presented in Table 11-5.

The recommendations of the DSB Task Force were to:

1. Support the establishment of a semiconductor manufacturing institute to develop, demonstrate and advance the technology base for efficient, high-yield manufacture of advanced semiconductor devices,
2. Establish, at eight universities Centers-of-Excellence for semiconductor science and engineering,
3. Increase DoD spending for research and development in semiconductor materials, devices, and manufacturing infrastructure by about 25 percent per year for four years,
4. Provide a source of discretionary funds to the Defense Department's semiconductor suppliers to underpin a healthy industrial research and development program.
5. Establish under the Department of Defense, a Government/Industry/University forum on semiconductors for assessment of the above program and to facilitate joint action on semiconductor research, development, and production.

Government participation in Sematech was the direct result of the first of these recommendations.

Table 11-5 DSB REASONING FOR SUPPORT OF IC R&D

- U.S. MILITARY FORCES DEPEND HEAVILY ON TECHNOLOGICAL SUPERIORITY TO WIN
- ELECTRONICS IS THE TECHNOLOGY THAT CAN BE LEVERAGED MOST HIGHLY
- SEMICONDUCTORS ARE THE KEY TO LEADERSHIP IN ELECTRONICS
- COMPETITIVE, HIGH-VOLUME PRODUCTION IS THE KEY TO LEADERSHIP IN SEMICONDUCTORS
- HIGH-VOLUME PRODUCTION IS SUPPORTED BY THE COMMERCIAL MARKET
- LEADERSHIP IN COMMERCIAL HIGH-VOLUME PRODUCTION IS BEING LOST
- SEMICONDUCTOR TECHNOLOGY LEADERSHIP WILL SOON RESIDE ABROAD
- U.S. DEFENSE WILL SOON DEPEND ON FOREIGN SOURCES FOR STATE-OF-THE-ART
- TECHNOLOGY IN SEMICONDUCTORS.
- THIS IS UNACCEPTABLE

Sematech was established by the semiconductor industry in August 1987 with government participation enabled by Congress in December of that year. During the formative period, SRC's President served as acting head of the Sematech start-up operations in Washington in order to provide a strong interface to the government. Sematech began operations in 1988 and continues today. The semiconductor manufacturing technology efforts of Sematech were supplemented by university based Sematech Centers of Excellence implemented through and managed by the SRC. From 1988 through 1996, Sematech provided the SRC with almost $85 million to support the centers and, at its peak in 1994, over 1/3 of the SRC budget was in support of these centers. Each center was designed to provide research in support of some form of manufacturing technology with

Table 11-6 SEMATECH CENTERS OF EXCELLENCE

Arizona: Contamination Free Manufacturing	Univ. of Arizona at Tucson	Sandia National Laboratories
California: Lithography	Univ. of California at Berkeley	Stanford University
Florida: Design for Manufacturability	Florida Institute of Technology Univ. of South Florida	Univ. of Florida
Massachusetts: Single-Wafer Processing	Boston University	Massachusetts Institute of Technology
New Jersey: Plasma Processing	David Sarnoff Research Center Princeton Plasma Physics Laboratory Rutgers Univ.	Princeton Univ. New Jersey Institute of Technology Stevens Institute of Technology
New Mexico: Semiconductor Metrology	Univ. of New Mexico Stanford Univ.	Sandia National Laboratories

Table 11-6 SEMATECH CENTERS OF EXCELLENCE (continued)

New York: Multilevel Metal	RENSSELAER Polytechnic Institute National Institute of Standards and Technology Sandia National Laboratories Univ. of North Texas	Colorado State University State University of New York at Albany
North Carolina: Automated Manufacturing	Duke Univ. Research Triangle Institute Univ. of North Carolina - Charlotte	North Carolina State Univ. Univ. of North Carolina - Chapel Hill Univ. of Illinois - Urbana-Champaign
Pennsylvania: Yield Enhancement	Carnegie Mellon Univ.	
Texas: Unit Processes & Mfg. Systems	Texas A&M Univ.	Univ. of Texas at Austin
Wisconsin: X-Ray Lithography	Univ. of Wisconsin - Madison	

the research focus given in Table 11-6. After the participation of the government ended in 1996, Sematech became an international organization that continues to advance the core technology involved in manufacturing ICs.

The initial purpose of Sematech was to restore the leadership of the U.S. semiconductor industry in integrated circuit manufacturing technology. By the middle of the nineties, this had been accomplished with little doubt that Sematech had played an important role in this recovery. The recounting of that is left to others.

NATIONAL ADVISORY COMMITTEE ON SEMICONDUCTORS (NACS)

> The DSB further stated that "Due to the national importance of the semiconductor industry's competitiveness to the nation's economy as a whole, it is recommended that an advisory group be established under OSTP ····to formulate a ···· strategy·····."

The multiplicity of government and industry efforts to restore the technology and market leadership of the U.S. semiconductor industry led to the creation of the NACS in 1988 as a direct result of efforts by the SRC. Its purpose was to devise and promulgate a national semiconductor strategy that would restore the leadership position of the U.S. semiconductor industry. It was to accomplish this purpose by examination of the technological, financial, and political issues affecting the semiconductor industry and to make recommendations to the government and industry on measures that would improve its competitiveness. The members of the NACS were appointed by the President with the process managed by the President's Office of Science and Technology Policy. The NACS membership, shown in Table 11-8, is for the full three-year term of the NACS. The industry membership was constant while the representatives from government varied. The NACS

held a series of meetings during which it gathered information on the state of the industry and considered measures tat would strengthened its competitiveness. Its findings and recommendations are contained in the series of reports given in Table 11-9. After three years, the NACS moved to terminate its operations expressing some frustration with respect to the response of the government to its recommendations.

A NACS initiative with lasting impact is the technology strategy process resulting from the Micro Tech 2000 Workshop. This workshop consisted of about 100 government and industry

Table 11 - 8 NATIONAL ADVISORY COMMITTEE ON SEMICONDUCTOR MEMBERSHIP

	Industry Members
Dr. Ian M. Ross (Chair)	President, AT&T Bell Laboratories
Dr. John A. Armstrong	VP for Science and Technology, IBM Corp.
Norman R. Augustine	Chairman and CEO, Martin Marietta Corp.
Robert. W. Galvin	Chairman of the Board, Motorola, Inc.
Jerry R. Junkins	Chairman, President and CEO, Texas Instruments, Inc.
James C. Morgan	Chairman and CEO, Applied Materials, Inc.
Charles E. Sporck	President and CEO, National Semiconductor Corp.
James G. Treybig	President and CEO, Tandem Computers, Inc.
Dr. Gordon E. Moore	Chairman, Intel Corporation
	Government Members
Honorable Robert B. Costello	Under Secretary of Defense for Acquisition, DoD
Honorable Erich Bloch	Director, National Science Foundation
Honorable D. Allen Bromley	Assistant to the President, Science & Technology Policy
Dr. Robert O. Hunter, Jr.	Director, Office of Energy Research, DoE
Honorable Thomas J. Murin	Deputy Secretary, DoC
Dr. James C. Decker	Asst. Director. Office of Energy Research, DoE
Dr. Charles M. Herzfeld	Director, Defense Research and Engineering, DoD
Dr. Robert M. White	Under Secretary for Technology, DoC
Dr. Eugene Wong	Assoc. Dir. for Physical Sciences & Engineering, OSTP
Honorable Frederick Bernthal	Acting Director, National Science Foundation
Honorable Walter E. Massey	Director, National Science Foundation
Dr. William Happer	Director, Office of Energy Research, DoE
Dr. Charles E. Adolph	Office of the Director, Defense Res. & Eng., DoD
	Executive Director
Dr. William R. Bandy	Program Manager, DARPA
Dr. Michael J. Kelly	Director, Defense Manufacturing Office, DARPA
Dr. Nicholas Naclerio	DARPA

technologists who together devised a 'roadmap' for microelectronics that could benefit the U.S. industry's competitiveness. The benefits of this to the industry were recognized and quickly resulted in the Semiconductor Industry Association accepting responsibility for its continued updating as described more fully in Chapter 6. The cooperative road-mapping process has become an important activity of the industry and has now been internationalized by the SIA. Lacking the roadmap, technology progress would be much more torturous

Table 11 - 9 NACS REPORTS

A STRATEGIC INDUSTRY AT RISK - 1989
PRESERVING THE VITAL BASE - 1990
CAPITAL INVESTMENT IN SEMICONDUCTORS - 1990
TOWARD A NATIONAL SEMICONDUCTOR STRATEGY - 1991
MICRO TECH 2000 WORKSHOP REPORT - 1991
ATTAINING PREEMINENCE IN SEMICONDUCTORS - 1992
A NATIONAL STRATEGY FOR SEMICONDUCTORS - 1992

MICROELECTRONICS ADVANCED RESEARCH CORPORATION (MARCO)

SRC has through the years become increasingly focused on needs identified by the industry managers on its Technology Advisory Board that are short range in nature. Recognizing the importance of long range research, the industry has created MARCO to support and manage the Focus Center Research Program (FCRP), a small number of multi-university research programs focused on longer range needs with the intent of identifying new concepts and radical alternatives to existing methodologies. MARCO is a wholly owned but separately managed subsidiary of the SRC with participation by the semiconductor industry; device manufacturers and their equipment and material suppliers and by the Department of Defense through DARPA. Representatives of these participants sit on a Governing Council.

At present, The FCRP funds and manages two Focus Centers - one in Design and Test with the University of California at Berkeley as the lead university and the second in Interconnect with the Georgia Institute of Technology leading the effort. Universities are participants in the Design and Test FCRP and six in the Interconnect FCRP. The funding of the two programs was over $5.1 million in 1999.

Two new focus centers have been approved for year-2000 initiation. One will perform research on materials, structures, and devices; while the second will focus on circuits, systems, and software.

CHAPTER 12

THE TECHNOLOGY MAZE

O what a tangled web we weave - it defies any rationale

Technology encompasses the spectrum of activities leading to the creation of useful products from scientific knowledge about information, materials, phenomena, and structures. This knowledge is derived from research that takes place in university, government, industry, and independent laboratories motivated by needs and curiosity, and limited by available resources. The diverse environments of this research are a strength and the results are often applicable in areas other than those intended. Often the research is not directed to any application beyond that of expanded knowledge but, even then, vigorous efforts are often made to identify applications in order to demonstrate value from the investments. From time to time, the efficiency of the overall process is questioned and attempts are suggested for restructuring in a more deterministic manner. These efforts are generally unsuccessful because the decision makers realize that the complexity of the technology maze may also be its strength.

This is not meant to justify the misdirection of research funding to achieve political or parochial purposes, nor to say that all research is productive. It is not. That is inherent in the processes of search and discovery. However, effective interactions among researchers help to identify and minimize this waste. In this short chapter, the nature of the technology maze as applied to technology in general and to semiconductor R&D in particular is examined.

GOVERNMENT SUPPORT OF R&D

The roots of modern technology are tangled. In the U.S., computing, transportation, communication, medicine, defense, agriculture, and manufacturing use technologies largely developed by industry but with roots in university and government research. In many cases government funding has been very important. Electronics is a good example. The key role of the government in the early development of radio, radar, television, and computers is unquestioned. The Department of Defense, in particular, maintained a strong program for basic and applied research in electronics that began in World War II, flourished through the sixties, and continued to make important contributions through the end of the century.. In the last decade, the DoD role has decreased as defense budgets have shrunk with the end of the Cold War.. At he end of the 20th

century, the relative importance of government funding of electronics R&D is at or near its nadir.

Major government funding of medical, agricultural, and transportation research continues. In these fields, the existence of large government organizations (two in transportation; NASA and DOT) are measures of their perceived relative importance In other fields, the government's role has become a lesser factor in applied research even though funding of the underlying science continues.

The appropriate role of government in technology is debated On one hand, inefficiencies and goal selection based on political factors support the thesis that the government's role should be minimal. On the other hand, in agriculture and health, for example, it is argued that the government has a fundamental obligation to support the research required for continued advances. Often the role is defined by the range of the research. It is argued that high-risk long-range research requires government funding while applications should be addressed by the private sector. Over the years, the role of the government in semiconductor research and development has been across the spectrum but now tends toward the long-range exploratory end.

The key role of government is the acquisition of resources through taxation and their distribution to achieve broad benefits. For R&D, this process is most efficient in the acquisition, less efficient in the distribution. Other means for amassing resources have been considered but the only practical means have been found in large corporations and voluntary cooperatives such as the SRC. Competition now limits the former.

Semiconductors are an enabling technology for advances in most if not all important economic sectors. Much of this importance derives from the increasing capabilities of computers and automata which have seen orders-of-magnitude growth in capabilities in the last four decades. It is difficult to identify any area of human activity that has not changed radically as a result. In agriculture, health, communication, banking, safety, and all other fields, semiconductor based or controlled tools have become ubiquitous. At some time, semiconductor advancement received significant funding from a variety of government organizations. For example, in the 1950ies, DoD had a major role in funding semiconductor research while, in the 1960ies, the major source of research support in universities for silicon device technology was from the National Institutes of Health. The Department of Energy, NASA, and other agencies have provided sporadic support while the National Science Foundation has provided continuing basic research support and variable applied research support. Government participation in the SRC has been beneficial but limited (See Table 8-4).

The major continuing contribution of the government to semiconductor technology lies in its

extensive support of basic research in universities. Funding of mathematics, physics, chemistry, and biology is essential for identifying future directions of integrated circuit technology both in terms of capabilities and applications. This foundation of fundamental research is strengthened further by engineering research enabled through government funding. This history of government support of research is a key element that differentiates US competitive efforts and leads to their success.

INDUSTRY SUPPORT OF SEMICONDUCTOR R&D

Today, U.S. semiconductor industry R&D exceeds $5 billion/year. How much is difficult to say simply because the line between R&D and product development is not rigidly defined nor is the line between semiconductor R&D and electronic product R&D. At least one company could well claim that their R&D budget exceeds that amount by itself. Regardless of the number there are certain well accepted characterizations of current semiconductor R&D including:

1. A majority of industry R&D investments are focused on near term product needs.
2. Government funding relating to semiconductors has decreased.
3. Industry R&D funding has not grown with the size of the industry.
4. The changing structure of the industry has depressed semiconductor R&D funding.
5. Long-range research 'beyond the shrink', is inadequate (The focus center program may correct this.)
6. The 'Roadmap' is providing an improved understanding of semiconductor R&D needs.

The big gain of the last several decades is the cooperative funding of, first, the SRC in 1982, then SEMATECH in in 1987, followed by the 'Roadmap' in 1992, and MARCO in 1998. These cooperative R&D initiatives have given the semiconductor industry the needed impetus for maintaining its rapid progress.

SEMICONDUCTOR RESEARCH IN UNIVERSITIES

University provide the major source of long-range research in the U.S. Despite their image of the "ivory tower' with its unbiased and unfettered independent research, in the sciences and engineering, university research is quick to respond to the goals defined of funding agencies. When the SRC initiated its research, it wakened a very large interest in silicon device technology in the universities with a ground swell that continued for a decade. This brought increased support of this technology from other funding sources - Federal government, state governments and internal funding by the universities - in recognition of the importance attached to this field by the industry and by the competition to participate. When the SRC budget stabilized in the decade of the nineties, this

leveraging effect gradually decreased and stabilized at a lower level. This continued government support benefits from the shared funding of significant research programs with NSF, DARPA, and DoE.

SRC research program has at times provided few competitive opportunities for new participants. This was a result of a stabilized or decreased research budget and recognition that a majority of the researchers capable of significant research were participants. As noted in Chapter 7, a number of research efforts have maintained SRC research support over the full life of the SRC. It recognizes that the attainment of worthy results in university research usually required several years of support before the output level stabilized and that shifting support creates periods of reduced output.

Another facet of SRC research is the difficulty in maintaining productive groups of researchers with coordinated goals. The university environment places considerable emphasis on independent research and thus making long-term collaborations difficult..

Chapter 13

LESSONS LEARNED

Unanimous decisions seldom result
in anything significant

Fourteen years of cooperative semiconductor research generates a plethora of lessons learned. Many of these lessons have been described in the previous chapters of this history. As with all such lore there is a high degree of uncertainty as to its transferability to other organizations or activities. The lessons have a short life, even in the friendly environment of the organization that gave them birth. They may be difficult to absorb, and you may have to live them to learn them. Finally, the lessons require actions that do not give substantive products.

The twelve lessons that seem most important are discussed in this chapter. Each lesson is presented as a brief essay. The subject of the lessons are listed below and they are described in the following pages.

1. Reasons for cooperation
2. Management of cooperation
3. Why join?
4. National versus international cooperation
5. Overhead expenses
6. Advice and advisory bodies
7. Measuring Research Performance
8. Government interface
9. Professional activities
10. University administration
11. Intellectual property
12. Cooperative Decision Processes

1. REASONS FOR COOPERATION

Cooperation among companies is based on the rationale that certain important needs can best be met by working with other companies with similar needs, even when companies compete. The need may be to accomplish something that costs more than a single company can afford, e.g., SEMATECH; or to present a united position to the government on issues affecting the industry, e.g., the SIA; or to fund research from which benefits diffuse rapidly, e.g., the S.C. In these cases, sharing the costs is an answer. This rationale has resulted in an expanding variety of cooperative activities in many industries. These range from product development and applied research, to addressing manpower needs, and to lobbying the government.

Semiconductor applied research is costly and the research results do diffuse rapidly. It meets the conditions for cooperation. Maintaining a research program to address the broad requirements for technological competitiveness in the semiconductor industry exceeds the resources of any one company. Moreover, since the results of long-range research are, by definition, for future application, their privacy cannot be assured in an open industry with high personnel mobility. In

SRC's experience, these arguments are weakened because, in the fast-moving semiconductor industry, cooperative research addresses some relatively short-term needs, computer-aided-design is a good example.

Performing cooperative long-range research in universities provides other benefits and penalties that are summarized in Table 13-1.

Table 13-1 ADVANTAGES (+) AND DISADVANTAGES (-) OF APPLIED UNIVERSITY RESEARCH

+ very capable students perform the research at low cost
+ few constraints are imposed on research directions
+ supervising faculty are generally recognized technology experts
+ broad interdisciplinary perspectives are provided in academia
+ engineering are eager to work closely with industry technologists
- academic research is required to disseminate results widely
- facilities, except computers, are generally poor
- management of research is weak
- universities have a confused intellectual property stance

U.S. semiconductor firms face rapid technological change, intense international competition, and reductions in the resources available for research. There exist few viable options other than cooperation. Government support for applied semiconductor research played an important role when the industry was small. It has decreased sharply as the industry has grown and is now being further reduced. Support of fundamental research by the National Science Foundation(NSF) has remained strong but, in general, is not driven by industry needs. NSF applied research programs are supporting high quality semiconductor research but have an uncertain future.

The bottom line is that the flow of knowledge essential for continued innovation in the semiconductor industry is now dependent primarily on industry. The industry has responded by cooperatively funding research through the SRC (1996 - $35M) and SEMATECH (1996 - $110M) with SRC being focused on long-range and SEMATECH on short-range needs. This strategy requires continuous review to maintain competitiveness. At present, there are many more users of the results, as well as employers of the well-trained university graduates, than there are supporters of the programs. This diminishes the effectiveness of cooperative research and, over time, may diminish the flow of research results available to the industry below that required to sustain progress.

The lesson - A robust cooperative is essential for providing the semiconductor industry with

a continuing ability to successfully advance its technology.

2. MANAGEMENT OF COOPERATION

Management of successful cooperative research requires a velvet glove. Who's in charge? How closely do we manage? The SRC functions between two generally strong camps - industry managers on its Board and TAB, and university faculty. Each has strong views on how to best direct, or not direct the research.

In the beginning, it was made clear that SRC management was responsible for the content and quality of the research program as well as the efficient operation of the SRC It was also made clear that this management must consider fully the inputs provided by SRC's governing and advisory bodies. SRC management has made its decisions under this guidance with remarkably few difficulties. This interactive process includes:

- balancing industry needs with university capabilities,
- providing appropriate level of programmatic leadership,
- avoiding excessive dominance by vocal members of advisory bodies,
- maintaining knowledge base of advisory groups,
- identifying programmatic decisions with 'SRC' instead of individual members,
- maintaining technical competence of SRC program managers,
- providing appropriate level of direction to university research managers, and
- transferring research products to users in member organizations.

The SRC has had difficulty in maintaining the proper balance between not-enough and too-much management of cooperative research. There exists a tendency to let TAB Science Committees make programmatic decisions and for the squeakiest wheel to get the grease. As member organizations and their representatives have changed, the learning curve is retraced and the skewing tendencies have been successfully dealt with. As the value of the research has become more evident the degree of selection that SRC members exercise is changing. Rather than defining goals and judging the program on the results, members are now in the process of selecting specific research efforts for a portion of their SRC fees. The impact of this new mode of operation will be determined over the next several years.

On the university side, there is less change. Students graduate but the faculty is relatively constant - more so than their industry counterparts. In the early stages of the program, the SRC established operational modes, e.g., accountability, real-time active dissemination, and goal-driven research, which were different from those of other research supporting organizations. To some universities, these have appeared to be onerous. Working with the University Advisory Committee,

the SRC has gradually reduced requirements for written reports and adapted research reporting to the electronic media, i.e., the SRC site on the World Wide Web.

There is a periodic tendency, derived from the technology roadmap experience, to define the results expected from the research. Such efforts are misdirected because, if the results are definable, then the effort is not research but development, and university efforts directed toward development are a poor use of the university capabilities.

The lesson - Management of cooperative research should be at the minimum level required to assure members that their technology needs are being addressed and that the results are being appropriately disseminated.

3. WHY JOIN?

The distinction between what nonmembers and members can acquire from cooperative research is a key and troublesome issue. The unique benefits associated with cooperation must be clear and substantial. In the SRC, benefits include the right to participate in:

- SRC events: reviews, workshops, technology transfer conferences, etc.,
- setting SRC's agenda and the priorities of the research program,
- interactions with other members in assessing technology needs and status,
- SRC's report dissemination system and the knowledge it provides,
- preferred identification of and contact with graduating students,
- technology interactions with government programs and organizations,
- positive interactions with universities, and
- continued assessment of semiconductor technology status.

It is important to understand that these rights require action on the part of the participant to become benefits. This is not automatic.

On the other hand, nonmembers can access SRC research in many ways. They can visit the universities that the SRC supports and be given access to research results, recruit students supported by the SRC, support research at the same universities with proximal advantages from SRC programs, and read published reports on SRC supported research. Non-members can gain many benefits from the SRC.

A closely related question is - If no company was a member of the SRC what difference would it make? In that case, SRC would not exist. Silicon integrated circuit related research would become rare in US universities as it was before the SRC was founded. Students with relevant skills would not be graduating and the flow of people and knowledge that now helps US companies

compete successfully would dry up. It could even be argued that over some period of time, the pace of industry advances would be slowed and the industry would assume more of the trappings of a mature industry. This becomes even more critical when industry requires new paradigms to replace lithography as the technology driver in the coming decade.

The dilemma thus presented is that the marginal impact of one company joining or not joining the SRC may be relatively small but the cumulative impact of a number of companies making the same decision can be very large. Governments require participation in actions for the collective benefit. Voluntary organizations such as the SRC cannot.

This is a real challenge for the SRC and for all similar organizations with no apparent easy solution. One industry leader once suggested that the government collect a tax from integrated circuit producers and transfer the proceeds directly to the industry for its collective R&D. That did not gain support.

In fact, the SRC has experienced the continued participation of a core group of the major US integrated circuit industry producers and several IC industry suppliers. Other companies have been members of the SRC over the last one and a half decades, many for limited periods. So long as the core group represents the bulk of US IC producers, the SRC is able to maintain a viable program. To date, this is the SRC experience.

The Lesson - Cooperative research in a free economy, no matter how important to an industry, will continually struggle to maintain support as long as non-members participate in its benefits without joining. This provides the SRC with a strong incentive for identifying exclusive benefits and is one reason the SRC has excelled.

4. NATIONAL VERSUS INTERNATIONAL COOPERATION

The rapid diffusion of SRC research results throughout the world and the potential for broader sharing of costs has, from time to time, led to consideration of foreign participation in the SRC. The SRC was originally chartered to accept international members on a fully reciprocal basis; they would be required to pay fees based on corporate worldwide IC sales and the home countries of foreign members would be required to provide full reciprocal access for US industry to its similar programs. These conditions were not met and no foreign company chose to participate in the SRC. With this less than enthusiastic response, the SRC Board of Directors decided, in 1983, to close this window. The by-laws were changed so that only US based companies with majority US ownership

would be eligible for SRC membership. At a later date, this was modified to permit participation by Canadian companies.

Subsequent discussions of international participation in the SRC, cited various reasons for maintaining an exclusive North American membership including those listed here.

- Foreign competition was the motivation for the creation of the SRC. Foreign participation would remove this motivation.
- With internationalization of the semiconductor industry, it is important to maintain an industry technology organization capable of dialoging with the US government on semiconductor technology issues. An internationalized SRC could not do this.
- Participation of government organizations in an internationalized SRC would become more difficult.
- Competition requires competitors. If the SRC were opened to international membership, and the larger companies joined, what would SRC be competing with?

In 1999, the continued internationalization of the industry and the need to cooperatively advance semiconductor technology in order to maintain the technology roadmap led the SRC to remove all barriers to foreign membership. This has redefined the goals of the SRC to focus on research, students, and technology transfer without reference to any geographically based advantages.

The Lesson - Relative advantage for its members is a prime motivating factor for the SRC. This advantage derives from member participation in the research planning process, member-focused research, student interactions, and through technology transfer efforts of the SRC. In addition, the nationalist policies of some countries continue to provide additional exclusivity for SRC membership.

5. OVERHEAD EXPENSES

The lesson learned about overhead expenses is perhaps obvious but merits discussion because of its pervasive impact on the operating modes of a cooperative activity. This discussion applies to overhead expenses of the SRC, not its research contractors, although universities could benefit from similar considerations. For the SRC, overhead can be defined as the percentage of the total budget that is used for operating expenses. The remainder of the total budget is programmatic, i.e., spent on research contracts.

Members were sensitive to the dangers of unbridled growth in non-programmatic costs from the initial days of the SRC and established goals for overhead expenses that became an important element in performance reviews. While initially about 10 percent of the SRC budget was allocated to overhead, in a few years it became set at 13 percent. This reflected the difficulty experienced in making industry assignees available for the SRC at the level originally contemplated. In the decade

and a half of its life, the 13 percent expense ratio ceiling has been essentially maintained. Several times the Board has experimented with different control algorithms for operating expenses but inevitably returned to the initial efficiency measure when difficulties were encountered.

A deviation from this limit is the Board approved 7 percent operating expense rate for SRC-managed external funding. This consists of research programs that are consistent with SRC goals for which funding is provided by government directly to the research organization without passing through the SRC. An example is state funding for research at a state university that is a cost share for an SRC research program at that university. This overhead exemption has provided SRC with the flexibility to undertake such activities for the benefit of the industry.

Certain types of activities that the SRC undertakes on behalf of its members are not directly associated with its university research program. These have included addressing industry competitiveness issues, support for the industry roadmap activities, funding of the SRC Competitiveness Foundation/SRC Education alliance, and other similar undertakings approved by the Board. For these types of activities and with Board approval, the associated costs are removed from the SRC overhead calculations.

The overhead rate ceiling has provided the SRC with the opportunity to demonstrate the efficacy of controlling management and management costs at a low level for cooperative research. At several times, the suggestion was made that a government research body was operating at a lower overhead rate but investigation revealed that this was not accurate. It was a product of the accounting methods employed to tabulate costs. When these were analyzed, SRC's overhead costs have always been significantly lower.

The challenge remains to balance within this limited overhead budget the various activities associated with the SRC program. The core research program consumes 87% of its budget and is the primary management function. This calls for a focus on technical management by SRC's research managers supported by the industry members on the Science TABs. Closely associated with the research program are dissemination activities including technology transfer, a variety of meetings, and the mentor program. A little further removed from the core activities are the administration of intellectual property rights, government relations, industry roadmap activities, maintaining a SEMATECH interface, SIA coordination, and a variety of other activities, all of which are 'good' but for which choices must be made. Obtaining the appropriate balance in these overhead operations is the key to successful management of cooperative research.

The Lesson - The imposition of a low overhead rate ceiling for operating the cooperative research program has required SRC management to optimize its operations through rigorous examination of the value of each function that it performs.

6. ADVICE AND ADVISORY BODIES

Cooperative research is by definition an amalgamation of the interests of funders and performers in which both are modified. Successful cooperative research reflects sufficient common ground that the modifications are neither extensive nor fundamental. In the SRC, the achievement of an operational mode and agenda that reflects this common ground is a continuing goal. The goal is elusive because the technology changes rapidly as industry advances rapidly through generations of increasingly sophisticated products.

SRC is fortunate in that it is provided with the best guidance available, not only from the industry that provides its resources but also from the participating universities and government organizations. The formal bodies that provide this guidance include: the SRC Board of Directors, the Technical Advisory Board(TAB) with its nine committees, the University Advisory Committee, and the Government Coordinating Committee. In addition, liaison is maintained with the SIA, SEMATECH, SEMI-SEMATECH, and other organizations with common interests. In addition, over 450 industry mentors advise the university researchers.

The challenge is to balance and modify the inputs from the various sources into SRC operations. There are conflicts. The Board is oriented toward long-range research while the orientation of the TAB is more short-range, largely because of their closer association with their company's current technology. University faculty are often pragmatic with poorly defined views of the future and of potential industry technical directions. Problems arise when industry representatives on the TAB seek to direct rather than advise the SRC on the research agenda. When this direction represents a consensus, SRC's response is usually positive. When the direction diverges from either the capabilities of the universities or collective sense of the TAB, then SRC must take the responsibility for deviating from it. There are many more opportunities for disagreement then there are right answers.

The Lesson - SRC managers must make decisions on research for the best collective benefit of the members recognizing that there are needs that cannot be addressed effectively by university research.

7. MEASURING RESEARCH PERFORMANCE

TAB science committees are asked to provide their evaluation of university performance on the various research tasks that they have helped define. The TAB evaluations are in the context of perceived industry needs, the status of industry technology, and the individuals competence in that specific technology. SRC research managers merge these evaluations with their assessments of the research, knowledge of the technology, broad SRC strategic goals, available SRC resources, and research priorities. The research manager makes a funding decision based on all of these considerations and presents it to the Research Management Committee(RMC) of the SRC for final approval. The RMC integrates the relevant information from all SRC research areas and the recommendations to provide the final funding decision. Since the research managers are experienced with both the RMC and the broad programmatic priorities, most decisions are consistent with the research manager's recommendations.

In the review and evaluation process, decisions are framed by many other similar decisions to produce results that are programmatically consistent and lead to a steadily improving research program. Each performer in the program is repeatedly evaluated based on 1) understanding of industry needs, 2) competence of research team, 3) past performance, 4) facilities, and 5) institutional support.

This methodology for measuring research performance is not perfect but it is probably as good as one can devise for this type of research program. It remains somewhat subjective and will thus vary among the different evaluators. The danger is that it is a process that does very well for short-term research with well defined measures of progress but less sell for long-range research for which results are less predictable.

The Lesson - Measurement of performance is difficult for research, more difficult for long-range research even when focused on specified needs. Competent reviews involving the judgements of the participants appears to be the best method of assessment.

8. GOVERNMENT INTERFACE

With admirable foresight, the founders of the SRC did not seek government participation in the SRC until its operating procedures were established. In 1985, the government was invited to participate and attention was given to an appropriate mechanism. The result was a Memorandum of Understanding(MOU) through the National Science Foundation(NSF) accompanied by grants

as funds were transferred from participating agencies to the NSF. This was initiated in 1986 with three government participants, the Department of Defense, the National Science Foundation, and the National Security Agency. It expanded to a maximum of seven agencies at any one time with those shown below participating.

Table 14-2 GOVERNMENT PARTICIPANTS IN THE SRC

Army Research Office
Defense Nuclear Agency
National Institute of Standards and Technology
National Science Foundation
National Security Agency
Naval Surface Warfare Center
Office of Naval Research (Office of Naval Technology)
Office of Under Secretary of Defense, Computer and Electronic Technology
Wright Laboratory, USAF

Through 1996, the government has provided 3.5 percent of SRC revenues through this MOU, but in one year, 1988, provided almost 19 percent of SRC revenues. Current reductions in budgets are reducing the participation. In 1996, government provided less than one percent of SRC revenues. The decrease is continuing. Thus, from a funding perspective, government participation in semiconductor cooperative research is no longer significant. In fact, the wide variations in support (see below) created management problems for the SRC. However, there is a value to this participation that extends beyond funding.

Table 13-3 GOVERNMENT FUNDING OF THE SRC VIA THE NSF MOU

1986	300,000	1992	850,000
1987	1,500,000	1993	810,000
1988	5,045,000	1994	433,650
1989	600,000	1995	343,100
1990	1,265,885	1996	234,795
1991	925,000		

The variations in funding are related to the multiple sources and the variety of decision-making processes involved. No one organization was responsible and the participation depended on key individuals in the organizations. Management of this process taxed the staff of the SRC out of proportion to its programmatic impact.

Beyond the funding, interactions with the agencies resulted in coordination of research

programs, research reviews, and information. Personnel from both communities participated in reviews and oversight activities of the other. One result is the jointly funded research effort at the University of Arizona on environmental, health and safety issues associated with semiconductor device manufacturing.

The fundamental question relating to government participation in the SRC remains unanswered. To what extent does government share responsibility for providing an environment in which its industry can successfully compete? So long as other governments actively assume a large responsibility for their industry's success, and the US does not, US industry is handicapped. Participation in cooperative industry activities is a method of industry support that is available to the government that benefits industry as a whole.

The Lesson - Government participation in cooperative research is an almost ideal method for government to support its industry's efforts to maintain competitiveness. To be effective, this participation must be consistent and free from bureaucratic entanglements.

9. PROFESSIONAL ACTIVITIES

A casualty of SRC's management style is the difficulty in maintaining professional activities. The SRC professional staff has never included more than 14 individuals with about half of these having their Ph.D. During its fourteen year history, fewer than 20 papers have been published by this staff and most of these were programmatic rather than technical. Early in the history of the SRC, attempts were made to provide staff with opportunities for involvement in research and publication. These attempts were aborted by the pressures associated with managing the research. The same strictures have deterred active participation in other professional activities. The priorities of the SRC are such that the university research program is number one and consumes all of the effort available. Second priority tasks are closely related to the research program and a small percentage of these are accomplished. Most everything else must be passed on.

The Lesson - In the environment of 20th century semiconductor technology, there is little opportunity to address other than the core activities. Those who succumb to diversions are rapidly left behind.

10. UNIVERSITY ADMINISTRATION

In working with universities, SRC has, at times, sought programmatic decision-making

mechanisms where none exists. Universities in their zealous pursuit of academic freedom, have burdened themselves with a bottoms-up management style that often limits their ability to participate in meaningful research. This management approach makes it difficult to form teams capable of addressing some of the most important issues and to acquire the facilities that are required for contemporary research. In SRC's experience, university programs and centers, in the absence of strong leadership, gain more cohesiveness from external direction than from internal management. Moreover, the existence of strong research teams is transitory so long as university reward systems continue to value individual research over research teams. These characteristics of universities have encouraged industry to seek new approaches to university research as it has become more important.

One reason for a less-than-perfect research management style is that research at universities takes second priority to education. This is as it should be. In attempting to increase the role of universities in the research required for maintenance of industry competitiveness, industry must work within or around these limitations.

The Lesson - Universities should not be asked to do all of the applied research required to maintain a competitive industry. They have more important tasks in providing well-educated scientists and engineers to staff the industry efforts, and in carrying out the long-range research that undergirds industry's applied research and development programs.

11. INTELLECTUAL PROPERTY

The appropriate distribution of intellectual property rights ensuing from SRC supported research has been a persistent issue, sometimes instigated by member companies, at other times by universities, and by the SRC in modifying its Contract-for-Research. The basic SRC objective has been to provide its members with unrestricted rights to apply SRC research results to their needs. Some universities have attempted to limit rights when pre-existing background intellectual property exists. Even when the SRC only asks for background rights in possession of the university or for identification of background intellectual property when a research contract is signed, this issue remains unresolved with several leading universities. The issues are often defined in other areas of technology and then applied to semiconductor research.

SRC's current position is that background intellectual rights issues have a low-probability of arising and therefore should be set aside until and if a real case appears. Some universities

apparently cannot except this resolution.

The Lesson - University administrations in coping with intellectual property issues develop positions that differ from those of industry, i.e., the SRC, especially with respect to background rights. These differences will have broad impacts on university-industry cooperative semiconductor research even though the policy may be based on issues from other research areas.

12. COOPERATIVE DECISION PROCESSES

One tenet of applied research is that factors external to the science or technology are included in prioritizing research. These externalities include industry needs, duplication and efficiency, applicability of potential results, ability of universities to contribute, timeliness, and economics. Since its founding, SRC has emphasized such factors in its program and, in doing so, has altered the style of many university researchers without decreasing their characteristic creativity. SRC through its goals in the beginning, and later through the semiconductor technology roadmaps, has defined the needs its research will address. During program reviews, it emphasizes the importance of all of the above factors in its cooperative program. SRC has been found university researchers receptive to this guidance and more productive because of it.

The paradigm through which university research is needs-driven as opposed to the knowledge-driven as with fundamental research is a key aspect of SRC research. The agenda of needs-driven research is shaped through industry-university interactions, and the SRC mentor program helps maintain the research on a course for maximum benefits to the industry.

The Lesson - The distinguishing feature of the SRC research program is its responsiveness to industry needs and the continuing interactions that assure that this feature continues as the first priority of the SRC. Every other action and activity must be measured by this standard.

CHAPTER 14

THE FUTURE

The semiconductor industry is changing. Of the 29 members of the SRC that are listed in the 1983 annual report, only ten remain in the 1999 report and two of these have changed their names. Foreign members may join the SRC and are doing so. The future of the SRC appears secure as it accommodates these changes and continues to serve the integrated circuit industry of the world.

The mission of the SRC has changed but not radically. In its first annual report in 1983, it stated its goals as:

> "to provide a scientific and technical information base for future industry development efforts and, in the course of this: (1) to provide a clearer view of limits, directions, opportunities, and problems in semiconductor technology; (2) to decrease the fragmentation and redundancy in U.S. semiconductor research; (3) to establish above-threshold research efforts for critical areas that require resources beyond those of many individual companies; (4) to enhance the image of the semiconductor industry: and (5) to strengthen university-industry ties."

The 1999 SRC annual report describes the mission of the SRC as:

"to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the ITRS, focusing on universities
- Relevantly educated university graduates
- Timely transfer of research results
- Strengthened university semiconductor technology capability through partnerships with members
- Collaboration to enhance commercialization and leveraged research."

These two statements are different but mostly in the wording and context. The latest does refer to the Roadmap and puts more emphasis on students.

The structure of SRC's research has changed. A significant portion of the research is now selected by individual member companies and thus is not fully integrated with the core research program. In addition, MARCO exists as a major long-range research activity managed by the SRC but with compartmentalized funding and a membership that differs from that of the SRC's core research program. However, this compartmentalization of industry supported semiconductor research has in the first instance increased member company involvement in the research and in the second instance has provided new funding and counteracted the continued trend of the core program to short-range objectives. At the same time, these decrease the core research budget which make coordinated responses to the 'Roadmap' somewhat more difficult to achieve.

The structure of the SRC will be increasingly impacted by the trend toward

internationalization. In the near future, it can be expected that the research program will include foreign participants. This will be complicated by the structure of university research in other countries and may cause SRC research to expand beyond the academic realm. It has tested this in the U.S. with research in university associated not-for-profit research laboratories but to a limited extent.

APPENDIX A

PERSONS
WHO HAVE MADE THE
SRC SUCCESSFUL

CHAIR - BOARD OF DIRECTORS

Erich Bloch	IBM	1982-4
Eugene Flath	Intel	1984
George Scalise	AMD	1984-6
Klaus Bowers	AT&T	1987
Robert McMillin	GMC/Delco	1988-9
Frederic N. Schwettmann	HP	1990
Gerald H. Parker	Intel	1991
Owen Williams	Motorola	1992
William Siegle	AMD	1993
Dan Fleming	IBM	1994
Owen Williams	Motorola	1994-5
Charles Carinalli	National	1996
Mark Melliar-Smith	AT&T	1996
Don Wollesen	AMD	1997
George Bodway	HP	1998
Michael Polcari	IBM	1999

INDUSTRY CO-CHAIR - TECHNICAL ADVISORY BOARD (and EXECUTIVE TAB)

L. David Sikes	Motorola	1982
J. Phillip Downing	AMD	1983
James M. Daughton	Honeywell	1984
Court Skinner	National	1985
Dragan Ilic	HP	1986
Stanley V. Jaskolski	Eaton	1987
Pallab Chatterjee	TI	1988
John R. Carruthers	Intel	1989
Edward L. Hall	Motorola	1991
Steven Knight	AT&T	1992
Robert R. Doering	TI	1993
Donald L. Wollesen	AMD	1994
Ashok Kapoor	LSI Logic	1995
John M. Pierce	National	1996
James Duley	HP	1997
Robert R. Doering	TI	1998
Steven J. Hillenius	Lucent	1999

MEMBERS- BOARD OF DIRECTORS

Erich Bloch	IBM	1982 - 1984
Johan F. Blokker	Hewlett Packard	1982 - 1984
Eugene J. Flath	Intel Corp.	1982 - 1984

Gregory Harrison	National Semiconductor	1982 - 1984
Bob J. Jenkins	Motorola	1982 - 1989
Jeffrey C. Kalb	Digital Equipment	1982 - 1986
John W. Lacey	Control Data	1982 - 1984
K. Carl Nomura	Honeywell	1982 - 1984
Joseph C. Ross, Jr.	Micro Mask	1982 - 1984
Carmelo J. Santoro	Silicon Systems	1982 - 1986
George M. Scalise	Advanced Micro Devices	1982 - 1984
ex officio	Semiconductor Industry Assoc.	1999 -
Larry W. Sumney	SRC	1984 -
Michael J. Callahan	Monolithic Memories	1984 - 1985
	Advanced Micro Devices	1988 - 1989
Jon E. Cornell	Harris	1984 - 1987
Brian A. Hegarty	Honeywell	1984 - 1984
Parl R. Low	IBM	1984 - 1986
Fred Schwettmann	Hewlett Packard	1984 - 1993
Tim B. Smith	Texas Instruments	1984 - 1984
Klaus D. Bowers	AT&T	1985 - 1987
Michael J. Thompson*	AT&T	1985 - 1986
Anthony B. Holbrook*	Advanced Micro Devices	1985 - 1986
Duane Dickhut*	Digital Equipment	1985
James E. Dykes	General Electric	1985 - 1986
Stephen W. Michael*	General Electric	1985
Robert J. McMillin	General Motors	1985 - 1989
Nils L. Muench*	General Motors	1985 - 1988
Thomas J. Sanders*	Harris	1985 - 1988
Chuck E. Tyler*	Hewlett Packard	1985 - 1986
William T. Siegle**(1989)	IBM	1985 - 1989
	Advanced Micro Devices	1990 - 1994
Gerald Parker	Intel	1085 - 1993
Robert N. Noyce*	Intel	1985 - 1987
Paul A. Tierney	Monsanto	1985
David L. Keune*	Monsanto	1985
W. J. Kitchen*	Motorola	1985 - 1992
James B. Owens Jr**(1990)	National Semiconductor	1985 - 1992
G. R. Mohan Rao	Texas Instruments	1985 - 1993
Dennis D. Buss*	Texas Instruments	1985 - 1986
Robert B. Palmer**(1987)	Digital Equipment	1986 - 1989
Richard A. Santilli*	General Electric	1986

MEMBERS- BOARD OF DIRECTORS (continued)

E. Randy Parker	National Semiconductor	1986 - 1989
Steve Cooper	Silicon Systems	1986
Joseph S. Mathias	Sperry	1986
Gaynor N.Kelly	Perkin-Elmer	1986 - 1987
Arnold Miller	Xerox	1986
Bruce R.Darnall*	AT&T	1987

William C.Robinette, Jr.	Digital Equipment	1987 - 1989
Kenneth A. Pickar	General Electric	1987 - 1989
John Herman III*	General Electric	1987 - 1989
Jack Anderson*	Hewlett Packard	1987 - 1990
Brian Hegarty	Honeywell	1987 - 1988
Sanford L. Kane	IBM	1987 - 1988
Frank Michelletti	Rockwell International	1987
Gilbert F. Amelio*	Rockwell International	1987
Gregory J. Armstrong	Texas Instruments	1987 - 1992
David A. Huchital	Perkin-Elmer	1987 - 1987
Michael J. Thompson	AT&T	1988 - 1989
David J. Lando*	AT&T	1988 - 1992
J. Phillip Downing*	Advanced Micro Devices	1988 - 1989
Samuel Musa	E-Systems	1988 - 1989
Charles J.Nuese**(1989)	Harris	1988 - 1990
Jack Anderson	Hewlett Packard	1988 - 1990
Tony Jurvetson	Varian Associates	1988 - 1989
Ira Weissman	Varian Associates	1988 - 1989
Gene Strull	Westinghouse Electric	1988 - 1989
John M. Walker*	Westinghouse Electric	1988 - 1989
Mounir M. Kamal*	General Motors	1989 - 1989
C. Mark Melliar-Smith	AT&T	1990 - 1995
	Lucent Technologies	1996
ex officio	SEMATECH	1997 -
Thomas F. Gannon	Digital Equipment	1990 - 1998
Llanda Richardson**(1998)	Digital Equipment	1990 - 1993
		1998
Jack F. Strange	E.I. du Pont de Nemours	1990 - 1992
Donald B. Rogers*	E.I. du Pont de Nemours	1990 - 1992
Stanley V. Jaskolski	Eaton	1990 - 1992
Walter R. McIndoo	General Motors	1990 - 1992
Linos J. Jacovides*	General Motors	1990 - 1992
Donald F. Reilly	IBM	1990
Dan J. Fleming** (1991)	IBM	1990 - 1993
Joseph L. Parkinson	Micron Technology	1990 - 1992
Eugene H. Cloud*	Micron Technology	1990 - 1992

MEMBERS- BOARD OF DIRECTORS (continued)

Owen Williams	Motorola	1990 - 1997
Phillip M. Neches	NCR	1990
J. H. Van Tassel	NCR	1990
Bami Bastani	National Semiconductor	1990 - 1992
Robert Holzel	Varian Associates	1990
Richard M. Levy	Varian Associates	1990
Rajinder P. Khosla	Eastman Kodak	1991 - 1994
Bruce C. Burkey*	Eastman Kodak	1991 - 1992
Peter A. Younger	Eaton	1991 - 1992
Jeffrey D. Peters	Harris	1991 - 1994
Thomas L. Haycock*	Harris	1991 - 1992

Dragan Ilic*	Hewlett Packard	1991 - 1992
Lowell D. Deckard	NCR	1991 - 1992
Daniel L. Ellsworth*	NCR	1991 - 1992
Charles Carinalli	National Semiconductor	1993 - 1995
George Bodway	Hewlett Packard	1993 - 1999
Pallab K. Chatterjee	Texas Instruments	1993 - 1994
Walter Class	Eaton	1993 -
Thomas Halloran	Etec Systems	1993
Lester Wilkinson	Delco Electronics	1993
Joseph M. Zelayeta	LSI Logic	1993 - 1996
Sunlin Chou	Intel	1994 -
Michael Polcari	IBM	1994 -
Claudine Simson	Northern Telecon	1994 - 1996
Bruce C. Burkey	Eastman Kodak	1995 - 1998
Mike Fitzpatrick	Westinghouse Electric	1995 - 1996
	Northrup Grumman	1997 -
Dyer A. Matlock	Harris	1995 - 1998
Yoshio Nishi	Texas Instruments	1995 - 1998
Don Wollesen	Advanced Micro Devices	1995 -
Richard S. Hill	Novellus Systems	1996 -
Court Skinner	National Semiconductor	1996
Sherry Gillespie	Motorola	1997 -
Gobi R. Padmanabhan	National Semiconductor	1997 - 1999
Mark Pinto	Lucent Technologies	1997 -
Richard Schinella	LSI Logic	1997 -
David N. Nichols	Eastman Kodak	1998 -
Addshwin Shah	Texas Instruments	1998
Dan Casaletto	Compaq	1999 -
Michael Jayne	Intersil	1999 -
Hans Stork	Hewlett Packard	1999 -
Mohan Yegnashankaran	National Semiconductor	1999 -

* Alternate ** From alternate to member

INDUSTRY RESIDENT MANAGERS

Benjamin J. Agusta	IBM	1983-4	Microstructure Sciences
Richard A. Lucic	HP	1983-4	Manufacturing Sciences
James R. Key	CDC	1983-5	Technology Transfer
John J. Cox	DuPont	1984-5	Packaging
Patrick W. Wallace	DuPont	1984	Packaging
Jeffrey A. Coriale	Harris	1984-7	CMOS - BiCMOS
Shakir A. Abbas	IBM	1985-7	Bipolar/reliability
Phillip A. Lutz	GM-Delco	1986-8	Packaging
Norman F. Foster	AT&T	1987-9	Manufacturing/Reliability
C. Edward Holland, Jr.	DoD	1987-9	Government Coordinating
Kenneth L. Pocek	Intel	1988-90	Design Sciences
Jeffrey L. Hilbert	Motorola	1988-89	Design Sciences
Vincent J. Lyons	IBM	1988-89	TECHCON'88
John E. Gragg	Motorola	1988-90	Microstructure Sciences
Syed Rizvi	TI	1989-91	Microstructure Sciences
Peter Verhofstadt National	1989-90	Microstructure/Design Sc.	
John Kelly	IBM	1989-90	Packaging
Mike Witty	GM-Delco	1991-4	Microstructure Sciences

Ray McMahon	TI	1991-3	Manufacturing Process Sc.
Justin E. Harlow III	National	1990-	Design Sciences
Vivek Bissessur	Intel	1994-	Interconnect/Bulk Processes
Don Sharfetter	Intel	1995-6	Modeling/Simulation CRADA
Dirk Bartelink	HP	1995-	Technology Strategy/Planning
Ron Goossens	National	1995-98	CSMS Liaison

CHAIRS - UNIVERSITY ADVISORY COMMITTEE

Andrew J. Steckl	RPI	1982-4
David Hodges	UCB	1985-6
Stephen W. Director	CMU	1987-8
Kensall D. Wise	Michigan	1989-90
Nino A. Masnari	NCSU	1991-2
Timothy N. Trick	Ill	1993-4
Joseph Ballantyne	Cornell	1995-6
Rob Maziar	Minesota	1999-00

CHAIRS - GOVERNMENT COORDINATING COMMITTEE

Kermit Speierman	NSA	1986-92
Gerald Iafrate	ARO	1993-96

UNIVERSITY RESIDENT MANAGERS

John Prince	Arizona	1988-9	Packaging
Dahua Kolbas	NSCU	1995-6	Microstructure Sciences
Mike Littlejohn	NCSU	1995-6	Technology Planning

TECHNICAL ADVISORY BOARD COMMITTEE CHAIRS

Chair - Design Sciences TAB

Michael U. Winbrow	Silicon Systems	1982
James M. Daughton	Honeywell	1983
Kenneth Slater	DEC	1984
Wally B. Edwards	CDC	1985
Alan A. Anderson	IBM	1986
Pallab Chatterjee	TI	1987
W. Terry Coston	Harris	1989
Paul J. Ainslie	GM/Delco	1988
William R. Griffin	IBM	1991
Kenneth Ray	Motorola	1992
Tom Jones	National	1993
Richard Byrne	MITRE	1994
W. Terry Coston	Cadence	1995
Ray Abrishami	LSI Logic	1996

Chair - Environment, Safety, & Health Sciences TAB

H. Ray Kerby	SEMATECH	1995

Chair - Factory Sciences TAB

Darius Rohan	TI	1995
John S. Wenstrand	MicroUnity Systems	1996

Chair - Manufacturing Process Sciences TAB

William E. Starks	Varian	1990-1
P. B. Ghate	TI	1992
Ronald P. Kovacs	National	1993
Thomas R. Bowers	AMD	1994

Chair - Manufacturing System Sciences TAB

Richard C. Donovan	AT&T	1990-1
E. Hal Bogardus	IBM	1992-4

Chair - Lithography Sciences TAB

Steven D. Berger	AT&T	1994
Gene E. Fuller	TI	1995
George A. Gomba	IBM	1996

Chair - Manufacturing Sciences TAB

Robert M. Brill	Harris	1982
Billy Lee Crowder	IBM	1983
Moiz M. Beguwala	Rockwell	1984*
Stanley V. Jaskowski	Eaton	1985-6
Donald F. Reilly	IBM	1987-8
Ronald K. Reger	GM/Delco	1989

* - less than full term

Chair - Interconnect Sciences TAB

David B.Fraser	Intel	1995
Darrell M. Erb	AMD	1996

Chair - Materials and Bulk Processes Sciences TAB

Baylor Bunting Triplett	Intel	1995
Allen Bowling	TI	1996

Chair - Packaging Sciences TAB

David J. Lando	AT&T	1985-6
Kenneth M. Brown	DEC	1991-2
James D. Hayward	AMD	1993
William T. Chen	IBM	1994
Kenneth M. Brown	DEC	1995
Luu Nguyen	National	1996

Chair - Process Integration and Device Sciences TAB

John M. Aitken	IBM	1995
Monir El-Diwany	National	1996

Chair - Microstructure Sciences TAB

Michael J. Callahan	Monolithic Memories	1982
L. David Sikes	Motorola	1983
G. R. Mohan Rao	Texas Instruments	1984
Dragan Ilic	Hewlett-Packard	1985
H. J. Levinstein	AT&T	1986
Marvin Garfinkel	General Electric	1987
A. L. Rivoli	Harris	1988
David E. Moss	GM/Delco	1989
John M. Pierce	National	1990
Michael Garner	Intel	1991
Ron Das	AMD	1992
Clarence J. Tracy	Motorola	1993
Clarence W. Teng	TI	1994

Chair - Technology Transfer TAB

Tom L. Haycock	Harris	1987
Philip J. Fleming	HP	1988
Michael R. Poponak	IBM	1989
James N. Smith	Motorola	1990
Ken VanBree	HP	1991-2
W. Dale Edwards	Harris	1993
Mahboob Khan	AMD	1994
John Pankratz	TI	1995
Graham Alcott	Intel	1996
Shirley Laine	Digital	1997
Ken Ports	Harris	1998

Co-chair - Computer Aided Design & Test Sciences Coordinating Committee

Sury Maturi	LSI Logic	1999

Chair - Integrated Circuit and System Sciences Coordinating Committee

Shishpal Rawat	Intel	1999

Chair - Material and Process Sciences Coordinating Committee

Clarence Tracy	**Motorola**	**1999**

Chair - Back end Processes TAB

John A. Mucha	**SEMATECH**	**1999**

Chair - Environmental Safety and Health TAB

Robert Duffin	**SEMATECH**	**1999**

Chair - Value Chain TAB

Ken Ports	**Harris**	**1999**

Co-chair - Student Relations TAB

Michael Sampogna	**IBM**	**1999**

Chair - Patterning TAB

Alex Liddle	**Lucent Technologies**	**1999**

Chair - Nanostructure and Integration Sciences Coordinating Committee

Brian Doyle	**Intel**	**1999**

Chair - Advanced Devices and Technologies TAB

Brian Doyle	**Intel**	**1999**

Chair - Factory Systems TAB

Mohammad Ibrahim	**National**	**1999**

Chair - Packaging and Interconnect Systems TAB

James Hayward	**AMD**	**1999**

Computer-Aided Design and Test Sciences
Integrated Circuits and System Sciences
Materials and Process Sciences
Nanostructure and Integration Sciences

CHAIR - CENTER FOR SEMICONDUCTOR MODELING AND SIMULATION TECHNICAL ADVISORY BOARD

David C. Cartwright	LANL	1995-
William C. Holton	SRC consultant	1995-
Don Scharfetter	Intel	1995
Ronald Goossens	National	1996

CHAIR - CSMS Bulk Processes Thrust

Hamid Soleimani	DEC	1995
Rex E. Lowther	Harris	1996-

CHAIR - CSMS Device Thrust

Ronald Goossens	National	1995
Philip Oldiges	DEC	1996-

CHAIR - CSMS Interconnect Performance Prediction Thrust

Ashok Kapoor	LSI Logic	1995-

CHAIR - CSMS Interconnect Reliability Thrust

Bob Rosenburg	IBM	1996-

CHAIR - CSMS Grid Thrust

R. Kent Smith	AT&T	1995-

CHAIR - CSMS Topography Thrust

Paco Leon	**Intel**	**1995-**

APPENDIX B

SENIOR TECHNICAL STAFF OF THE SRC

NAME	TITLE	TENURE	TERM
Larry W. Sumney	-> Exec.Director	18	82-
	-> President (84)		
	-> President/Chief Executive Officer (93)		
Richard D. Alberts	-> Senior Officer for Policy and Planning	2	82-84
	-> Staff VP for Policy & Planning (84)		
Robert M. Burger	-> Chief Scientist/Senior Technical Officer	14	82-96
	-> Staff VP/Research (84)		
	-> Staff VP/Chief Scientist (87)		
	-> VP/Chief Scientist (90)		

Benjamin J.Augusta IBM	-> Prog. Mgr., Microstructure Sciences	2	83-84
Ralph K. Cavin III	-> Director, Design Sciences (83)	7	83-89
	-> Vice President, Research Operations	4	96-
Richard Lucic	-> Prog.Mgr., Manufacturing Sciences	1(HP)	83-84 86-90
James R.Key Control Data	-> Prog.Mgr., Technology Transfer	2	83-84
Michael D. Connelly	-> Manager, Information Systems	17	83-
	-> Senior Manager, Information Systems (89)		
	-> Director, Information Systems and Services (91)		

William C. Holton	-> Director, Microstructure Sciences	13	84-96
	-> Senior Director, Microstructure Sciences (89)		
	-> Vice President, Research Operations (91)		
Richard D. LaScala	-> Manager, Contracts and Grants	16	84-00
	-> Manager, Member Services and Communication (91)		
D. Howard Phillips	-> Director, Manufacturing Sciences	8	84-93
	-> Senior Director, Corporate Development & Government Relations (89)		
	-> Vice President, Marketing & Member Relations (91)		
Jeffrey A. Coriale Harris	-> Prog.Mgr., Microstructure Sciences	2	84-86
John J. Cox duPont	-> Prog.Mgr., Packaging	1	84
Patrick W. Wallace duPont	-> Prog. Asst., Packaging	2	84-85

NAME	TITLE	TENURE	TERM
Shakir A. Abbas IBM	-> Prog.Mgr., Microstructure & Manufacturing Sciences	2	85-86
Phillip A. Lutz General Motors	-> Prog.Mgr., Manufacturing Sciences	2	86-88
James F. Freedman	-> Director, Research Integration -> Staff Vice President, Research Integration(89) -> VP, Research Integration(90) -> VP, Research Integration & Technology Transfer(93)	11	87-98
Norman F. Foster Bell Labs(87-88)	-> Prog.Mgr., Manufacturing Sciences -> Director, Manufacturing System Sciences (89) -> Director, Information Transfer (94)	4	87-91
Linda L.Gardner	-> Manager, Intellectual Property -> Senior Manager.Intellectual Property (89) -> Director Administrative Operations (91)	11	87-98
Jeffrey L. Hilbert Motorola	-> Prog.Mgr., Design Sciences -> Director, Design Sciences (89)	3	87-90
C. Edward Holland DoD (87-88)	-> Manager, Governmental Affairs -> Director, SEMATECH CoE Program (89)	3	87-90
Kenneth L. Pocek Intel	-> Prog.Mgr., Design Sciences	3	87-90
J. Richard Burke	-> Prog.Mgr., Manufacturing Sciences -> Director, Manufacturing Process Sciences (89)	2	88-90
John Prince U.of Arizona	-> Visiting Scientist	1	88-89
John E.Gragg Motorola	-> Prog.Mgr., Microstructure Sciences	2	88-90
Peter Verhofstadt National (88-90)	-> Prog.Mgr., Microstructure Sciences -> Director, Design Sciences(91) -> Executive Vice President and Chief Scientist(94)	12	88-
John H.Kelly IBM;	-> Prog.Mgr., Manufacturing System Sciences -> Director, Packaging Sciences	3 2	89-90 93-95
Syed Rizvi TI	-> Prog.Mgr., Manufacturing Process Sciences	2	89-90
William T.Lynch	-> Director, Microstructure Sciences -> Director, Process Integration & Device Sciences & Materials & Bulk Process Sciences (95)	7	90-97
Justin E.Harlow III NSC (90-97)	-> Prog.Mgr., Design Sciences -> Program Manager,	10	90-

	----------		
Daniel J. C. Herr	-> Director, Manufacturing Process Sciences & Lithography Sciences -> Director, Environment, Safety & Health Sciences & Lithography Sciences(95)	7	93-
	----------		
William Atkins	-> Director, Factory Sciences & Interconnect Sciences	2	94-97
Dirk Bartelink HP	-> Visiting Scientist	2	94-96

Ronald C. Bracken	-> Director, Packaging Sciences	4	95-99
Vivek Bissessur Intel	-> Prog.Mgr.,	4	95-99
Ron Goossens NSC	-> Prog.Mgr. CSMS	2	95-97
Mike Littlejohn NCSU	-> Visiting Scientist	1	95

Ronald Gyurcsik	-> Director, Factory Sciences	1	96
Dinesh Mehta	-> Vice President, Administrative Operations and Strategic Initatives	4	96-
E. D. Maynard	-> Executive Vice President, Gov.Affairs	2	98-

Average tenure 5.9 years

APPENDIX C

SRC RESEARCH CONTRACTS

Annual Funding Level

A <$50K $50K ≤ B <100K $100K ≤ C <$200K $200K ≤ D <$400K
$400K ≤ E <$800K $800K ≤ F <$1,600K $1,600K ≤ G <$3,200K

Will vary over term of contract - Indicates approximate size of effort

NOTE: In this listing of contracts, there are gaps in the sequence of contract numbers because small awards are not included. These include special awards for graduate students to finish their thesis research after completion of the research effort on which they had been supported, for travel grants, for preparation of white papers, for one-time equipment grants, and for other similar functions that generally were small and of peripheral consequence to the research.

SRC # Funding	Title (File number of related contracts)	Principal Investigator(s)	University Term or Start Date
82/01 F	Microscience and Technology (69)	J. Frey N. MacDonald	Cornell 1982
82/02 C	Performance Enhancement Using Cooling (64)(103)	R. Pease	Stanford 1983-
82/03 B	Transfer of Software Methodology to VLSI Design	F. Brooks	UNC 1982-84
82/04 B	Low Resistance Ohmic Contacts for VLSI	G. Robinson	Minnesota 1983-84
82/05 C	Multilevel Interconnection and Reactive Ion Source	T. Wade	Miss. St. 1983-85
82/06 B	Vapor Phase Film Growth	J. Greene	Illinois 1983-96
82/07 E	Center for Computer Aided Design (68)	S. Director	CMU 1982-96
82/08 G	Computer Aided Design	D. Peterson D. Hodges, R. Brayton	UC/Berkeley 1982-94
	---		
03 C	Design Automation System for Speed Independent VLSI Circuits	S. Reddy	Iowa 1983-86
04 B	Mechanical-Environbmental Inter-actions in VLSI Bond Interfaces	B. Livesay	Ga Tech 1983-85
05 B	Ultra-Compaction Algorithms for Symbolic VLSI Layouts	J.Rosenburg	MCNC 1983-84
06 C	Multilevel Interconnections and Contacts for Sub-Micron VLSI	K. Saraswat	Stanford 1983-88
07 B	CVD of Refractory Metals and Their Silicides	J. Fordemwalt	Arizona 1983-85
08 B	Incoherent Light & Laser Annealing	R. Kwor	Notre Dame 1983-86
09 C	Complementary MESFET Devices	J. Plummer	Stanford 1983-86
10 C	Thermal Nitridation of Silicon and Silicon Oxides	R. Tressler J. Monkowski	Pa State 1983-86
11 C	Polysilicon in Advanced Integrated Circuit Processes	D. Greve	CMU 1983-87

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
12 C	Bipolar Transistor Structures	B. Wilamowski R. Mattson	Arizona 1983-84
13 C	Design Verification and Testing of VLSI Circuits	T. Trick	Illinois 1983-84
14 C	Design of Testable VLSI	J. Abraham	Illinois 1983-96
15 C	Very Low Temperature Silicon Epitaxy	R. Warner, Jr.	Minnesota 1983-86
16 B	MOS VLSI at Low Temperature (93)	R. Anderson	Vermont 1983-87
17 C	CAD Methodology for Analog LSI/VLSI	P. Allen	Tx A&M 1983-85
18 B	Radiation Effects in MOS Devices (79)	T. Ma	Yale 1983-96
20 C	Three Dimensional VLSI Device Simulator	L. Akers	Ariz. St. 1983-86
21 B	MBE Silicides for VLSI Applications (88)	K. Wang	UCLA 1983-96
22 B	On-Line Testable VLSI Processors (68)	J. Shen	CMU 1983-86
23 B	VLSI Digital Signal Processors	M. Yuschik	So. Car. 1983-84
24 B	Acoustic Microscopy	R. Mueller	Minnesota 1983-86
25 C	Scanning Electron Microscopy (83)	R. Propst	No. Car. 1983-87
26 B	Plasma/RIE with Flourine Compounds	J. Stach B. Golja	Pa State 1983-85
27 B	High Conductivity Silicides	M. Lagally	Wisconsin 1983-86
28 C	CAD for VLSI Layout	E. Kinnen	Rochester 1983-86
29 C	Laser Repair of Mask Microfaults	S. Allen	So. Calif 1983-87
30 C	Reliability Physics	C. Sah	Illinois 1983-88
31 C	Si/SiO_2 Interface States	C. Bates	Stanford 1983-86
32 B	Hierarchical Silicon Compilation (84)	J. Savage	Brown 1983-88
33 E	Microstructure Sciences (80)	P. Penfield, Jr. R. Reif	MIT 1983-96
34 B	Cluster Ions	K. Bowen, Jr.	Johns Hopkins 1983-87
35 C	VLSI Arrays	F. Preparata	Illinois 1983-84

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
36 C	Thin Insulators/Interfaces (79)	R. Barker	Yale 1983-86
37 B	Optimization of Polysil Emitters	D. Burke	Florida 1983-85
38 B	Simulation of MOS ICs	O. Palusinski	Arizona 1983-86
39 B	Growth Kinetics of Thin Insulators and Interface Defects	R. Raj	Cornell 1983-86
40 E	Low Temperature Processing (76)	C. Osborn	MCNC 1983-88
41 F	Advanced Beam Systems Hydrogen in Deposited Oxides	A. Steckl S. Murarka	RPI 1983-91
42 D	VLSI Reliability (82)	J. Lathrop	Clemson 1983 -
43 B	Oxygen Induced Defects/Internal Gettering	H. Gatos	MIT 1983-87
44 E	GaAs Digital Research	J. Merz	UC/SB 1984-88
45 D	Automation in Semiconductor Mfg. (85)	K. Wise	Michigan 1983-96
46 F	Mfg. Science & Tech. for VLSI	J. Meindl	Stanford 1984
47 C	GaAs Digital Device Research	J. Harris R. Dutton	Stanford 1984-88
48 B	Low Resistance Ohmic Contacts	G. Robinson	Col. St. 1984-86
49 E	VLSI Systems: Architecture and Reliability	J. Abraham T. Trick	Illinois 1984
50 D	VLSI Packaging and Interconnections (86)	J. Prince	Arizona 1984-96
51 C	Multilevel Analog IC CAD (91)	P. Allen	Ga Tech 1984-88
52 C	Active Silicon Packaging	R. Jaeger	Auburn 1984-88
53 B	Self-Testing VLSI Circuits	A. Albicki	Rochester 1985-87
54 B	Fault Tolerant WSI Processor Arrays	A. Rosenberg	Duke 1985-87
55 C	Laser Photochemical Techniques	R. Osgood	Columbia 1985-91
56	Wafer Scale Integration of Parallel Processors	C. Hedlund	No. Carolina 1985-86
57	Agent: A VLSI Designers Assistant (92)	P. Drongowski	CWU 1985
58 B	Integrated CAD/CAM/CAT for VLSI	D. Hodges R. Leachman, C. Spanos	UC/Berkeley 1985-92

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
59 B	Epitaxial Layers and Super-Lattices on Silicon	M. Nicolet B. Paine	Cal Tech 1985-96
60 C	Modeling Advanced Bipolar ICs (87)	J. Fossum	Florida 1985-96
61 C	Rapid Thermal Processing	D. Kwong	Texas 1985-87
62 F	Process Simulators (101)	J. Plummer R. Dutton	Stanford 1985
63 C	Pulsed Laser Techniques (102)	T. Sigmon	Stanford 1985
64 C	System Level Packaging (2)(103)	F. Pease	Stanford 1985
65 A	Condensed Matter on the Submicron Scale	R. Schrieffer J. Wilkins	UC/SB 1985-87
66 B	Continuous-Time MOS Analog Cells	M. Ismail	Ohio St. 1985-94
67 A	Packaging Phase 0 Proposals	5 PIs	5 universities 1985
68 G	Center of Excellence for CAD (82/O7)	S. Director R. Rutenbar, R. Rohrer	CMU 1982-96
69 F	Microscience and Technology Silicon-Based Nanoelectronics (82/01)	N. MacDonald J. Ballantyne	Cornell 1982-96
70 D	Electronic Packaging	C. Li	Cornell 1986-96
71 C	Packaging Expert System	R. Jaccodine M. Santori	Lehigh 1986-96
72 B	Information Sharing Survey	W. Ouchi	UCLA 1986
73 C	Low-Temperature Si Oxynitrides for Ultrathin Gate Insulators	J. Hutchby J. Lucovsky	RTI 1986
75 D	Vertically-Integrated VLSI Design for Signal Processing	S. Kung A. Parker	So. Cal. 1986-92
76 E	IC Manufacturing Technology	C. Osburn	MCNC 1983-88
77 C	Mfg. Eng. Cirriculum Development	D. Kerns	Fl. St. 1986-87
78 C	Modeling and Simulation of Submicron Devices	C. Mead	Cal Tech 1986
79 C	Thin Gate Oxides and Interface Reliability Research (18)	T. Ma	Yale 1983-96
80	Novel Processing Technologies (33)	R. Rief	MIT 1986
81 B	MOSFET Channel Engineering	J. Wortman M. Ozturk	NC State 1986-93
82 D	VLSI Reliability Research (42)	J. Lathrop W. Harrison, D. Dumin	Clemson 1983-94

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
83 C	Process Characterization Using Digial Scanning Electron Microscope (25)	R. Propst	No. Car. 1983-87
84 C	Hierarchical Silicon Compilation (32)	J. Savage	Brown 1983
85 F	Automation in Semiconductor Mfg.	K. Wise	Michigan 1984-98
86 E	VLSI Packaging and Inter-connection Research	J. Prince	Arizona 1984-96
87 D	Physics Based Device Models	J. Fossum	Florida 1985-96
88 C	Properties & Device Applications of Si-Based Quantum Structures	K. Wang	UCLA 1983-96
89 C	Scattering Matrix Simulation of Advanced Devices	M. Lundstrom	Purdue 1983-98
90 A	Multidimensional Computations: A Design Theory & VLSI Prototyping	W. Liu	NC State 1986-88
91 C	Analog CAD Methodology	P. Allen	Ga Tech 1986
92	VLSI Designer’s Assistant (57)	P. Drongowski	CWU 1985
93 B	MOSFETs at Low Temperature	R. Anderson	Vermont 1986-87
94 C	Computer-Aided Manufacturing	A. Strojas	CMU 1986-92
95 C	Molecular Beam Epitaxy	K. Wang	UCLA 1986-89
96 B	Creating Manufacturing Advantage in the U.S. Microelectronics Industry	W. Ouchi	UCLA 1986-87
97 A	Interconnection Structures for VLSI	D. Hammerstrom	Oregon GC 1986-88
98 B	Laser Pyro-Processing Mechanisms	S. Allen	So. Cal. 1986-87
99 C	High Density MOSFET and Memory Structures	A. Tasch, Jr.	Texas 1986-98
100 C	Properties of Si-Based Epi-taxial Layers & Superlattices (59)	M. Nicolet	Cal Tech 1985-95
101 F	Process Simulators for Silicon VLSI Devices (62)	J. Plummer R. Dutton	Stanford 1985-96
102 B	Insertable UV Laser Doping Pro-cess for ULSI Device Fabrication	T. Sigmon	Stanford 1985
103 C	System Level Packaging (82/02)(64)	F. Pease J. Bravman	Stanford 1983-96
104 C	Multilevel Interconnections (06)	K. Saraswat	Stanford 1983-87
105 C	Advanced Bipolar Devices for VLSI	J. Plummer	Stanford 1983-88

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
106 F	Mfg. Science & Tech for VLSI (46)(704)	K. Saraswat J. McVittie	Stanford 1984-98
107 D	Models for GaAs HEMPT Devices	J. Harris R. Dutton	Stanford 1984-88
108 C	Bipolar Transistor Using Silicon Epitaxial Lateral Overgrowth (81)	G. Neudeck	Purdue 1987-98
109 D	Reliable VLSI Architectures	T. Trick J. Patel, S. Kang	Illinois 1984-98
110 D	Reliability Physics (30)	C. Sah	Illinois 1983
111 C	Film Growth, Dopant Incorporation, and Low Temperature Epitaxy (06)	J. Greene	Illinois 1983-96
112 B	Oversampled Data Conversion Interfaces for VLSI Signal Processing	B. Wooley	Stanford 1987-94
113 D	Planning Tool, IC R&D/Technology Assessment	R. Whisnant	RTI 1987-91
114 B	International Competition	C. Ferguson	MIT 1987-88
116 C	Advanced 1D & 2D Device Simulators Tools for Silicon	R. Dutton	Stanford 1987-96
119 B	Software Technology Transfer	A. Rosenberg	Duke 1987-88
120 C	Metrology of ICs	G. Kino	Stanford 1987
121 C	Color Vision Inspection and Measurement System	S. Hackwood G. Beni	UC-SB 1987-88
122 B	Packaging Materials Database	C. Ho	Purdue 1987-96
123 C	Magnetically Levitated Micro-robots	I. Busch-Vishniac	Texas 1987
124 B	Prediction of Electromigration Using Noise Measurements	C. Chen	So. Florida 1987-91
125 B	Novel Data-Driven VLSI Arrays for Arbitrary Algorithms	I. Koren	Mass
126 B	Automatic Layout Packages for Sea-of-Gates Environment	C.Sechen	Yale 1988
130 B	Numerical Modeling of Devices	I. Mayergoyz	Maryland
131 B	Test Chip to Evaluate and Predict Reliability of Packaged ICs	R. Jaeger	Auburn 1985-88
132 D	Single Wafer Mfg.	N. Masnari J. Hauser	NC State 1988
133 C	Semiconductor Mfg. Cirriculum	S.Campbell	Minnesota 1983-85
134 C	Microel. Mfg. Eng. Cirriculum	L. Fuller	RIT 1988-89

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
135 C	Microel. Mfg. Eng. Cirriculum	A. Saxena	RPI 1988-89
136 C	Microel. Mfg. Eng. Cirriculum	W. Adcock	Texas 1988-89
137 C	Microel. Mfg. Eng. Program	T. Hanley	Fla. St. 1986-88
138 A	Japan Technology Report	R. Dutton	Stanford 1988-89
139 A	Technology Transfer in Japan’s Semiconductor Industry	W. Finan J. Frey	Finan 1988-89
141 B	Characterization and Testing for Realistic CMOS Faults	J. Ferguson	UC/S Cruz 1988
142 D	Design of Testable Systems	J. Abraham	Texas 1988-94
144 D	Multilevel Copper Inter-connections and Contacts	K. Saraswat S. Wong	Stanford 1989-92
145 C	Oxide and Interface Traps	C. Sah T. Nishida	Florida 1989
146 C	Tools for System-on-Silicon Specification	D. Gajski N. Dutt	UC-Irvine 1989-92
147 B	System Level Design for Testability	C. Papachristou	CWU 1987-92
148 C	Berkeley Reliability Tool	C. Hu	UC/Berkeley 1989-98
149 B	Sequential Circuit Automatic Test-Pattern Generation	M. Bushnell	Rutgers 1989
150 A	Ion Projection Lithography	E. Wolf	Cornell 1989-90
151 A	Routing and Layout Generation of Analog ICs	R. Gyurcsik J. Paulos	NC State 1989-92
152 B	Modeling of Digital Systems in a Common Simulation Environment	J. Aylor	Virginia 1989-92
153 A	Light Scattering by Raleigh Particles on Surfaces	E. Hirleman	Az. State 1989-92
154 C	Operation of MOSFETs on Very Thin SOI for VLSI Applications	J. Woo	UCLA 1989-94
155 B	Advanced Adaptive Control Strategy for Photolithography	D. Mellichamp	UC/S. Barbara 1989-94
156 A	Effects of Series Resistance & Saturation Velocity on CMOS Power Supply Voltage at Low Temperatures	S. Titcomb R. Anderson	Vermont 1989-91
157 A	Smart Power Technology	B. Baliga	NC State 1989
158 C	Resists Based on Heteropoly-tungstic Acid Adducts	A. Heller	Tx/Austin 1989-92

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
160 C	New Silicon Devices	J. Frey	Maryland 1989-92
161 B	Accurate and Rapid Measurement of Metallization Lifetimes	S. Campbell	Minnesota 1989
169 A	Mini-Mill/Megafab White Paper	H. Levinstein	Lepton 1989-90
174 C	Development Methodologes for Reactive Processes	T. Cale	Az. State 1989-97
175 B	Reliability for Advanced CMOS	S. Kerns	Vanderbilt 1990-98
176		C. Popelar	Ohio St. 1990-92
178		C. McConica	Col. St. 1990-92
179		W. Wolf	Princeton 1990
190		E. Seebauer	Illinois 1990-92
194		Fountain	RTI 1990-91
196 B	Integrated Layout for Multichip Modules	W. Dai	UC/Santa Cruz 1990-94
198		E. Shaqfeh	Stanford 1990-92
199 C	Particle Control in Process Equipment	R. Donovan	RTI 1990-94
200 B	Plasma Resistant Photoresist	F. Tranjan	UNC/Charlotte
203		M. Woo	UCLA
205 B	Synthesis/Verification of Multimodule Systems	D. Dill	Stanford
206 B	CAD Tools for Verification/Testing/ Synthesis Interface	G. Hachtel	Colorado
210 A	Status of SOI Technology	J. Stach	So. Florda 1991
211 B	Interconnect Modeling	K. Webb	Purdue 1991-94
222 B	W-Cu MOCVD	A. Kaloyeros	SUNY-Albany 1991
223 B	Pattern Precision in E-beam Litho	F. Pease	Stanford 1991-94
224	Noninvasive Temperature Measurement	J. Sturm	Princeton 1991-92
225	Measuring Sub-0.5 μm Particles	P. McMurry D. Kittelson	Minnesota 1991-92

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
270 C	Parallel E-beam Lithography	N. MacDonald	Cornell 1991
273 C	Models and Tools for Simulation of Deep Sub-micron Devices	J. Fossum	Florida 1992-98
274		J. Ruzyllo	Pa St 1992
278		D. Kwong	Tx/Austin 1992
279	Metal-Organic CVD of Copper	J. Kelber	North Texas 1992
280 C	Real-time Process Control Using Fuzzy Logic and Neural Nets ((557)	R. Mahajan	Colorado 1992-94
281		J. Prince	Arizona 1992
283		J. Abraham	Tx/Austin 1992
284	Power ICs Based on SOI	J. Plummer S. Wong	Stanford 1992
285	Device Models for Power IC CAD	D. Burk K. Ngo	Florida 1992
286		J. Sturm	Princeton 1992
289		M. Feldman	LSU 1992
290		C. Spanos	UC/Berkeley 1992
292 C	Techniques for Design Verification & Verification Based Test	D. Fussel	Tx/Austin 1992-94
293	Performance Verification	R. Vemuri	Cincinatti 1992
294	Automatic Verification	E. Clarke	CMU 1992
295	Two-level Formal Approach to Hardware Verification	C. Seger	Brit Col 1992
297		L. McGinnis	Ga Tech 1992
298	Automatic Layout	C. Sechen	Washington 1992
299		C. Y. Ho	Purdue 1992
300		M. Nicolet	CIT 1992
302	Dopant Profiling by Scanning Microscopy	C. Williams	Utah 1992
304		J. Herman	Sigma Xi 1992

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
305	Mixed-Mode Simulation Acceleration	D. Overhauser	Duke 1992
306	Epitaxial $CoSi_2$ on (001) Si	T. Tan	Duke 1992
308		J. Sturm	Princeton
309 E	Microsystem Technologies	D. Antoniadis	MIT 1993-98
312		T. Murrin	Duquesne -92
313		D. Hirleman	Az.State 1992
314		E. Seebauer	Illinois 1992
315 C	Test Generation for Realistic Faults	F. Ferguson T. Larabee	UC/S. Cruz 1993-98
317		D. Antoniadis	MIT
319	Optical and Electrical Interconnects	A. Christou	Maryland 1992-95
320	Polymeric Materials and Packaging	P. Ho	Texas 1993-95
321	Optoelectronic Applications	A. Cangellaris	Arizona 1992-96
322		V. Kenner	Ohio St. 1992-93
323		R. Mahajan	Colorado
324	CoE in Design Automation (82/08)	R. Brayton	UC/Berkeley 1993
325		C, Ho	Purdue 1993
329		J. Bravman	Stanford 1993
331 C	Mechanical Reliability of Packages	C. Popelar V. Kenner	Ohio St. 1990-94
337	Reliability of BiPolar Transistors	C. Sah A. Neugroschel	Florida 1993-94
338	Tools for System Level Timing	K. Sakaliah	Michigan 1993
340 B	Nucleation and Growth in $TiSi_2$ CVD (341)	E. Seebauer	Illinois 1993-94
343	Circuit-Level Modeling/Optimization	L. Pileggi	Texas/CMU 1994
344 B	Semiconductor Mfg Productivity	A. Glassey	UC/Berkeley 1994
345 A	Interconnect Test Structure Design	J. Prince	Arizona 1993-94
346	Placement and Routing	C. Sechen	Washington

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
348	Gas Phase Cleaning of Silicon	J. Ruzyllo	Pa State 1989
350	Surface Roughness Correlations	C. Helms	Stanford 1993
351 B	RF Telecommunications Ics	S. Wong	Stanford 1993-96
352	Stress Voiding and Electromigration	C. Li	Cornell 1993
353	Interconnect Metallurgy Optimization	P. Ho	Tx/Austin 1993
354	Production Logistics	R. Akella R. Leachman	UC/Berkeley 1993
356	Reliability of Lead-Free Solder	K. Tu	UCLA 1993-96
357 C	Microminiature Thermal Management	F. Pease K. Goodson	Stanford 1993-97
358	Reliability of IC Packages	C. Popelar V. Kenner	Ohio St 1993-96
361 B	Silicon Oxidation and Surface Cleaning	J. Gibson	Illinois 1994-97
362	Lo-cost Hi-performance Interconnects	P. Kohl	Ga Tech 1993-96
365 B	Physics-of-Failure/Electronic Packages	M. Pecht	Maryland 1993-94
374 C	Gigascale Integration	J. Meindl	Ga Tech 1993-98
376 B	Oxides on 6H-SiC and β-SiC	J. Baliga J. Wortman	NC State 1994
377 C	Numerical Modeling of Devices	I. Mayergoyz N. Goldsman	Maryland 1994
378 B	Fabrication Technology for SiC Devices	J. Cooper, Jr. M. Melloch	Purdue 1994
384	Production Logistics	R. Akella	CMU 1993
388 E	Verification of Large Scale Systems	J. Abraham D. Fussell	Texas 1994-98
389 B	Asynchronous Control Circuits	D. Dill	Stanford 1994
400	Multilevel Copper Interconnections	S. Wong	Stanford
402	Dissolution-Inhibition Resist	A. Reiser	Polytech
403	193 nm Lithography	B. Smith	RIT
405	Single-Wafer Processing	H. Sawin	MIT
406 B	Transport Simulation	K. Hess U. Ravaioli	Ill

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
407 C	Low Power Mixed Mode Circuits	J. Woo	UCLA
408	Reliable Interconnects, Contacts, and Vias	C. Thompson	MIT
409	Advanced Resist Materials	G. Wilson	Tx/Austin
411	Resists with Low Environmental Impact	J. Frechet	UC/Berkeley
412	Reliability of Submicron Silicon	C. Sah	Florida
413	Metrology at 0.13 Micrometers	D. Joy	Tennessee
415	Proximity Effect Correction	S. Lee	Auburn
416	Silicon Based Nanoelectronics	J. Ballantyne	Cornell
417	BSTM and MOSFET Modeling of Transistors	C. Hu	UC/Berkeley
418	Semiconductor Technology Limitiations	N. Masnari W. Holton	NC State
420	Optical Interconnect Systems	R. Kostak A. Cangellaris	Arizona
421	Design for Quality	M. Styblinski	Texas A&M
422	Adhesion/Wetting of Copper	J. Kelber	North Texas
425	NSF/SRC ERC Environmentally Benign Semiconductor Manufacturing	F. Shadman	Arizona
428	Moisture Induced Crack Growth	H. Nied	Lehigh
436	Lithium Plasma Source for EUV Lithography	W. Silfvast	Central Fl
437	Design of Optical Systems/Metrology	D. Moore	Rochester
438	Near-Field Optics	R. Grober	Yale
440 B	MOSFET Modeling	J. Fossum	Florida
441 C	Surface Nanoparticles	E. Hirleman	Wayne State 1996-97
442 D	Particle Control	S. Campbell	Minnesota
443	Gas Phase Conditioning of Silicon Surface	J. Ruzyllo	Penn State
446	0.1 Micron Lithography	J. Sesian	Arizona
448 G	Advanced Interconnections	S. Murarka	RPI 1996-98
449 B	Effect of Nanoscale Material Inhomogeneity	T. Gross	N Hampshire 1996-98
450	Spin-on Aerogels	W. Gill	RPI
451	Ultrathin Silicon Oxynitride Dielectrics	E. Garfinkel	Rutgers

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
452	Advanced Lithography and Metrology	F. Cerrina	Wisconsin
453 C	Clock-signal Distribution Using Microwaves	K. O	Florida 1996-98
454	In-line Metrology and Surface Engineering	C. Helms	Stanford
455	All-silicon Optimal Interconnect	D. Kerns	Vanderbilt
456	Polymers for Mircoelectronic Packaging	M. Santore	Lehigh
457	Fatigue in Packaging	S. Liu	Wayne State
458	System Level Packaging	J. Bravman	Stanford
459	Innovative Sensors	R. Jaeger	Auburn
460	Advanced Lithography Network	W. Oldham	UC/Berkeley
461	Simulation/Thermometry for ESD Reliability	K. Goodson	Stanford
462	Improved Capacitors & Mixed Signal Packaging	P. Krusius	Cornell
463	Ferroelectric Materials for Semiconductor Devices	A. Kingdon	NC State
465	Fracture Parameter Modeling in Packaging	E. Madenci	Arizona
466	Run-to-run Control	E. Zafiniou G. Rubloff	Maryland
478 B	Device Noise Simulation	G. Bosman	Florida
479 C	Gate Dielectrics for 0.1 Micron FETs	S. Campbell	Minnesota 1996-98
480 B	D_2 Annealed Ultra-Thin Dielectrics	E. Rosenbaum	Illinois
481 B	EUV Lithography	F. Cerrina	Wisconsin
482 C	VLSI Test and Diagnosis	J. Patel	Illinois 1996-98
483 C	High-Level Approaches to IC Testing	J. Abraham D. Fussell	Texas
484 B	High-level Power Estimation for VLSI	F. Najm	Illinois
485 A	Design Methodologies for 1 Ghz & Above	K. Yun	UC/S Diego
486 A	Approximation Based Verification	P. Beerel	So. Cal.
487 B	Synthesis and Verification of Timed Circuits	C. Myers	Utah
488 B	Channel Engineering in MOSFETs	S. Banerjee A. Tasch	Texas

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
489 A	Analysis of Wafer Fab Operations	P. Kumar	Illinois
490 C	Modeling Stochastic Processes in Semiconductor Manufacturing	L. Schruben	Cornell
491 C	Integrated Hierarchial Life Cycle Approach	M.Fu, Herrmann I.Marcus, G.Rubloff	Maryland
492 A	Modeling, Analysis, & Design of Wafer Fabs	S. Gershwin	MIT
500 F	Lithography and Pattern Transfer-SCOE	W. Oldham A. Neureuther	UC/Berkeley 1987-96
501 C	Contamination/Defect Assessment and Control-SCOE	F. Shadman J. Prince, H. Parks	Arizona 1988-96
502 E	On-Line Analysis and Metrology for Semicond. Manufacturing-SCOE	S. Brueck J. McNell	N. Mexico 1988-94
503 D	Single Wafer Processing for Flexible IC Manufacturing-SCOE	H. Sawin	MIT 1988-96
504 F	Plasma Processing-SCOE	D. Richman J. Cecchi	Sarnoff Princeton 1988-94
505 F	Materials and Bulk Processes-SCOE	W. Adcock A. Tasch	Texas 1988-96
506 D	Factory Systems-SCOE	D. Phillips	Tx A&M 1988-92
507 D	X-ray Lithography-SCOE	F. Cerrina	Wisconsin 1988-96
508 F	Multilevel Metallization-SCOE	R. Gutmann S. Muraka	RPI 1989-96
509 F	Clustered Processes-SCOE	N. Masnari	NCSU 1989-94
510 C	Predictive BiCMOS Process Design for Manufacturing-SCOE	T. Sanders	Florida IT 1988-92
511 D	Rapid Yield Learning-SCOE	W. Maly A. Strojwas	CMU 1989-92
512 C	Plasma Equipment Modeling	M. Kushner	Illinois 1990-98
513	Confocal Microscope	G. Kino	Stanford
515	Optical Lithography-SCOE	F. Pease	Stanford 1987-96
516		F. Cerrino	MIT
517		C. Spanos	UC/B
518		J. McNeil	N. Mexico
519		D. Mellichamp	UC/SB
520		A. Daloyeros	SUNY-Alb.
521		S. Brueck	N. Mexico

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
522		H. Sawin	MIT
523		K. Jensen	MIT
527 B	Behavioral and Structural BIST	C. Papachristou	CWR 1993-97
528	Algorithms for Test Pattern Generation	M. Bushnell	Rutgers
529 B	Large Area RF Plasma Sources	F. Chen	UCLA 1993-98
530	Multidimensional Process Simulation	S. Dunham	Boston U. 1993
531	CVD Metallization of Lo-K Dielectrics	J. Kelber	N. Texas 1993
532	Adaptive Grid Algorithms	M. Law	Florida 1993
533	Impurity Gettering	G. Rozgonyi	NCSU 1993
534	Solder Fatigue Data Base	L. Keer	NWU 1993
535	Stress in Packaged Ics	R. Jaeger	Auburn 1993
534		L. Keer	Northwestern 1994-96
535		R. Jaeger	Auburn 1993-96
538	Behavioral BIST Insertion	A. Orailoglu	UC/SD 1993
539	Models/Numerics for Process Simulation	M. Law	Florida 1993
540 C	Analytical Modeling Methodologies	D. Phillips	Texas A&M 1994-96
541 C	Plasma Diagnostics	J. Cecchi	N. Mexico 1994
549 D	Advanced Helicon Source Development	J. Cecchi H. Anderson	N. Mexico 1994
550 C	Spatial-Phase-Locked Beam Lithography	H. Smith	MIT 1994-99
551 C	Photocatalytic Oxidation	G. Raupp	Az. State 1994
552 C	Built-in Self Test	M. Soma	Wash. 1994
553 C	Benchmark Program in Design Automation	F. Brglez	NCSU 1994
554 C	Organic Chip Attachment Adhesives	R. Pearson	Lehigh 1994
555 A	Low Power IC Design	C. Sodini	MIT

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
556	Device Models for Power IC CAD	K. Ngo	Florida 1994
557 C	Process Control Using ANN/Fuzzy Logic (280)	R. Mahajan	Colorado 1992-95
558 C	Adaptive Gridding	J. White	MIT 1993-98
559 C	CAD for Low Power	M. Pedram	USC 1994
560 C	Activity Driven Low Power Synthesis	G. Hachtel F. Somenzi	Colorado 1994
561 B	Lo Pwr/Lo Volt Analog Circuit Design	H. Lee	MIT 1994
562 B	Low Environmental Impact Resists	C. Willson	Texas 1994
563 C	Sensing and Reaction Modeling	G. Rubloff	NCSU 1994
564 C	Water Recycle and Waste Minimization	F. Shadman	Arizona 1994
565 C	Optimizing DI Water Use	C. Helms	Stanford 1994
566 A	Scatterometry	J. McNeil	N. Mexico 1994-99
567 A	IC Reliability Simulator	C. Hu	UC/B 1994
568 D	Resist User Facility	M. Rothschild	Lincoln 1994
569 B	Resist Materials with Low Environmental Impact	Frechet	Cornell 1994
570 C	Analog-Digital Interface Circuits	P. Gray R. Meyer	UC/B 1994
573 C	IR/Chemometric Sensors	T. Niemczyk	N. Mexico 1994-97
574	Metrology & On-line Analysis	J. McNeil	N. Mexico
700 C	Intelligent IC Factory	C. Spanos	UC/B 1993-98
701 C	Technology Transfer for EVOLVE	T. Cale	Az State 1993-94
702 D	Packaging Architecture Design Methods	P. Krusius	Cornell 1994-96
703 C	Mixed Signal IC Design	B. Wooley	Stanford 1994
704 F	CIM for VLSI (106)	K. Saraswat	Stanford 1984
705 C	Advanced Resist Materials	C. Willson	Texas 1994

SRC # Funding	Title (Numbers of related contracts)	Principal Investigator(s)	University Term or Start Date
706	Automatic Test Pattern Generation	M. Bushnell	Rutgers 1994
707	Models/Numerics for Process Simulation	M. Law	Florida
801 C	Ion Implantation Characterization	A. Tasch	Texas 1994
802 C	Non-perfluorocompounds for Etching	R. Rief	MIT 1994
803 C	PFC and CFC Emissions and Abatement	H. Sawin	MIT 1994-98
804	Yield Learning Model for Package Devel.	D. Walker	Tx A&M
805	Enhancements to MGP for S/C Industry	B. Soni	Miss St
806	Process Sensitive Simulation Tools	C. Thompson	MIT
807	Model for Ion-Implant Induced Damage	A. Tasch	Texas
808	Kinetic and Transport Models	T. Cale	Arizona St
809	3d Topography Simulation	A. Neureuther	UC/Berkeley
810	Water Conservation	F. Shadman	Arizona
811	Advanced Resist Materials	J. Frechet	Cornell/UCB
812	Silicon TCAD	W. Harrison	Stanford
813	Verification of First Principle Cals.	K. Jones	Florida
814	Atomistic Models for ULSI Simulation	S. Dunham	Boston U.
815	VIA, Contact, & Interconnect Structures	H. Frost	Dartmouth
816	Monte Carlo Device Simulation Platform	U. Ravaioli	Illinois
817	Simulations of Plasma Surface Chemistry	D. Graves	UC/Berkeley
818	Surface Chemistry Predictions	K. Jensen	MIT
820	Etching in Chlorine Plasmas	E. Shaqfeh	Stanford
900	Metrology of Very Thin Films	R. Reif	MIT 1994

APPENDIX D

PARTICIPATION IN THE SRC

MEMBER ORGANIZATIONS

Bold face type indicates full members

Advanced Micro Devices, Incorporated
AG Associates
ANACAD Electrical Engineering Software
Applied Materials, Incorporated
AT&T
BTA Technology, Inc.
Cadence Design Systems
CVC Inc.
Dawn Technologies, Inc.
Department of Defense
Digital Equipment Corporation
E. I. duPont de Nemours & Company
Eaton Corporation
Epic Design Technology, Inc.
ETEC Systems, Incorporated
Excimer Laser Systems Inc.
FLIPCHIP Technologies
GCA Corporation
General Instrument Corporation
Goodyear Aerospace Corporation
Hampshire Instruments
Hestia Technologies, Inc.
Honeywell, Incorporated
IBM Corporation
Integrated Silicon Systems, Inc.
Intel Corporation
Jamar Technology Co.
Lawrence Livermore National Laboratory
LSI Logic Corporation
Lucent Technologies
M/A COM
Mentor Graphics Corporation
Meta-Software, Inc.
Micron Technology, Incorporated
Mission Research Corporation
Monolithic Memories, Incorporated
Motorola, Incorporated
National Science Foundation
National Semiconductor Corporation
nChip Inc.
Neo Linear, Inc.
Numerical Technologies, Inc.
Novellus Systems Incorporated
OEA International, Inc.
Office of Naval Technology
Advanced Technology Applications, Inc.
Alcoa
Analogy Inc.
Arizona Packaging Software Inc.
Brantford Computer Haus
Burroughs Corporation
Control Data Corporation
DARPA
Defense Nuclear Agency
DesignAid, Inc.
DTX/Thermacore Inc.
Eastman Kodak Company
Emergent Technologies Corp.
Essential Research Inc.
E-Systems, Incorporated
Famtech/Speedfam Corp.
Ford Motor Company*
General Electric Company
General Motors Corporation
GTE Laboratories, Incorporated
Harris Corporation
Hewlett-Packard Company
Ibis Technology Corp.
Integrated Electronic Innovations
IntelliSense Corp.
Intersonics, Inc.
Lawrence Berkeley National Laboratory
Loral Systems Group
Los Alamos National Laboratory
LV Software, Inc.
Matrix Integrated Systems Inc.
MEREX Corp.
Microelectronics & Computer Technology Corp.
MicroUnity Systems Engineering, Inc.
The MITRE Corporation
Monsanto Company
National Institute of Standards and Technology
National Security Agency
Naval Surface Warfare Center - Crane
NCR Corporation
NORTEL (Northern Telecom)
Northrop Grumman Corporation
Oak Ridge National Laboratory
Office of Naval Research
Office of the Undersecretary of Defense, CET

MEMBER ORGANIZATIONS (continued)

Bold face type indicates full members

OMNIVIEW, Inc.
PDF Solutions, Inc.
Process Technolgy Ltd.
Physical Electronics
Prometrix
QuanScan, Inc.
RCA Corporation
Rockwell International Corporation
Sandia National Laboratories
SEMI, Chapter
SEMI Chapter
Shipley Company
Sienna Technologies Inc.
SILVACO Data Systems
Solid State Equipment Corp.
Solid State Systems, Inc.
Spire Corp.
Sunrise Test Systems
Techware Systems Corp.
Texas Instruments Incorporated
Ultratech Stepper
Unit Instruments, Inc.
U.S. Army Research Office
Verity Instruments, Inc.
Westinghouse Electric Corporation
WYKO Corp.
XMR Inc.
Peak Systems, Inc.
Phenix Semicron Corp.
The Perkin-Elmer Corporation
Praxir Incorporated
Q-metrics, Inc.
Rapro Technology Inc.
Realtime Performance Inc.
SAL Corporation
Scientific Exchange
SEMATECH
Semiconductor Industry Association
SiBond, L.L.C.
Silicon Systems, Incorporated
Snopsys
Solid State Measurements, Inc.
Sperry Corporation
SRI International
Technology Modeling Associates, Inc.
Tessara, Inc.
Tyecin Systems, Inc.
Union Carbide Corporation
UTI Instruments Company
Varian Associates, Incorporated
VLSI Standards, Inc.
Wright Laboratory
Xerox Corporation

AFFILIATE AND CHAPTER MEMBERS OF THE SRC (99)

Advanced Technology Applications, Inc.
American Technical Ceramics
ANACAD Electrical Engineering Software Inc.
Arizona Packaging Software, Inc.
Brantford Computer Haus
Coors Ceramics Co.
Dawn Technologies, Inc.
DTX/Thermacore Inc.
Eagle-Picher Industries, Inc.
Emergent Technologies Corp.
Essential Research Inc.
Famtech/Speedfam Corp.
Flexible Manufacturing Systems, Inc.
AG Associates
Analogy Inc.
Applied Electron Corp.
ASYST Technologies, Inc.
BTA Technology Inc.
CVC Holdings Inc.
DesignAid
Dynapert/Amedyne
E/G Electro-Graph, Inc.
Epic Design Technology, Inc.
Excimer Laser Systems, Inc.
FEP Analytic
FSI Corp.

Genus, Inc. Gryphon Products

AFFILIATE AND CHAPTER MEMBERS OF THE SRC (99) (continued)

Hampshire Instruments
Hercules Specialty Chemicals Co.
Hestia Corp.
Ibis Technology Corp.
Integrated Electronic Innovations Inc.
Integrated Silicon Systems, Inc.
IntelliSense Corp.
Intersonics, Inc.
Ion Beam Technologies, Inc.
Ion Implant Services
Isitec Corp.
Jamar Technology Co.
Logical Solutions Technology, Inc.
Lehighton Electronics, Inc.
LV Software Inc.
MacDermid, Inc.
Machine Intelligence Corp.
Machine Technology, Inc.
Meta-Software Inc.
Matrix Integrated Systems Inc.
MEREX Corp.
MG Industries/Scientific Gases
The Microminipulator Company, Inc.
Micrion Corp.
Micronix Corp.
Micro Mask, Inc.
MicroUnity Systems Engineering Inc.
Mission Research Corp.
nChip, Inc.
OEA International
Omniview Inc.
Oneac Corp.
Optical Specialties, Inc.
Pacific Western Systems, Inc.
PDF Solutions
Peak Systems, Inc.
Phenix Semicron Corp.
Probe-Rite, Inc.
Process Technology Limited
Prometrix Corp.
PT Analytic, Inc.
Pure Aire Corp.
Q-metrics Inc.
QuanScan, Inc.
Rapro Technology, Inc.
Realtime Performance Inc.
Sage Enterprises, Inc.
Scientific Exchange
Semi-Gas Systems, Inc.
Sienna Technologies Inc.
Silsco, Inc.
SILVACO Data Systems
SOHIO Engineered Materials Co.
Solid State Equipment Corp.
Solid State Measurements, Inc.
Solid State Systems Inc.
Spire Corp.
SRI International
The SEMI Group, Inc.
Sunrise Test Systems, Inc.
Technology Modeling Associates, Inc.
Techware Systems Corp.
Thermco Systems, Inc.
Tyecin Systems Inc.
Universal Energy Systems, Inc.
Unit Instruments, Inc.
UTI Instruments Co.
Verity Instruments Inc.
VLSI Standards, Inc.
WYKO Corp.
XMR, Inc.

ASSOCIATE MEMBERS (8)

Lawrence Berkeley Laboratory	Lawrence Livermore Laboratory
Los Alamos National Laboratory	The MITRE Corporation
Microelectronics and Computer Technology Corp.	Oak Ridge National Laboratory
Sandia National Laboratories	SEMATECH, Inc.

PARTICIPATING GOVERNMENT ORGANIZATIONS (11)

Army Research Office	Defense Nuclear Agency
Department of Defense	National Security Agency
National Institute for Standards and Technology	National Science Foundation
Naval Surface Warfare Center - Crane	Office of Naval Technology
Office of Naval Research	OUSD/Computer/Electronic Technology
Wright Laboratory, USAF	

APPENDIX E

TIME LINE
1981 - 1996

NOTEWORTHY EVENTS IN THE LIFE OF THE SRC

INTRODUCTION

The integrated circuit (IC) industry emerged in the late fifties in the U.S., took form in the sixties, and experienced rapid growth in the 70ies. In 1979, when Japanese companies captured 42% of the U.S. market for 16 kbit DRAMs and converted Japan's integrated circuit trade balance with the U.S. from a negative $122 M in 1979 to a positive $40 M in 1980, the U.S. industry's "ownership" of the IC industry was challenged. Other nations seeing the IC as a key to future economic success, resolved to do whatever was necessary to participate.

Both government and private groups recognized the importance of the IC industry and described the negative impacts of a loss of leadership in widely circulated reports. All agreed that U.S. industry leadership in semiconductors was important.

The Semiconductor Industry Association was created in 1977 to gather reliable information on the industry and to develop mechanisms for addressing industry issues with the government. It was the appropriate organization to address the competitive challenge. In a presentation to an SIA Board Meeting in June, 1981, Erich Bloch of IBM described the issue and proposed the creation of a "semiconductor research cooperative" to assure continued U.S. technology leadership.

From this the SRC was born. Its research program and the students that graduate after participating in SRC-supported research have proven valuable to this vital industry. Partially because of these activities, the U.S. semiconductor industry is leading both the market and the technology.

Highlights in SRC's history are given below.

TIME LINE

NOTEWORTHY EVENTS IN THE LIFE OF THE SRC

1981

At the June SIA Board meeting, Erik Bloch outlined the proposal for a cooperative research organization with the primary purpose being the maintenance of U.S. industry leadership in the semiconductor industry through research. On December 16, Bob Noyce, then SIA chairman and Intel Corp. vice-chairman, announced the establishment of the SRC. The purpose was to stimulate joint research in advanced semiconductor technology by industry and U.S. universities. He noted that leadership in semiconductor research will determine market performance in the future and noted that U.S. research in real dollars has been decreasing in the last few years. Cooperative research such as the SRC should help reverse this trend.

1982 Board Chair - Erich Bloch(IBM) Budget $6.5 M
TAB Industry Cochair - Phil Downing (AMD) UAC Chair - Andrew Steckl(RPI)

Jan - First SRC Board (interim) meeting in Santa Clara dealt with membership, selection of Executive Director, fees, technical advisory board, university relationships, agenda, and SRC structure.
- Erich Bloch elected chairman.

Feb - SRC incorporated with eleven founding members.

Mar - Board of Directors defines purposes of SRC: 1) provide clearer view of technology needs, 2) fund research that addresses needs, 3) focus attention on competition, and 4) reduce redundancy. Invites participation by U.S. industry.

Apr - Larry W. Sumney, director of the Defense Department's VHSIC program, is named executive director of the SRC. Recommendations received from first meeting of SRC University Advisory Committee.

Aug - Research Triangle Park, North Carolina chosen as SRC site. Technical Advisory Board appointed to provide technical guidance and direction.

Sep - Core SRC staff hired, and corporate offices are opened. First request-for-proposals mailed to approximately 150 universities. First TAB meeting held at SRC RTP office.

Nov - Centers of Excellence in major research focus areas are established: Cornell-SRC Center for Microscience and Technology, and CAD Centers at Carnegie-Mellon and UC/Berkeley. Membership grows to 12 companies. Five proposals for research selected for early funding from 166 received.

Members - Advanced Micro Devices, Control Data Corp., Digital Equipment Corp., General Instrument, Honeywell, Hewlett-Packard, IBM, Intel, Monolithic Memories, Motorola, National Semiconductor and Silicon Systems.

1983 Board Chair - Erik Bloch(IBM) Budget $11.5 M
TAB Industry Cochair - Dave Sikes (Motorola) UAC Chair - Andrew Steckl(RPI)

Jan - Thirty-seven research proposals are accepted for funding. First industrial assignee joins the SRC from IBM.

May- Membership reaches nineteen companies. Joint Conference and SRC/SIA Board meeting held in RTP, NC featuring addresses by Jim Hunt, Governor of North Carolina, and George A. Keyworth II, Science Advisor to the President.

Jun - New programs initiated at MIT (3-D circuits and systems) and MCNC (manufacturing technology). The SRC publishes its first newsletter and holds its first technology workshop (Gallium Arsenide devices).

Jul - First Topical Research Conference (TRC) on Multilevel Simulation is held at UC/Berkeley, and the first nine Technical Reports are published.

Aug- VLSI Reliability research program is initiated at Clemson University.

Sep - SRC launches Industrial Mentor Program and publishes initial set of aggressive research goals. Membership expands to 24 companies.

Nov- SRC research portfolio includes 50 research contracts with 30 private and state universities. Over 100 faculty members and 125 graduate students are working under these contracts.

- Second TRC held: Deposition Processes.

Dec- First patent resulting from SRC research is disclosed by G.C. Dalman of Cornell. The SRC Board of Directors excludes foreign membership.

Regional Distribution of SRC Funding
October 1983

Region / Institution	Funding	Region / Institution	Funding
New England	1,222,000	South Atlantic	1,340,000
MIT	747,000	MCNC	636,000
Yale	197,000	North Carolina	220,000
Brown	99,000	Clemson	215,000
Vermont	79,000	Georgia Tech	100,000
		South Carolina	97,000
Middle Atlantic	3,044,000	Florida	72,000
Cornell	1,094,000		
CMU	937,000	East South Central	116,000
RPI	525,000	Miss State	116,000
Penn State	195,000		
Rochester	105,000	West South Central	101,000
Columbia	89,000	Texas A&M	101,000
Johns Hopkins	99,000		
		Mountain	350,000
East North Central	826,000	Arizona	249,000
Illinois	555,000	Arizona State	101,000
Wisconsin	88,000		
Purdue	92,000	Pacific	1,645,000
Notre Dame	91,000	UC Berkeley	1,000,000
		Stanford	438,000
West North Central	398,000	So. California	116,000
Minnesota	286,000	UCLA	91,000
Iowa	112,000		
	TOTAL	$8,942,000	

New members - AT&T, Burroughs, du Pont, E-Systems, Eaton, General Electric, Goodyear Aerospace, Harris, LSI Logic, Monsanto, Perkin Elmer, RCA, Rockwell, Union Carbide, Varian, Westinghouse, Xerox, and SEMI chapter.

Technical Meetings - III-V Digital Research Strategy, Deposition Processes, Multilevel Simulation, Advanced Packaging Strategies

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1984 Board Chair - George Scalise (AMD) Budget $15M
TAB Cochair - Jim Daughton (Honeywell) UAC Chair - David A. Hodges, UCB

Jan - Three new programs established: Digital GaAs (UC/Santa Barbara); Manufacturing Automation (Michigan); and Manufacturing Simulation (Stanford). Membership expands to 25 companies.
Mar - Research funding reaches $12 million annual level. The research portfolio includes three Centers of Excellence, 7 programs, and 43 projects. Membership expands to 29 companies.
Apr - SRC Technical Reports Series reaches 45 volumes.
May - Information Central, a dialup database of research abstracts and other nformation, is activated.
Jun - Eugene Flath (Intel) becomes second Board Chairman.
Aug - SRC holds its first 3-day Summer Study in Denver, Colorado, resulting in echnology goals with a ten-year horizon: described in the April 1985 SRC Newsletter.
Nov - RFP for "Research in Design Concepts" sent to approximately 150 universities.
Dec - 1985 budget set at $16 million.

New members - Kodak, GCA, GTE, General Motors, Sperry and Texas Instruments.

Technical Meetings - Built-in Test/Testability, Design Synthesis, Interface Engineering, Devices & Structures, Manufacturing Science, Wafer Scale Integration, nterconnections and Contacts, Rapid Thermal Annealing

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1985 Board Chair - George Scalise (AMD) Budget $16 M
TAB Industry Cochair - Court Skinner (NSC) UAC Chair - Dave Hodges (UCB)

Jan - First SRC Technology Transfer Course held at CMU on FABRICS II, a statistical process modeling software package.
Feb - Richard Alberts, SRC Vice President for Policy and Planning (and a semiconductor industry mover-and-shaker) retires.
Mar - George Scalise succeeds Eugene Flath as Board Chairman.
May - SIA/SRC Health and Safety Workshop held in Chapel Hill, NC.
Jun - SRC sponsors 5-day Packaging Training Course/Univ. of Arizona
Aug - Summer Study in Vail, Colorado recommends a careful expansion of the SRC scope to meet increasing industry expectations. A discussion of this summer study is published in the October 1985 SRC Newsletter.

New members - GTE

Technical Meetings - Post-shrink Silicon Devices, FABRICS II, Placement and Routing, Health and Safety, Submicron Microstructure Characterization, Analog Computer-Aided-Design, In-situ Processing, Gallium Arsenide Device Models, Technology Assessment, Manufacturing Competitiveness, Quarter Micron CMOS, Al:Si/Ti Multilayer Metallization Interconnect System, Short-channel MOS Device Model, Submicron Device Reliability

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1986 Board Chair - George Scalise (AMD) Budget $19.4 M
TAB Industry Cochair - Dragan Ilic (HP) UAC Chair - David Hodges (UCB)
GCC Chair - K. Speierman (NSA)

Jan - Fellowship and Summer Intern programs initiated.
Apr - SRC Executive Director testifies before U.S. House of Representatives Committee on Science and Technology on science policy re scientific research by the federal government.
- SRC announces $250,000 awards to both Lehigh University and Cornell University for research in semiconductor packaging.
May- Seminar on Microelectronics in Japan held in RTP, NC and sponsorship of micorelectronics manufacturing engineering curriculum development initiated.
Aug - Summer Study focuses on technology roadmaps and concludes that
(a) the roadmaps should be integrated,

(b) SRC should focus on only the most important technical areas, and
(C) SRC should extend itself into competitiveness issues.

Dec - SRC conducts survey on U.S. status in semiconductor manufacturing equipment and materials.
- 1987 SRC budget set at $17.6 million.

New members - Applied Materials and LSI Logic. SEMI Chapter formed and U.S. government participation initiated.

Technical Meetings - In-situ Laser Processing; Software Portability; Bipolar Device Technology; Automatic Synthesis; Microelectronics in Japan; Manufacturing Sciences; Quarter-micron CMOS Technology; Packaging; Advanced III-V & Si Device Modeling; FABRICS; Microstructures; Characterization; E-Beam Lithography; Automatic CAD Package for CMOS Circuits; Kinetic Modeling of Directional Plasma-Etching Processes; Process Modeling & Simulation with SUPREM, SAMPLE, & SIMPL;
Concurrent Hierarchical & Extensible Fault Simulator; Computer-integrated-Manufacturing; GaAs HEMT Device Models.

1987 Board Chair - Klaus Bowers (AT&T) Budget $17.6 M
TAB Industry Cochair -Stan Jaskolski(Eaton) UAC Chair - Steve Director (CMU)
GCC Chair - K. Speirman (NSA)

Jan - SRC staff visits Japan to study cooperative research there.
Mar - Senator Bingaman keynotes SRC annual technical meeting.
Apr - SRC takes lead in establishing National Advisory Committee on Semiconductors (NACS) including Sumney testimony before House subcommittee supporting NACS as "A coherent strategy that ties the many programs and players together..".
May - Steering Committee for SEMATECH designates Larry W. Summney acting head of start-up operations, while remaining as SRC President. SEMATECH mission is to reverse erosion of U.S. leadership in manufacturing technology.
Jun - Klaus D. Bowers of AT&T Bell Labs succeeds George Scalise of AMD as Chairman.
Aug - 1987 Summer Study (Park City, Utah) addresses issues regarding SRC and SEMATECH, technology roadmaps, inventions needed, SRC's growth and operations, and technology transfer.
Sep - N.C. Governor James Martin addresses Joint SIA/SRC forum on "U.S. Competitiveness - Analysis and Remedies."

New members - Loral and NIST

Technical Meetings - Technology Transfer; FABRICS; Reliability; Process and Device Modeling, Bipolar Device Technology, Quantum Domain, Design Verification; Data Management for CAD; TCAD for BiCMOS Design; Japan; Packaging Reliability Without
Hermeticity; Submicron BiCMOS Technologies for the 1990s.

1988 Board Chair - Robert McMillin (GMC) Budget $16.3 M
TAB Cochair - Pallab Chatterjee (TI) UAC Chair - Steve Director (CMU)
GCC Chair - K. Speierman (NSA)

Jan - Klaus Bowers (ATT) completes term as Board Chair.
May - University Advisory Committee provides comprehensive set of recommendations to SRC - research program, E-mail, technology transfer, patents, review effectiveness, program terminations, funding, mentors, etc.
Jun - Bob McMillin (General Motors) elected Board chairman, first SRC video seminar, "Computer Automated Semiconductor Manufacture,"
- SRC Competitiveness Foundation established.
Jul - New SRC Centers-of-Excellence at Michigan (manufacturing automation) and Stanford (manufacturing systems).
Aug - National Advisory Committee on Semiconductors created. SRC summer study discusses: 1) future research agenda, 2) role of the SRC, 3) organizational aspects for 2001, 4) government participation and role, and 5) technology transfer.
Oct - TECHCON 88, first SRC general technical meeting. Speakers: Gil Amelio (Rockwell) on "The Semiconductor Industry: Cooperation for Survival;" Jim Gibbons (Stanford) on "Universities, the SRC, and Cooperative Research;" Paul Castrucci (SEMATECH) on "The Semiconductor Technology Chain;" and Larry Sumney (SRC)

on "Semiconductor Technology Strategy and the SRC."

Nov - SRC participates in GOMAC-88 with theme, "International Competitiveness - its impact on Government Electronics"

New members - LSI Logic, Micron, NCR, SEMATECH, AFWAL, DNA

Technical Meetings - CREEP: A 2D Creepflow Process Simulator; Microelectronics Mfg Engineering Cirricula Development; Computer-Automated Semiconductor Manufacture; Synchrotron Radiation and Semiconductors; Manufacturing Excellence in the 1990s; Design Synthesis; Technology CAD for BiCMOS Design; CIM Research; COSMOS Switch-level Simulator; Sea-of-Gates Design; and Analog Design Automation.

1989 Board Chair - Robert McMillin (GMC) Budget $31.9 M
TAB Cochair - John Carruthers (Intel) UAC Chair - Ken Wise (Michigan)
GCC Chair - K. Speierman (NSA)

Jan - SRC joins CAD Framework Initiative, first SEMATECH Centers-of-Excellence established; Arizona/Contamination Control, Cal-Berkeley/Lithography, Massachusetts/Single Wafer Processing; New Jersey/Plasma Processing; New Mexico/Metrology; and Texas/Modeling of Unit Processes.

Feb - 7000 dial-in and E-mail linkups to SRC in 1988

- Washington meetings - Bob McMillin(GM), Joe Sitarik(SEMATECH), Pallab Chatterjee (TI), Frank Huband (NSF), and Larry Sumney (SRC), speak, in order, on "The New Era for SRC Research," "SRC/SEMATECH Cooperation," "Research Challenges," "World-wide Cooperative Research," & "Preparing for the Future"

May - Government Coordinating Committee comprehensive meeting - providing of non-threatening environments for government agencies and companies to discuss issues was identified as important SRC task.

Jun - BoD and ETAB join in SRC Strategy Forum to review past and provide guidance for the future SRC agenda, focused on "Silver Bullets and Silver Buds," and concluded that despite stress on peripheral areas, the underlying silicon integrated device technology must remain the core mission of the SRC.

Aug - Over 400 industry scientists/engineers are mentoring SRC research.

Sep - Summer study focuses on research goals: technology push; market pull; workstation, supercomputer, automotive; and research environment. Sources of potential paradigm shifts identified as high quality SOI wafers, enhanced software productivity, reduced cost for fab equipment, shared on-chip interconnects, high temperature devices, and object-oriented designs.

- Proceedings of the IEEE special issue on Cooperative Research edited by Bill Holton.

Nov - Congressional testimony re semiconductor research and government support by Sumney.

Dec - In 1989, about 80 research contracts were active.

New Members - MCC

Technical Meetings - Design for Manufacturability, Plasma Etch; Behavioral Synthesis Systems; Process Engineering Toolbox; SPECS (Circuit Simulation); CIM of ICs '89; ADAM- High-Level Synthesis; CAD Frameworks; Epitaxial Silicon Growth; Deposition Processes; BSIM 2 - Sumicron MOS Models; Macrocell Placement and Routing System; Submicron MOS Models and Parameter Extraction; Prediction of Electromigration in VLSI Circuits Using Noise Measurements as a Tool; Integrated Factory Management for IC Manufacture; Hierarchial Logic and Fault Simulator; BiCMOS

1990 Board Chair - Fred Schwettmann (HP) Budget $34 M
TAB Industry Cochair - Ed Hall (Motorola) UAC Chair - Ken Wise (Michigan)
GCC Chair - K. Speierman (NSA)

Mar - President Bush briefed on SRC at NCSU by Sumney

Jun - Bob Noyce who presided over the creation of the SRC in 1981, dies.

Aug - 1990 SRC Faculty Source Book published.

- SRC Summer Study focuses on technology, research operations, technology transfer, and operations strategies. A "bible-like" set of recommendations were given to SRC management. One of these was to get more resources ($) for the research program.

Oct - TECHCON '90 held in San Jose with a plenary session focused on competitiveness challenges. Gordon Moore spelled out the requirements for success in the global semiconductor competition noting the key role of

technology. Dr. Glashow, a Harvard physics Nobelist provided insight on the technology oriented education challenge and Congressman Mineta, by satellite hookup, noted the key importance of the semiconductor industry and thus of the SRC in his clarion call - "America needs a technology strategy for government and industry .....". Larry Sumney concluded by calling for reduced redundancy,
improved coordination, and increases in productivity, noting that the SRC was ready to do its part. More than 550 participants helped make TECHON "90 a huge success.

New member - ETEC Systems

Technical Meetings - Temperature Measurement in Single Wafer Processing; Integrated Technology Modeling; Gate Oxides; Mixed Analog/Digital Simulator; Metrology; Tech Transfer Best Practices; Interconnect Technology; Designing for Quality; Lithography; R&D Commercialization; System Level CAD; Logic and Fault Simulator; AWEsim Simulator; CIM for Ics; Analog Synthesis System; Synthesis of Testable Designs; Logic
Synthesis System; Microelectronics Manufacturing
Engineering; Integrated Semiconductor Representations for
Technology CAD; Monte Carlo Simulation of Electron Transport

1991 Board Chair - Gerhard Parker (Intel) Budget $34.1 M
TAB Industry Cochair - Steve Knight (AT&T) UAC Chair - Nino Masnari (NCSU)
GCC Chair - K. Speierman (NSA)

Feb - The theme of the SIA/SRC Washington meeting was "Toward a National Technology Strategy." Rep. George Brown, Chair of the House Science, Space, and Technology Committee voiced strong support of cooperative government-industry programs that buttress the Nation's technology base. His presentation was preceded by Larry Sumney calling for a vision, strategy, and leadership to assure U.S. technologyleadership. Following Brown, John Armstrong of IBM called for measures to maintain U.S. industry market leadership and described the technology workshop being sponsored by the National Advisory Committee on Semiconductors. Warren Davis of the SIA described that organization's technology initiative being formed under the leadership of Gordon Moore and called for a research effort that is better coordinated, more effective, and more efficient.

Apr - Micro Tech 2000 Workshop held in Research Triangle Park, NC with major SRC participation.

Jun - SRC establishes dedicated link on Internet.

Jul - In testimony for the House Technology and Competitiveness Subcommittee, Larry Sumney calls for increased support of cooperative research efforts.

Aug - At the Summer Study in Port Ludlow, the Technology Advisory Board stressed continued emphasis on university research and added the following recommendations: provide venues for discussion of strategic industry needs, expand management plan to include technology transfer, put executive summary
in every SRC report, focus on strengthening existing consortia, address technology transitioning needs, and develop strategy for obtaining new members.

Sep - New edition of SRC Management Plan issued with three parts: Mission and Outlook, Research Strategy, and Research Operations.

Nov - At SRC Fellows Banquet, Bill Warick, President of AT&T outlines industry technology challenges.

Meetings - Device Performance TCAD; TIMBERWOLF; Real Time Process Control; Reliability; Integration of Novel Processes; Position Measurement; Ion Beam Projection Lithography; Technology CAD; Package Analysis, Design, and Simulation; Formal Verification of Hardware; Microelectronic Manufacturing Education; Packaging Materials and Measurements; Contamination Issues in VLSI Manufacturing

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1992 Board Chair - Owen Williams (Motorola) Budget $37.6 M
Industry TAB Co-chair - Bob Doering (TI) UAC Chair - N. Masnari (NCSU)
GCC Chair - K. Speierman (NSA)

Jan - At beginning of SRC's second decade, electronic report distribution is initiated.

Feb - Changes resulting from SRC's first decade are summarized in a newsletter article.

Mar - Washington meeting plenary session features Dr. Gerhard Parkers enumeration of SRC accomplishments for the industry - strong membership, roadmaps, university partnership, research results, and eight additional products.

Ian Ross
described the 5 core recommendations by the NACS and Tim Valentine focused his remarks on the government's role in technology. Erich Bloch, first Chairman of the SRC, later NSF director, and now Council on Competitiveness fellow,
discussed education and competitiveness noting in closing that "The U.S. position in many critical technologies is slipping and, in some cases, has been lost altogether. Future trends are not encouraging."

- A joint meeting of the University Advisory Committee and the Technical Advisory Board generates recommendations on improving the mentor program, communications and relations with principal investigators, and the research review process.

Apr - A survey by the Roper organization indicates strong public support for technology with two-thirds favoring a strong government role.

May - At a Washington meeting, industry execs identify SRC research results - simulation programs, design-stage reliability models, circuit designs, tools for timing analysis in chip design - as providing a %250 return on investment.

Jun - Tenth anniversary dinner - Owen Willims sets SRC goal as being the best research management organization in existence.

Aug - Summer study in Santa Fe focuses on strategic planning, the role of the National Labs, the SIA technology roadmap process, the extended planning horizon, and long term/high risk research were subjects of presentations. Strong recommendations were made to integrate universities and national laboratories in the technology planning process.

Nov - SIA Semiconductor Technology Workshop leading to first SIA Roadmap.

Dec - Wollesen rule on chip cost: 1/3 to design and fab, 1/3 to packaging, and 1/3 to testing is reported in the newsletter. At IEDM and Interface Specialists conferences, over half of university papers report on SRC supported research.

New members - Northern Telecom

Meetings - SOI Technology; Berkeley Reliability Tool; Contamination Control; Silicon-Germanium Technology; Plasma Etch; TCAD; Cobalt Silicide Technology; CAD for Ics; Power Ics; Floating-Gate NVM Research; Multilevel Interconnect Technology; Chem-mechanical Polishing for Planarization; Packaging Materials and Measurements; A Low Pressure Deposition Simulator; IC Package Design Analysis & Simulation Systems; RICE Timing Simulation Software; Process Control Measurements for Advanced IC Manufacturing; CARAFE Software System

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1993 Board Chair - Bill Siegle (AMD)
TAB Industry Cochair - Bob Doering (TI)
Budget $36.8 M
UAC Chair - Tim Trick (ILL)
GCC Chair - Gerald Iafrate (ARO)

Mar - MIT designated as CoE for Microsystem Technologies.

- At the annual SIA/SRC meetings in Washington , the plenary session focus was "Unifying Our Vision for Economic Competitiveness." Owen Williams opened with a discussion of the Roadmap. He noted that "it is phenomenal that we could all agree on a set of technology roadmaps for our industry .." Bill Siegle than noted that "one of the things initiated by the SRC ....was a very effective Total Quality Management program." Senator Bingaman spoke on "America and Competitiveness" suggesting that the technological infrastructure works best when it is clustered regionally. He espoused support for a flexible and regenerating economy. Finally, Kent Hughes, President of the Council on Competitiveness discussed the challenges associated with education and competitiveness - ranging from kindergarten to continuing education. In Larry Sumney's presentation on "Competitiveness and the SRC Model," he summarized by his vision for the future of the industry was a bright one based on the bright young people entering the workforce and the unity of the industry.

Jun - Tenth anniversary of SRC's Industrial Mentor program with over 500 mentors participating - feedback on this aspect of the SRC is highly favorable.

Aug - An enhanced SRC mission statement is described by Sumney in the SRC Newsletter. It consists of the technical challenge: keep the U.S. industry ahead; the SRC goals: do responsive research, relate to others similarly engaged, and obtain maximum return on industry's investment. These goals are
further broken down in a list of more specific objectives.

- At SRC 1993 Summer Study in Park City, the theme was "Enhancing the University Research Program." Bill Holton, Joe Ballantyne (Cornell), Frank Oettinger (NIST), Linton Salmon (NSF), and Linda Gardner addressed this theme from
various perspectives after which the TAB generated a strategy for enhancement. This included an industry internship for faculty before beginning a teaching career, generation of good ideas, a structure for improved

research coordination, and structures for improved research productivity. Sumney stated in the conclusion that the correctness of old paradigms can no longer be assumed.

Sep - TECHCON '93 Atlanta. The plenary session provided outstanding speakers with a variety of perspectives - a senior policy fellow from the Office of Science and Technology Policy, Cynthia McKenna, who praised the SRC as a successful model for stimulating dialogue and formulating a program. Craig Barrett of Intel forecast a continued validity of Moore's Law, noted the global challenge to technology leadership, and described the U.S. industry's response. Larry Monteith of NCSU provided the academic viewpoint noting that universities must change as their mission changes - as exemplified by the SRC research program. Sumney, in his remarks, noted the progression to consortia and roadmaps as essential for addressing today's goals. Bill Siegle, as anchor man for the plenary discussions, noted the necessity for maintaining the goal structure as provided by the Roadmap and defined the roles of the various customers of the Roadmap.

Meetings - Ordered Binary Decision Diagrams in CAD Programming; Simulation of Optical and X-ray Lithography; Statistical Optimization for Quality; Copper Interconnect Technology Genetic Test Cultivation Program for Sequential VLSI Circuits; Object-Oriented Device and Process Simulators; Design of Oversampling A/D & D/A Converters in CMOS VLSI; Physically Based Models of RTP Equipment; Technology Insertion; BSIM3; EOS/ESD in VLSI IO Circuits; Device Performance TCAD

1994 Board Chairs - Dan Fleming(IBM — Budget $37.4 M
Owen Williams (Motorola) — UAC Chair - Tim Trick (ILL)
TAB Industry Cochair - Don Wollesen (AMD) — GCC Chair - Gerald Iafrate (ARO)

Jan - Armstrong article in Spectrum identifies SRC as leading cooperative organization.

Feb - Every member of SRC technical staff is given Roadmap-94 assignment.

Mar - Changes in the format of the Washington meeting resulted in discontinuation of the 10-year tradition of a joint plenary session. The University Advisory Committee discussed the Roadmap process, improving the mentor program was the focus of a joint ETAB/UAC meeting, the ETAB focused on the Modeling and Simulation CRADA, the University Advisory Committee reviewed its role and function, and the Board of Directors conducted a typical busy meeting with a focus on the CRADA and the planned Board retreat.

Jun - 240 people join efforts in 1994 Roadmap Workshop. The course was determined and the challenges identified for advancing integrated circuit technology for the next fifteen years.

Jul - The SRC Summer Study focused on "customer satisfaction" with papers on evaluation of SRC activities, minimizing the research-to-commercialization cycle, technology and knowledge transfer, and research process differences. New approaches were generated in each of these areas and strategies adopted.

Sep - Strategic planning retreat of Board results in plethora of ideas in four areas: 1) university directions and methods, 2) technology transfer, 3) revenue base, and 4) mission and operations. 22 issues were identified for further study and discussion.

Nov - Graduate fellowship conference hears Bill Siegle speak on "Technology Challenges for the Twenty-first Century" noting that volume production of 0.25 micron ICs was expected in 2000. (Sorry Bill, in 1996, people were already starting to produce 0.18 stuff. We were all wrong.)

New members - National laboratories (Lawrence Berkeley, Lawrence Livermore, Los Alamos, Oak Ridge, Sandia)

Meetings - SpecCharts and SpecSyn Environment; ULSI Routing Framework; Full Wafer Interferometry; Physical Circuit Models for Power ASIC Design; Critical Issues for Gate Dielectric Integration; EVOLVE v4,0; ACACIA; Critical Issues for Advanced Imaging Materials; Lithography and Topography Simulation; Low Dielectric Constant Interlayer Dielectrics for High Performance Circuits; Direct Liquid Injection for
Advanced CVD Processing; Models for Process Simulation; Silicon Wafer Bonding for Micromechanical Devices; Future of Digital ICs: Alternatives to a Continuation of Technology Shrink.

1995 Board Chair - Owen Williams (Motorola) — Budget $36.5 M
TAB Cochair - Ashok Kapoor(LSI Logic) — UAC Chair - Joe Ballantyne (Cornell)
GCC Chair - Gerald Iafrate (ARO)

Jan - Center for Semiconductor Simulation and Modeling established through Cooperative Research and Development Agreement with National Laboratories.

Feb - SRC research reorganized to correspond to Roadmap structure.
Mar - Don Pederson given SIA award for his SRC research.
Apr - Semiconductor R&D catechism given in newsletter:
1) SEMICONDUCTORS ARE SEMINAL,
2) INDUSTRY LEADERSHIP IS IMPORTANT,
3) STRUCTURE OF U.S. SEMICONDUCTOR R&D HAS CHANGED,
4) U.S. LEADERSHIP IS CHALLENGED,
5) ROLES/RESPONSIBILITIES OF PARTICIPANTS IS KEY, AND
6) RESEARCH INFRASTRUCTURE APPEARS INADEQUATE.
May - SRC day at NIST results in identification of mutual interests.
Jun - NSF and SRC announce intention to establish jointly funded Engineering Research Center.
Jul - SRC launches electronic research catalog making research results instantly available to all members.
Aug - Summer study - research opportunities in system integration, research prioritization, critical challenges and research efficiency in IC design, role of the infrastructure in SRC's research agenda, and encouraging innovation - these were the titles of the prepared presentations. In abstract form, the ETAB identified the challenges as follows: integrated systems - the ability to
produce a cost-effective assembly of system components with uncompromised functionality, design - organize design summit for improved design roadmap, innovation - increase satisfaction of industry customers with the innovation and accountability of university research, research efficiency - maximize satisfaction with output of university researchers and industry customers.

New Members - Cadence Design Systems, duPont, Ford, Novellus Systems, Shipley.

Technical Meetings - Statistical Design; GOSSIP; PICES DUET; SOI MOSFET Models in SOISSPICE; Formal Verification; Chemical-Mechanical Polishing II; SWEC Circuit Simulator; Short-Channel IGFET Models; Transient-Enhanced Diffusion Analysis
Using FASTCAP, FASTHENRY, & MEMCAD; Modeling Multilevel Metallization CVD Processes; Interconnect Resistance and Capacitance; Sensing/Simulation for Environmentally Conscious Manufacturing; Perfluorocarbon & Chlorofluorocarbon Emissions
& Abatement; Alternative Chemistries to Perfluorocompounds

1996 Board Chair - Charles Carinalli (NSC) -> June - Mark Melliar-Smith (ATT/Lucent)
TAB Industry Cochair - John Pierce (NSC)
Budget $39.
UAC Chair - Joe Ballantyne (Cornell)
GCC Chair - Gerald Iafrate (ARO)

Jan - NSF and SRC announce first jointly supported and operated Engineering Research Center - the Center for Environmentally Benign Manufacturing at the University of Arizona with participation of Stanford, UC- Berkeley, and MIT.
- A product of SRC design sciences research, BSIM3v3, is selected as standard compact MESFET model for circuit simulation.
Feb - First Center for Semiconductor Modeling and Simulation review by participants; SRC, SEMATECH, universities, and national laboratories.
- Results of Member Satisfaction and S-TAB surveys announced in Newsletter.
Mar - John Gibbons of Stanford presented with 1996 SIA Unversity Research Award.
Jun - SRC Technical Excellence Awards presented to CMU team for Symbolic Model Verifier and to UCLA team for research on post-shrink silicon device structures.
- SRC Web page provides members with rapid access to research results.
Jul - New CoE in Advanced Interconnect Science and Technology established at RPI, cooperative funding of $3 million/year.
Sep - TECHCON 96 with 28 parallel sessions, 500 attendees in Phoenix.
- Graduate Fellowship Program Conference
- First Aristotle Award presented to Steve Director
Oct - Focus Center Research Program authorized by SRC Board.
Nov - SRC Master's Scholarship Program initiated.
Dec - Final issue of SRC Newsletter.

New Members - Northrup-Grumman, Lucent Technologies, LV Software, Inc.; Microunity Systems Engineering, Inc.; and SiBond, L.L.C.

Technical Meetings - Advanced Surface Preparation, Ultrapure Water Techniques, Ultrathin Gate Dielectrics, Gas-Phase Cleaning of Silicon Wafers, Charged Beam Patterning, Power Estimation, EOS/ESD Design Simulation, Electromigration Simulation, Copper Interconnect Technology, TECHCON'96, Level 2 Packaging, Florida Object-Oriented Process Simulator (FLOOPS), 2D Dopant Profiling, Contamination-Defect-Fault Mapping Tool.

APPENDIX F

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APPENDIX G

HONORS AND AWARDS

TECHNICAL EXCELLENCE AWARDS

William Oldham Richard Schenker Fan Piao	UCB	1997	Ultraviolet Damage To Fused Silica
Grant Wilson Tsutomu Shimokawa Uzoodinma Okoroanyanwu Kyle Patterson David Mederos	Texas	1996	Advanced Resists
Randall Bryant Edmund Clarke Kenneth McMillan	CMU	1995	Formal Verification Techniques
Kang Wang Martin Tanner, Shawn Thomas Xingyu Zheng, Timothy Carns	UCLA	1995	Si-Based Quantum Structures
Carl Sechen William Swartz	Yale (Washington)	1994	Layout optimization
Mark Kushner Peter Ventzek Seung Choi, Robert Hoekstra	Illinois	1994	Modeling of Plasma Reactors
Joe Greene Lucia Markert	Illinois	1993	Ion Doping during Film Growth
Mark Law Heemyong Park Chih-Chuan Lin, Minchang Liang Stephen Cea	Florida	1993	Device and Process Simulation
Thomas M. Miemczyk David M. Haaland David K. Melgaard	New Mexico Sandia	1992	Chemometrics for the Analysis of Dielectric Films
Wojciech Maly	CMU	1992	IDDQ Testing and the Thomas Storey Quality of IC Test
Al F. Tasch, Jr. Christine M. Maziar, H. Shin	Texas	1991	MOSFET Structure for Deep Submicron ULSI Processes
Ronald A. Rohrer Lawrence Pillage	CMU	1991	Asymptotic Waveform Estimator(AWE)
Fahang Shadman Robert A. Governal Asad M. Haider, Alison Bonner	Arizona	1991	Contamination Control In Gases and Liquids
Chemming Hu Ping K. Ko, Peter M. Lee Boon-Dhim Liew, Elyse Rosenbaum, J. David Burnett	UCB	1991	Berkeley Reliability Tool(BERT)

OUTSTANDING INDUSTRIAL MENTOR AWARDS

Robert Aitken	HP	UC-Santa Cruz	1998
Laurie Beu	Motorola	MIT	1998
Martin Giles	Intel	Florida	1998
Effiong Ibok	AMD	NCSU	1998
Sungho Jin	Lucent	Northwestern	1998
Alexander Liddle	Lucent	Wisconsin	1998
Martin Giles	Intel	Stamford	1997
Ted Kamins	HP	Cornell	1997
Linda Milor	AMD	CMU	1997
John Sauber	DEC	Ohio State	1997
Denise Puisto	IBM	Wisconsin	1997
Bradley Van Eck	SEMATECH	Minnesota	1997
T. M. Mak	Intel	UC-Santa Cruz	1997
Erik Egan	Motorola	MIT	1996
Avtar Jassal	SEMATECH	Arizona/Texas-Austin	1996
Paul Packan	Intel	Florida	1996
Karl Puttlitz	IBM	Northwestern	1996
Mario Pelella	IBM	Florida	1996
Rob Ramage	Intel	Texas-Austin	1996
Deo Singh	Intel	USC	1996
Noel Strader	Motorola	UC-Berkeley	1995
Kathy Early	AMD	Wisconsin	1995
Tracy Boswell	SEMATECH	Arizona	1995
Hsing-Huang Tseng	Motorola	Yale	1995
E. Hal Bogardus	SEMATECH	UC-Berkeley	1995
Steven Groothuis	TI	Ohio State	1995
Charvaka Duvvur	TI	Illinois	1994
William Johnson	Motorola	Wisconsin	1994
Robert Simonton	Eaton	Texas-Austin	1994
Rick Scott	SEMATECH	Texas A&M	1994
Rex Lowther	Harris	Florida	1994
Ravi Kaw	HP	Arizona	1994
Robert P. Larsen	Rockwell	UC-Irwin/CMU	1993
Thomas E. Zirkle	Motorola	Arizona State	1993
Peng Fang	AMD	UC-Berkeley	1993
Herbert A. Lord	AT&T	Colorado	1993
Tien Y. Wu	IBM	Ohio State	1993
Don Sharfetter	Intel	Texas-Austin	1992
Sury Maturi	National	Yale	1992
Jack Linn	Harris	New Mexico	1992
George Katopis	IBM	Arizona	1992
John Andrews	National	CMU	1990
Bruce Beltman	Harris	So. Florida	1990
David Abercrombie	Harris	NCSU	1990
William Starks	Varian	Michigan	1990
Walling Cyre	CDC	ILLinois	1988
Frederick Dill	IBM	UC-Berkeley	1988
George Rouse	Harris	Purdue	1988
Mali Mahalingam	Motorola	Purdue	1988

ARISTOTLE AWARD

Franco Cerrina	Wisconsin-Madison	1998
Joseph Greene	Illinois	1998
Kensall Wise	Michigan	1997
Steve Director	CMU	1996