Some (possibly controversial) thoughts

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The right questions are formulated. One could start suggestions for solutions for each one of them…But I am not sure that the problem today is ONLY a scientific or technical issue. I do believe it is in the first place an economical, perceptive, organizational and political issue.

1. Economical

EDA industry is 6 B$, 200 B$ semicon depends on it and on that a 5000B$ service and system industry relies. This makes the EDA dwarf essential for the existence and further growth of the ICT industry. But, at the same time it makes it also an extremely vulnerable system as the "small" size, huge development costs and small margins lead to the point that the financial world (VC and co) is not much interested in it or only in those aspects that TODAY are crucial for the semi industry (such as DFM). Long term perspectives addressing ultimate CMOS designs are not funded and are not sexy with funding agencies (sofar). This has to do with perception:

2. Perceptive, sociology, society view.

The attractiveness of "More Moore" to the public and the young researcher is rapidly decreasing. The message became boring and complexity is not something handled by the value given to the individualistic achievement in western society. Result: western (and Japanese) students are either moving to more lucrative law (IP rights!), economics or (bio)medical studies. Asian students in view of their more collective culture and drive to achieve a higher economical status are choosing massively for technology and work 7days/12 hours/day.

In addition funding agencies are much more driven (and justly so in my view) by the system level "collection" of ICT devices delivering services to societal issues rather than by the IC component itself that we proudly want to hide in the pervasive computing of ambient intelligence. Further coping with ultimate scaling looks like a self-destructive optimism. As a result of a clear(?) scaling roadmap, funding agencies begin to consider scaling too much from the physical device level and the development of process technology. The motto is: "If we support the physics of the process technology all issues will be solved". *Evidently they oversee the fact that further scaling is not business as usual...hence:*

3. The need for a long term perspective and public investment in guided DA research

Whereas, so far, process technology scaling introduces a new node every two years, design methodology changes occur only every 7 years. Therefore relevant design technology research, funded by public money today, must address at least the 22 or 16 nm nodes. *So we must start by analysing what kind of complexity and application domains need to be served and what the implications of scaling will be on architectures serving these applications. Otherwise we may be shooting in the dark and ROI of research will be limited. First one has to understand the issues (by doing!), create skilled people and only after that can tools emerge. Tools are no solution right now.*

A few possible scenarios for future products (in ultimate CMOS):

1. Further expansion of servers and microprocessors to homogeneous deca-core systems at Teraflop level: maybe 2 players left in the world? Who must develop tools for them? Public or private?
2. Further expansion of heterogeneous multi-core platforms with networks on chip and embedded software for consumer oriented ambient intelligence nodes

(stationary (car, home, games, and office.) and nomadic (universal personal assistant). Two possibilities:

   a. Use ultimate technology capability for more compute/communication power: leads in 2015 to more than 1B$ NRE costs of which at least 2/3 is software and middleware development / platform *if nothing is done to increase design productivity*. But, again only a few players will be left in this field, potentially fab-less companies. Same question as above or not?
   b. Use scaling for cost reduction of existing or new simple functions and use 3D integration for system integration: use existing tools or develop new ones to redesign in scaled technology. NRE Cost reduction is the key driver.

3. Chips for sensor and actuator nodes in a transducer network:

   These are ultra cheap, ultra-low power micro- or nanosystems for which there are very few tools and models available as each design encompasses electrical and non-electrical effects (e.g. 3D integration, fluidics, photonics, (bio)chemistry, mechanics…). Process technology is 2, 3 generations beyond state of the art but ultimately will catch up when nano sensors pop up. Many small fab-lite companies may appear in this domain. *They need tools but in the first place ultra-creative engineers with broad skills to cope with a plethora of technologies.*

Categories 1 and certainly 2 require a serious effort in long term EDA research for the following reasons:

1. Further scaling is not business as usual. Leakage and dynamic power management, variability resilience, on- off chip interconnect issues, signal integrity, fault tolerance, reliability, litho-effects on layout style, new device architectures, new materials *all occur at the same time and affect the complete design process and the nature of future architectures. The living apart together days of happy scaling are over and new "Technology Aware Design" (TAD) techniques are needed that reestablish a decoupling by new abstraction methodologies for ultimate CMOS (22…16nm). This is only possible by cross-disciplinary open innovation LT research from systems to atoms by a tight interaction of industry, universities and research institutes.*

2. ESL is needed desperately but is very domain and architecture specific (hence little ROI) and requires a considerable amount of *training and education aspects,* which is not business as usual. *Universities must produce skilled brainpower* but have *difficulties to do realistic system level design in ultimate CMOS technology.* As a result, today's EDA industry focuses on DFM with an emphasis on OPC, RET and MCP effects since this is *generic technology for all silicon foundries without which further scaling will stop* (as long as we do not have EUV litho as will be the case for 22…16nm?). Hence ROI for DFM software can be achieved. However too little attention is paid to ESL and certainly not to the impact of device variability, signal integrity, on-chip communication (networking) (TAD

3. Especially category 2 is a huge challenge as the metrics are daunting: energy efficiency >100 Gop/Joule yet eSW programmable, < 10$ ASP, memory intensive, heterogeneous mixed-signal architecture, 3D packaging while coping with the above physical aspects.

So my 3 challenges:

1. Create methods and tools as well as design skills to map (download) multiple embedded software applications on a single co-designed flexible yet energy efficient and scaling tolerant (22...16nm) heterogeneous multi-core platform satisfying the above challenging metrics.
Bottleneck: domain and architecture specificity, lack of ROI.

2. Establish and organize cross-disciplinary research in "technology aware design" for ultimate CMOS form systems to atoms. Goal must be to improve design productivity by at least one order of magnitude by reestablishing a separation of concern methodology for eSW ultimate CMOS architectures, producing the skills to execute it and applying them to realistic examples in categories 2a,b. Can only by a tight cooperation between industry, academy of scale covering the complete value chain and research institutes. Sense of urgency: be ready 7 years from now.

3. For nano-sensor networks system level design methodologies there is a definite need to set-up a design methodology and modeling effort for ultra low cost, ultra low power heterogeneous nano-systems. Problem here is how to cope with diversity and domain specificity again.

Bottom line is: we are entering a world of uncertainties at which time not tools but skilled people and system architects are most important. This is hard to establish in the actual academic world in view of the complexity of the issues. This requires a reorganization of research on which I have a few suggestions that go a bit beyond this text but are quite consistent with some trends already followed by SRC today and with the concept of "poles de competitivite" now emerging in Europe.

Status Today

- ESL = Electronic System Level (Design Tools)
  - Not focus of large EDA, mainly start-ups
  - Issue: diversity, new hw/sw culture (edu!), ROI risk
  - EDA's fear training and edu aspects
  - But ESL skills and tools will be future bottleneck
- DFM= Design for Manufacturablity
  - Without it scaling breaks down hence M€ business now
  - Focal point of large EDA vendors (16 DFM cies…)
  - Focus on Litho RET, CMP and Statistical timing. What if EUV at ultimate CMOS?
- TAD = Technology Aware Design
  - How to abstract leakage, variability to design level
  - An emerging domain of research esential for ultimate CMOS