A Forum on Future Directions for Design Automation Research

Juan C. Rey Senior Director Of Engineering Design to Silicon Division Mentor Graphics Corporation

October, 2006

10:30Panel 2Increased Uncertainty

- Are there fundamentals that will support design at all levels for IC's whose internal properties vary widely?
- What approaches can design automation apply to resilient systems, designing reliable systems from unreliable elements?
- Can/should design and manufacturing be more tightly integrated? If so, what methods might be successful?
- What test strategies should be employed for extraordinarily complex systems with new defect modes?

Definitions:

One of the key interfaces between the integrated circuit design activity and its manufacturing in a semiconductor operation is through the artwork represented in the integrated circuit design layout.

Several activities need to be performed on the layout itself to verify its compliance to manufacturing rules, analyze and change the layout to improve its manufacturing yield, and in the future analyze and improve its reliability.

Position:

A brief description will be provided to describe the typical activities currently performed once an integrated circuit layout is completed with a description about how process limitations are analyzed and compensated. It will be followed by a description of the type of activities that could be required in the future due enable manufacturing as well as improve reliability. Here, the trend towards models (as opposed to rules) will be highlighted.

A description of research needs will be presented on the following areas:

1) Computer Science Research: to produce computationally efficient techniques to process layout data (for analysis and modifications)

2) Engineering/Computer Science Research: to produce models that describe processes and device behavior that can be applied at full chip level (as opposed to the microscopic level)

3) Engineering/Physics/Chemistry Research: to develop an understanding and derive modeling techniques that accurately describes failure mechanisms for device and interconnects of integrated circuits.