Future Directions in Design Automation

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Will there be a greater or smaller variety of electronic chips a decade from now?

There is a dramatic decrease in the number of new chip starts in industry as compared to six years ago, partly because of the escalating cost of chip design. On the other hand it is almost certain that there will be orders of magnitude more hand-held devices and sensors in our environment in future. These devices will be severely power-constrained and cost-constrained. The only way to dramatically reduce power consumption of an application is to implement it using specialized hardware as opposed to as a program on a microprocessor. So there is huge economic incentive to produce a great variety of chips but this can happen only if we can figure out how to design new chips and associated software economically.

A fundamental shift is needed in the current design-flow of systems-on-a-chip. The research focus has to shift from post-design verification of increasingly complex systems to methodologies that permit rapid development of complex systems by composing pre-tested, existing modules. Following is a partial list of topics that EDA research should focus on:

- Higher-level design methodologies to increase the capability of a fixed-size design team to produce order of magnitude larger or more complex systems

- Methods of specifying and producing reusable components. For example, there should be a description available for a video codec such as H.264 so that it can be *refined* into hardware or software or any other implementation technology as needed.

- Systems for doing rapid micro-architectural exploration to understand power-area tradeoffs and hardware-software tradeoffs. We need to move away from the "batch-oriented" mentality of SoC design to a more "interactive" design style where the designer can rapidly try different alternatives.

- Design systems which will make it easy for the designers (without PhDs in Formal Methods) to assert and prove some properties of the design.

I believe such design issues are far more important from research point of view than the physical design issues that are likely to arise in sub-nanometer technologies. In my opinion Semiconductor industry is in a much better position to tell us how to deal with uncertainty and unreliability of the underlying substrate. The level of physical unreliability that the designers of complex systems will have to deal with is likely to be dwarfed by the level of functional unreliability of their design components.