Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

global RESEARCH COLLABORATION

Emerging Research Devices for Added Functionality

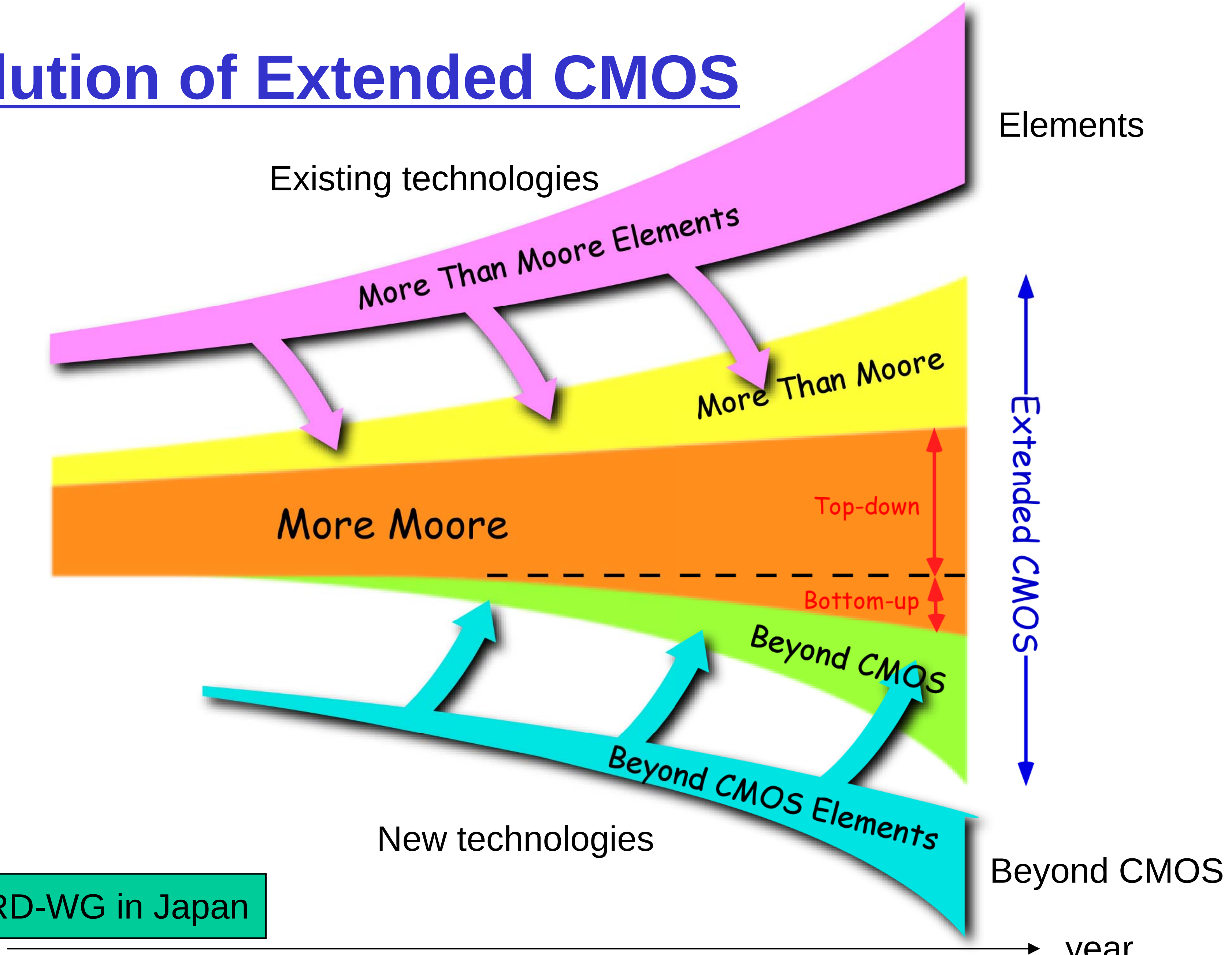
SRC / NSF Forum on Nano-Morphic Systems

Jim Hutchby

Semiconductor Research Corporation

Stanford University, November 8 - 9, 2007

Evolution of Extended CMOS



ERD-WG in Japan

Control Logic Unit for Autonomous Micro-Scale Systems

$$n_{\max} \sim \frac{1}{20 L_g^{\,2}} \sim 10^{10}\, cm^{-2}$$

L_g~5nm!

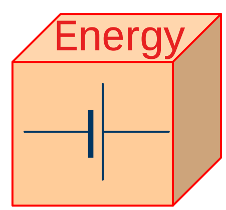
$$N_{tr} = 10^{10} \cdot \left(10^{-3}\right)^2 = 10{,}000$$

Intel 8080 (5000 trans)

Aggressive scaling is mandatory for µ-scale systems

In principle, the full MPU capabilities can be realized within 10um square if we can sustain scaling to ultimate CMOS (~5 nm gate lengths)

Beyond-CMOS devices for more functionality at less device count?



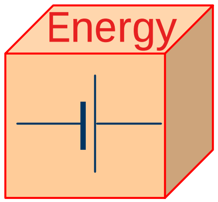
E_{bit}~$2x10^{-18}$ J/bit

$$E \sim 10^{-5}\, J$$

Max number of binary transitions

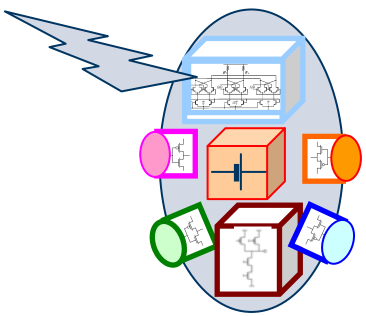
~$5x10^{12}$

Energetics of an Autonomous Micron-Scale System



TOTAL

$$E \sim (10^{-3} cm)^3 \cdot 10^4 \sim 10^{-5} J$$



Per Bit

$E_{bit} \sim 500 k_B T$
$2x10^{-18}$ J/bit

$$N = \frac{E_{total}}{E_{bit}} \sim$$

10^{12} equivalent binary transitions

Control Logic

$\sim 10^4$ transistors
$\sim 5x10^{12}$ binary transitions

$\sim 10^{-18}$ J/bit

Communication

~4000 transmitted bits

$\sim 10^{-9}$ J/bit

Communication is costly

Sensing

Min size ~ 5 nm

$\sim 10^{-18}$ J/bit

Summary: Extreme Microsystems

- Extremely-scaled CMOS technology should support computation and control for the ten micron cube
  - Beyond CMOS devices may offer more functionality at lower device count
- Technology issues aside, it appears that a careful atomic-level trade-off could yield a functional system.
- Micron-scale energy sources are key to extreme microsystems
  - Design space is bounded by the limits of electrochemical sources
  - Alternative energy sources should be investigated
- Communication energy/volume expenditures is most costly activity – should therefore maximize “system intelligence”
- Potential for arrays of nano-scale sensors needs further exploration

Summary: Extreme Microsystems

- Communication energy/volume expenditures is most costly activity – should therefore maximize “system intelligence”

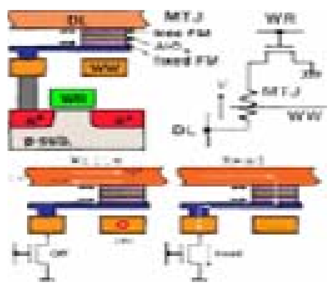
Question

How might Emerging Research Devices and Architectures best enable Extreme Microsystem functions?

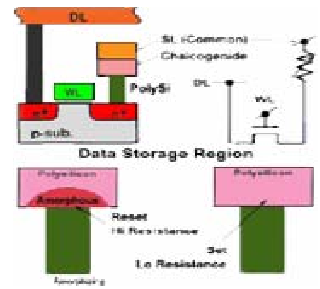
Emerging Research and Prototype Memory Technologies

Resistive Memories 1T1R or 1DIR

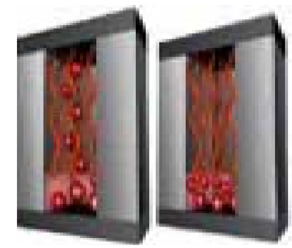
MRAM



PCRAM

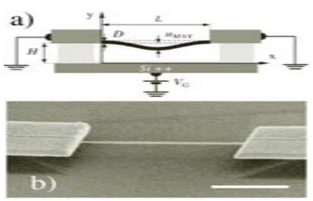


Polymer

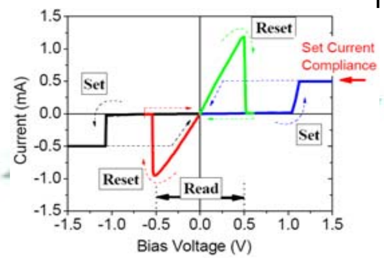


Molecular

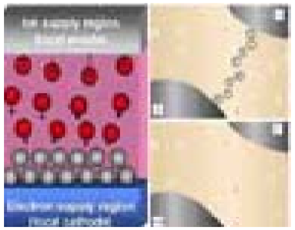
Nano Mechanical



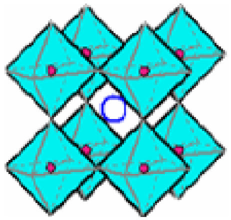
Fuse/Anti-fuse



PMC/Ionic

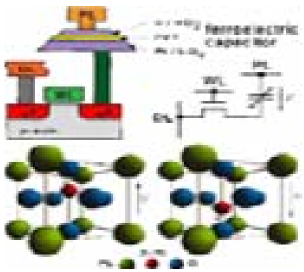


Electronic Effects Perovskite

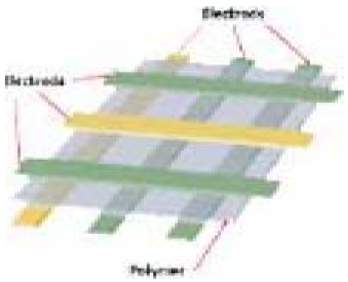


Capacitive Memories 1T1C & 1T

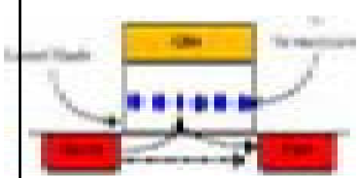
FeRAM & FeFET



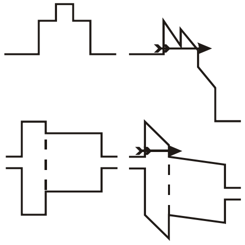
PFRAM



NanoX'tal



Eng Tunnel Barrier



> 20	>16 - 18
>18 - 20	≤ 16

2007 ITRS ERD Chapter

Capacitance-based memory technologies

	Engineered tunnel barrier Memory	Ferroelectric FET Memory
Storage Mechanism	Charge on floating gate	Remnant polarization on a ferroelectric gate dielectric
Cell Elements	1T	1T
Device Types	Graded insulator	FET with FE gate insulator

> 20	>16 - 18
>18 - 20	≤ 16

2007 ITRS ERD Chapter

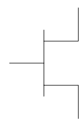
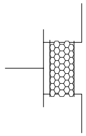
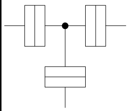
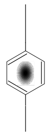
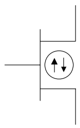
Resistance-based memory technologies

	Nanomechanical memory	Fuse/Anti fuse Memory	Ionic Memory	Electronic effects Memory	Polymer Memory	Molecular Memories
Storage Mechanism	Electrostatically-controlled bi-stable mechanical switch	Multiple mechanisms	Ion transport in solids	Multiple mechanisms	Not known	Not known
Cell Elements	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
Device Types	CNT bridge CNT cantilever Si cantilever Nanoparticle	M -I-M e.g. Pt/NiO/Pt	1) Solid Electrolyte 2) RedOx reaction	1) Charge trapping 2) Mott transition 3) FE Barrier effects	M-I-M (nc)-I-M	Bi-stable switch

> 20	>16 - 18
>18 - 20	≤ 16

2007 ITRS ERD

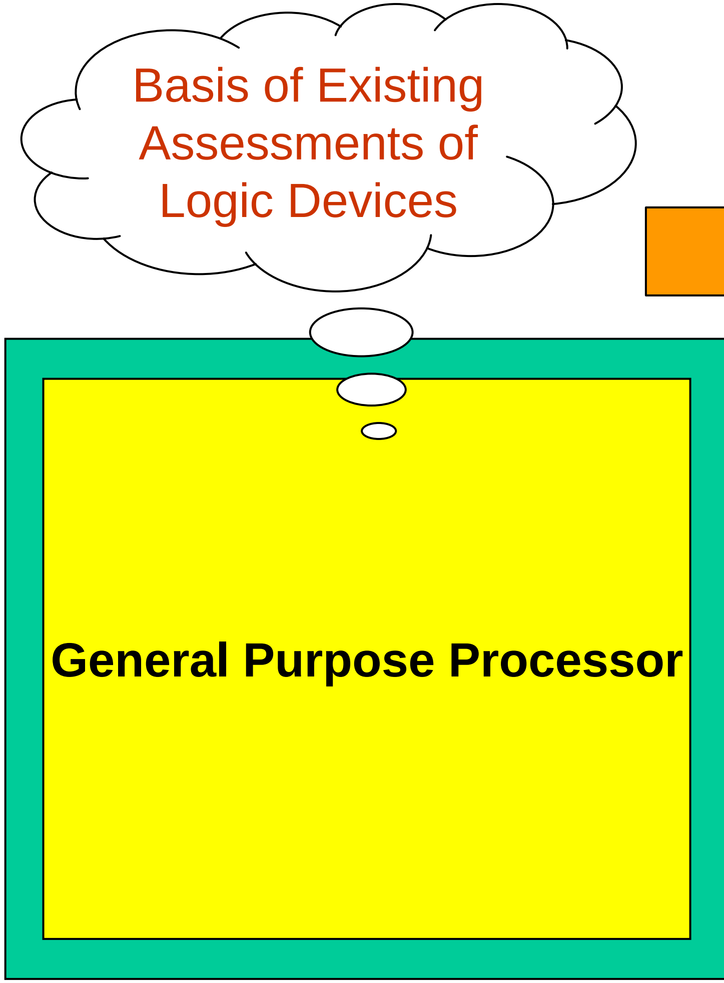
CMOS Scaling & Replacement Emerging Research Logic Devices

Device							
	FET	*CMOS Extension Low dimensional structures*	*CMOS Extension III-V channel replacement*	*SET*	*Molecular*	*Ferromagnetic logic*	*Spin transistor*
Types	Si CMOS	•CNT FET •NW FET •NW hetero-structures •Nanoribbon transistors	•III-V compound semiconductor channel replacement	SET	•2-terminal •3-terminal FET •3-terminal bipolar transistor •NEMS •Molecular QCA	•Moving domain wall •Hybrid Hall effect •Magnetic Resistive Element •M: QCA	•Spin Gain transistor •HMF Spin MOSFET •Spin Torque Transistor
Supported Architectures	Conventional	Conventional	Conventional	Threshold logic	Memory-based QCA	Lithographically defined	conventional

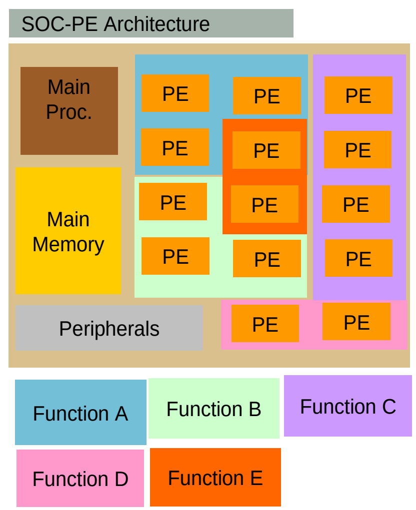
Emerging Research Logic Device Conclusions

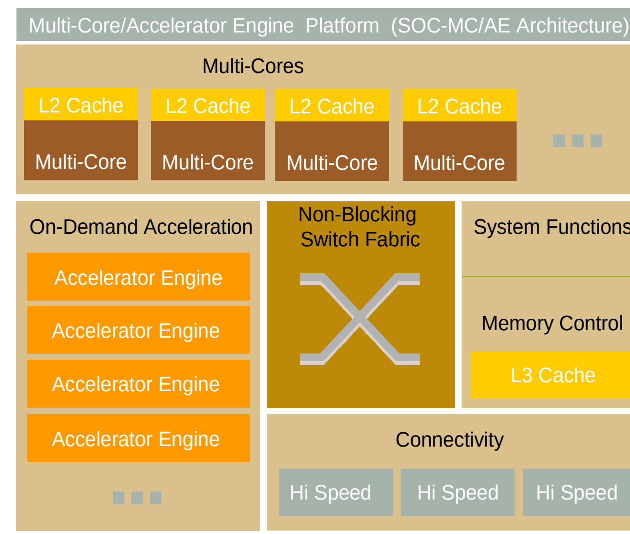
- Continued analysis of alternative technology entries likely will continue to yield the same result:
  - **Nothing beats MOSFETs overall for performing Boolean logic operations at comparable risk levels**
- Certain functions, e.g. image recognition (associative processing), may be more efficiently done in networks of non-linear devices rather than Boolean logic gates

Supplementing CMOS



A possible ultimate evolution of **on-chip** architectures is Asynchronous ***Heterogeneous*** Multi-Core with Hierarchical Processors Organization

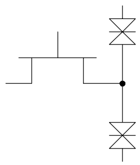
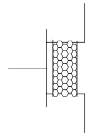
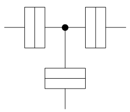
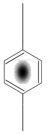
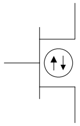




Courtesy Fawzi Behmann - Freescale

2007 ITRS ERD

CMOS Supplement Devices

						
Device	Resonant tunneling diodes	Muti ferroic tunnel junctions	Single Electron Transistors	Molecular devices	Ferro-magnetic devices	Frequency coherent spin devices
State variable	Charge	Dielectric and magnetic domain polarization	Charge	Molecular Conformation	Ferromagnetic polarization	Precession frequency
Response function	Negative differential resistance	Four resistive states	Coulomb blockade	Hysteritic	Non-linear	Nonlinear

Emerging Research Architectures

Architecture	Implementation	Computational Elements	Network	Application	Research Activity
Homogeneous Many-Core	Symmetric cores	CMOS	Irregular/ Fixed	Synthesis/GPP	
Heterogeneous	Asymmetric cores	CMOS	Irregular/ Fixed	Synthesis/GPP	
	CMOL	CMOS+Molecular Switches	Irregular/ Fixed	Synthesis/GPP	
	Molecular Cross-bar	Molecular Switches	Regular/ Flexible	Synthesis/GPP	
	Check-point	CMOS+ Ferromagnetic logic	Irregular/ Fixed	Synthesis/GPP	
Morphic	CNN	CMOS+Sensors	Regular/ Flexible	Recognition/Vision	
	AMP	FG-FET, SET	Irregular/ Fixed	Recognition/Vision	
	Bio-inspired	MFDT, Spin-gain transistor	Mixed	Recognition Mining Synthesis	

CMOL – ‘Molecule on CMOS’ architecture
CNN – Cellular Nonlinear Network
AMP – Associative Memory Processor

GPP – General Purpose Processor
FG-MOS – Floating Gate MOS devices
SET – single electron transistor

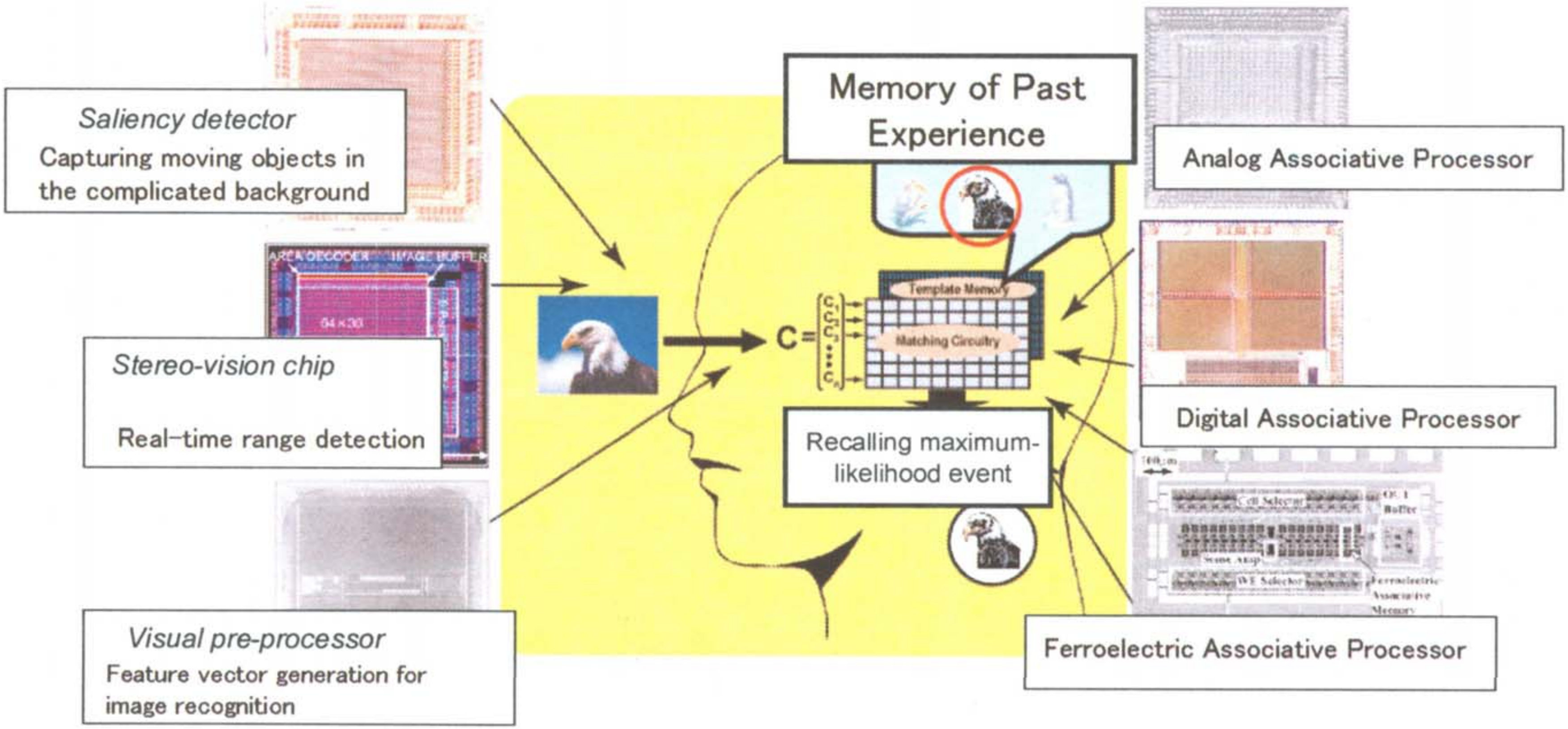
MFTD – multiferroic tunnel diode

Potential Supplemental Applications

- Image recognition
- Speech recognition
- DSP (cross correlation)
- Data Mining
- Optimization
- Physical simulation
- Sensory data processing (biological, physical)
- Image creation
- Cryptographic analysis

Illustrative Example

Top Down Information Processing
Image Recognition



Tadashi Shibata, University of Tokyo

Specialized Devices for Image Recognition

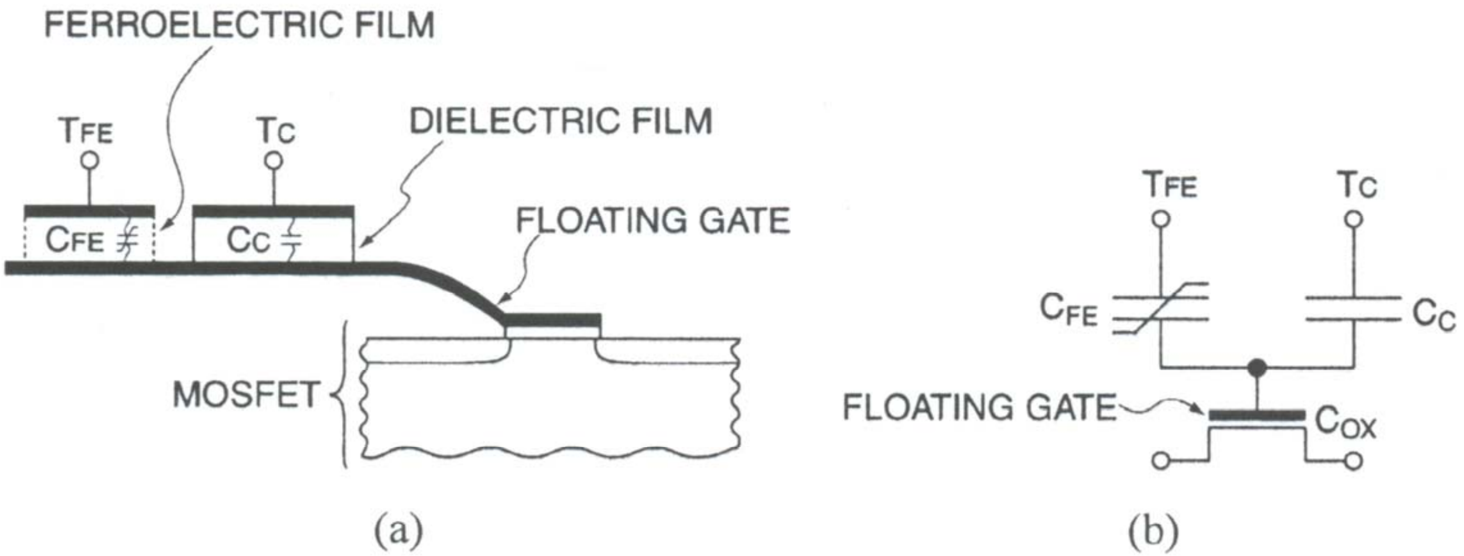


Fig. 1. (a) Conceptual drawing of the basic structure of the heterogate FGMOS. (b) Symbol representing the device.

Heterogate ferroelectric FGMOS FET

Tadashi Shibata, University of Tokyo

Image Recognition

TABLE I

PERFORMANCES COMPARISON OF IMAGE RECOGNITION SYSTEMS

Search target: Sella (a pituitary gland)

Number of templates (generated by learning algorithm): 15

Search Area: 75x100-pel area

	Power(W)	Computational time (Second)	Total energy(J)
Pentium 4 1.5GHz Optimized in an assembly language level	54.7	5	273.5
Mobile Pentium 3 500MHz/1.1V Optimized in an assembly language level	3.5	15	52
Our digital vector generator & neural analog associative processor	0.152	1.2	0.182

Tadashi Shibata, University of Tokyo

Conclusions

- Some new approaches to obtaining dense, high speed, non-volatile memory are showing some promise for success in replacing SRAM.
- Conversely, most new approaches proposed for emerging binary logic devices show only modest potential to eventually replace CMOS.
- However, emerging logic devices may have unique analog properties that provide complementary functions when integrated with CMOS.
- These observations suggest new information processing algorithms, such Associative Memory Processors for certain applications.