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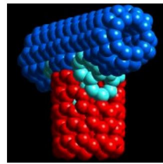
Nanowire based Phase Change Memory



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Collaboration: Prof. David Janes, Purdue University on measurements

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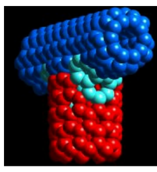
Nanowire as Nano-Chip Component



- **One-Dimensionality**
  - Lowest-dimension transport channel for best device scalability
- **Lithography-less Approach**
  - Vertical transistor does not depend on lithography for defining source-drain separation in CMOS.
- **Unique Physics**
  - Reduced phonon scattering (logic)
  - Surface sensitivity to external excitation (memory)
  - Quantum confinement (logic/memory)
  - Bandgap inversely proportional to the radius
- **Variety of Material Choices**
  - Semiconductor, metal, superconductor, IV, II-VI, III-V, …
- **High Level of Integration**
  - Device / interconnect co-design: ultra-compact chip design (e.g., SRAM, NVM, FPGA)

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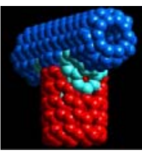
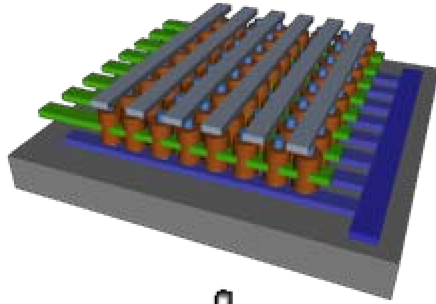
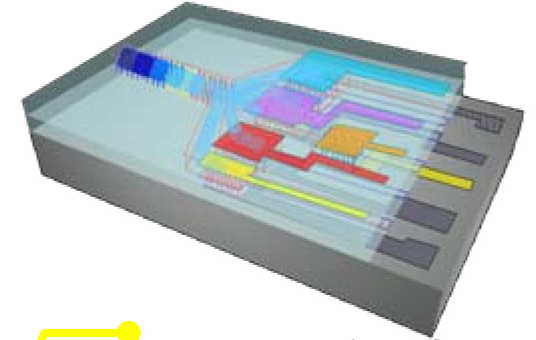
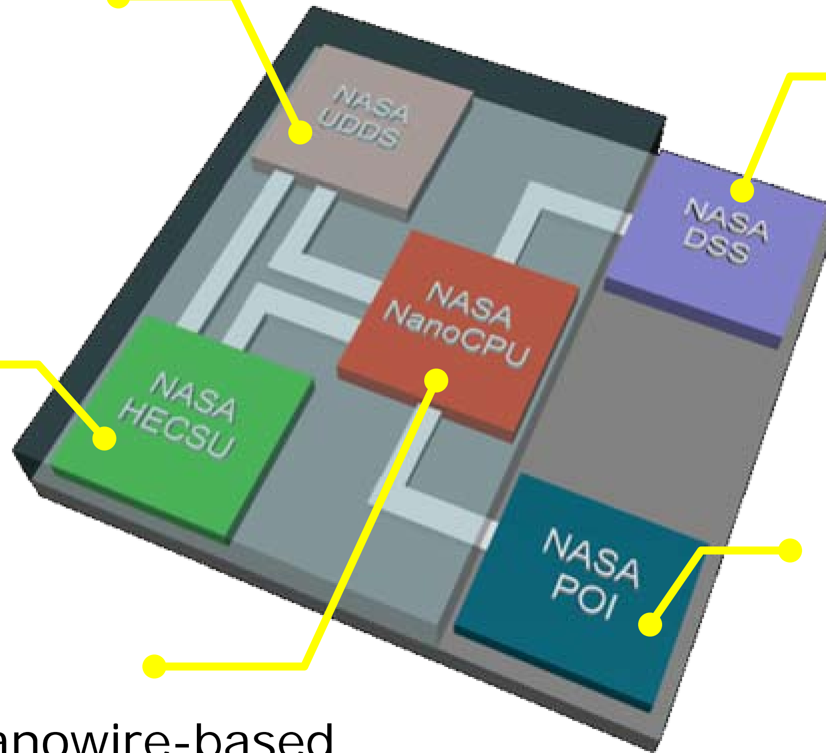
Future Outlook for Inorganic Nanowires





Nanowire-based
Ultra-high Density
Data Storage

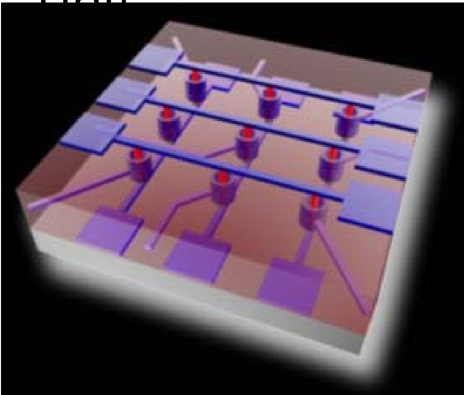




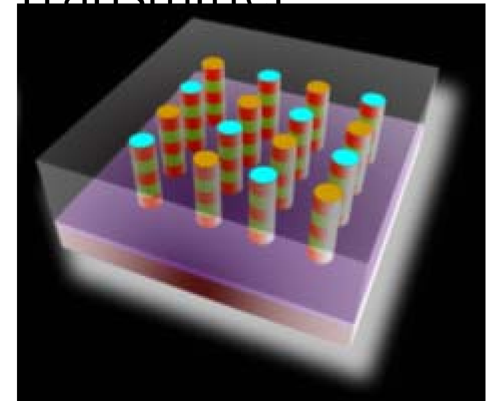
Nanowire-based
Detector Sensory
Systems

Nanowire-based
Hybrid Energy
Conversion/Storage
Unit

Nanowire-based
Peripheral Optical
Interconnect/
Transmitter



Nanowire-based
Radiation-harden
Central Processing Unit



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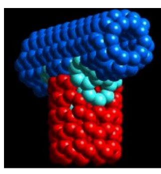
Requirements for an Ideal Memory



- Combine the best of these:
  - High speed of the Static Random Access Memory (SRAM)
  - Nonvolatile nature of flash memory
  - Density of DRAM
- Low Cost
- Scalability

Some Candidates

- Magnetic RAM
- Ferroelectric RAM
- Ovonic Unified Memory (after Ovshinsky who proposed it in 1968) or Phase-change Random Access Memory (PRAM)

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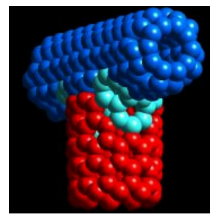
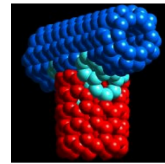
Phase-Change Random Access Memory (PRAM)

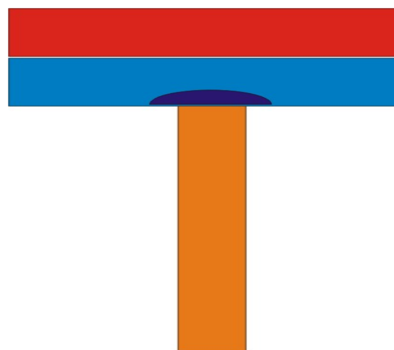


- Phase change materials date back to 1960s
  - Mainstream optical storage media (CDs, DVDs)
  - Electrically operated phase-change Random Access Memory (PRAM) proposed some time ago
- Common phase-change material candidates
  - GeTe, GeSbTe, In_2Se_3, InSe, SbTe, GaSb, InSbTe, GaSeTe, …
- PRAM advantages
  - Binary or multiple reflective/resistive states of the programmable element to represent the logic levels for data storage
  - Thermally induced phase change (orderly single crystalline or polycrystalline C-phase vs. less orderly amorphous α-phase
  - Faster write/read, improved endurance, much simpler fabrication than transistor-based nonvolatile memory
  - Since the data is stored in the form of material phase, soft-error or radiation free operation
- PRAM Issues
  - Enormous programming current to generate the thermal energy for inducing the phase change
  - Joule heating induced power dissipation issues
  - Intercell thermal interference
  - Scaling difficulties

Why 1-D Phase-Change Nanowire?



- Low Thermal Energy and Current for Programming
  - Reduced programmable element volume
  - Reduced melting point compared to bulk value
  - Other favorable thermal transport parameters
- Device Scalability
  - Ultra-low current / voltage / power operation
  - Reduced thermal interference between neighboring memory cells



2-D Thin film PRAM

1-D Nanowire PRAM

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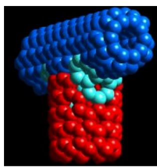
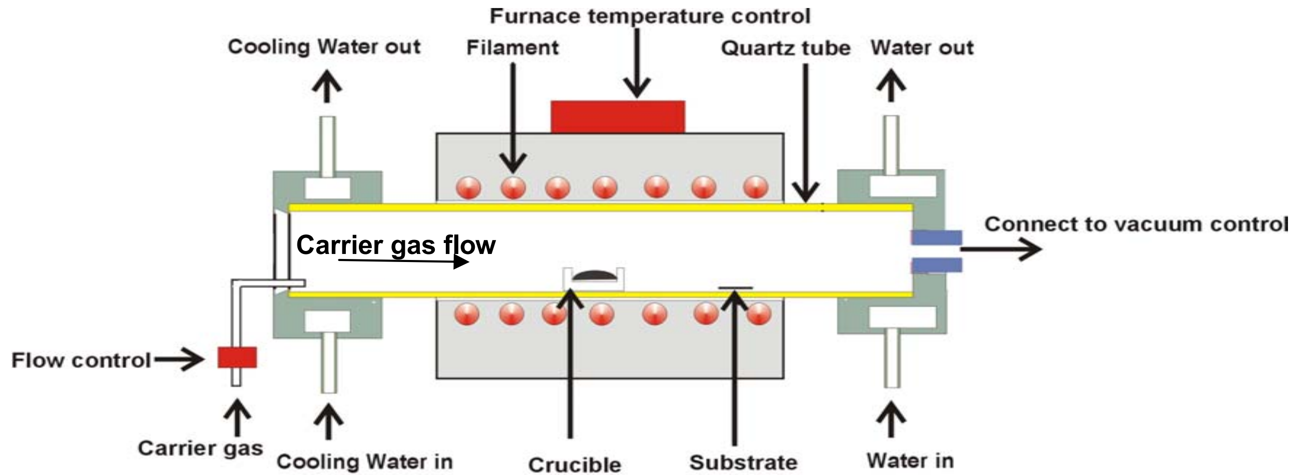
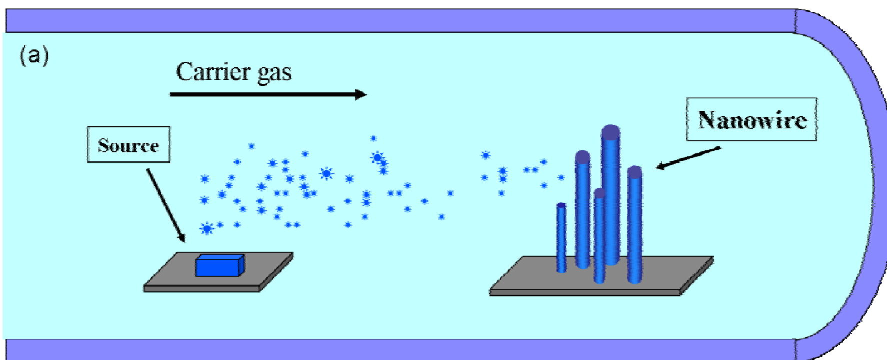
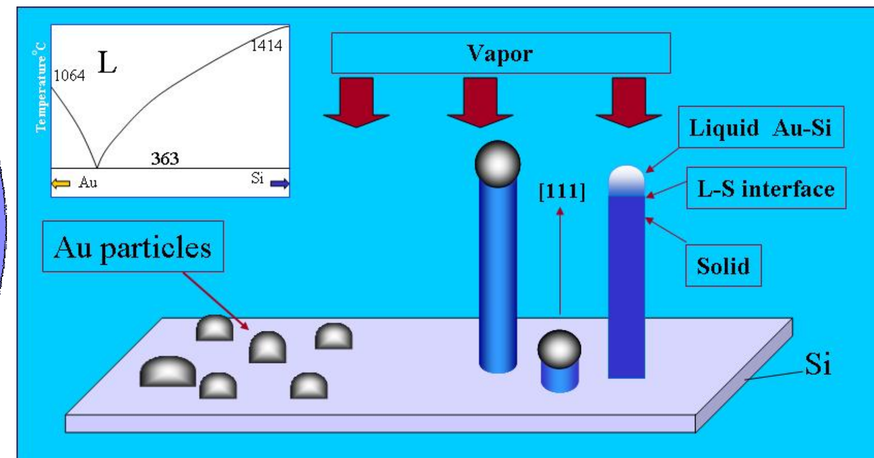
Nanowire Synthesis by VLS Technique





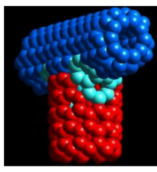
A schematic diagram of the thermal evaporation apparatus





Vapor-Liquid-Solid (VLS) Mechanism

PCM Growth Details



PCM	Source	Source Temp.	Growth Temp.
GT	GeTe powder	720ºC	450ºC
GST	Sb_2Te_3: GeTe= 1:2 powders	690°C	450ºC
In_2Se_3	In_2Se_3 powder	900-950ºC	650-700ºC

- Upstream temperature is dictated by the sublimation temperature of the source powders.
- Growth temperature is dictated by the catalyst choice. Low melting metal such as In would lower growth temperature (in the case of In_2Se_3, In will serve as self-catalyst).

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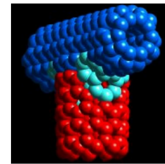
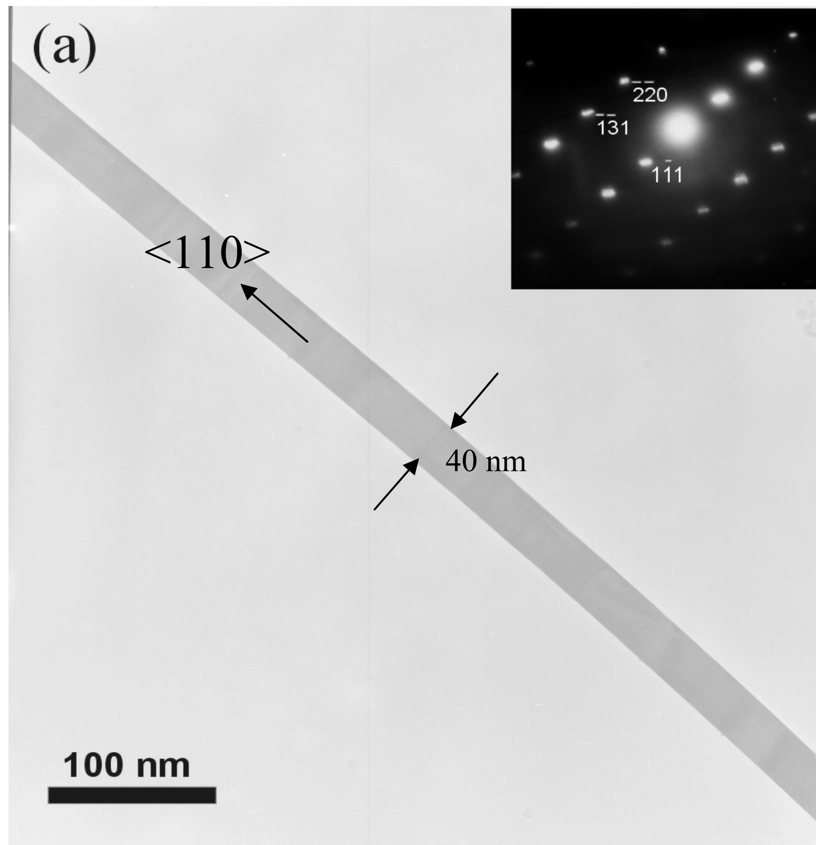
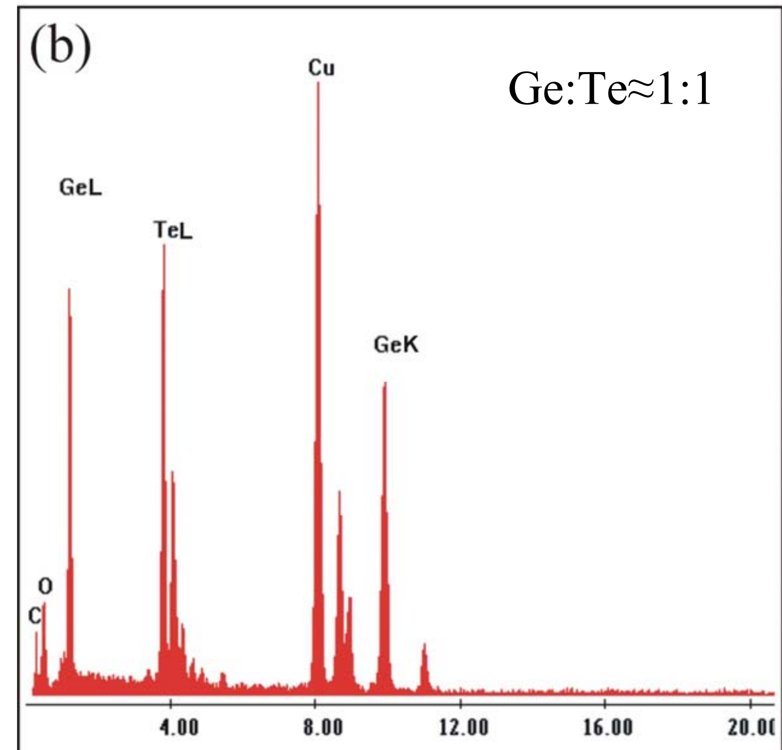
GeTe Nanowires: TEM, SAED, and EDS







(a) TEM image of an individual GeTe nanowire with a diameter of about 40 nm. The inset shows an SAED pattern of fcc cubic lattice structure. (b) EDS spectrum of the same GeTe nanowire.

X. Sun et al., JPCC, 111, 2421 (2007)

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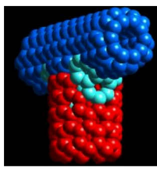
In_2Se_3 Nanowires: TEM and EDS Spectra



In:Se≈2:3

TEM image and corresponding EDS spectra of an individual In_2Se_3 nanowire. Scare bar is 100 nm

X. Sun et al., APL, 89, 233121 (2006)

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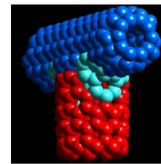
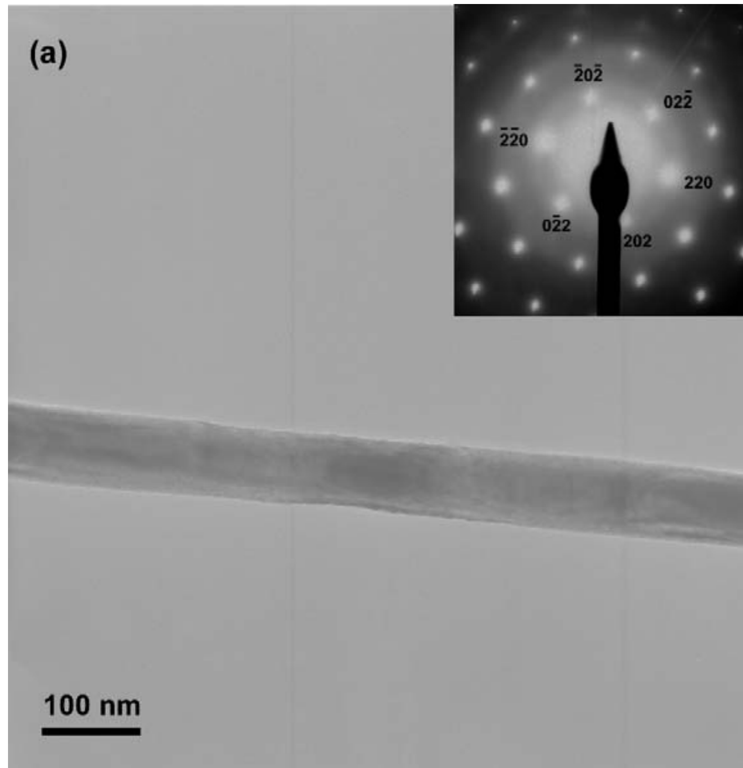
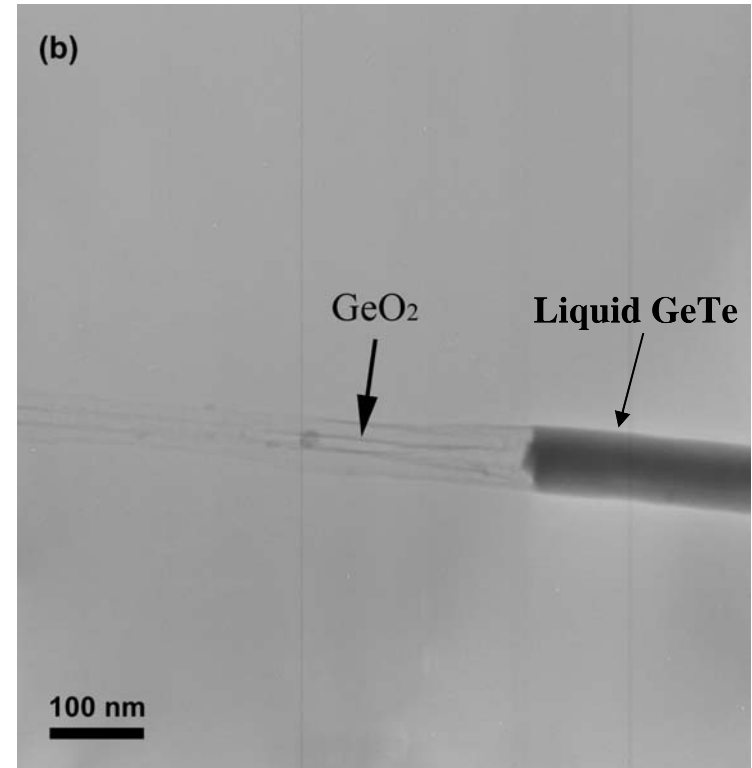


GeTe Nanowires: Melting Experiment and In-Situ Monitoring by TEM





In-situ T_m measurement of GeTe nanowire under TEM image monitoring (a) The GeTe nanowire is under room temperature. (b) The GeTe nanowire is heated up to 400°C when the nanowire is molten and its mass is gradually lost through evaporation. The remaining oxide shell can be seen from the image.

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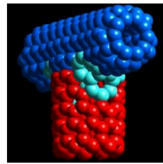
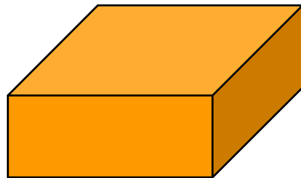
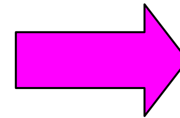
PCM Nanowires: Melting Point

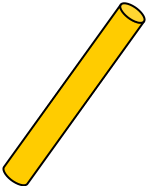




T_m of bulk GeTe: 725°C



46% reduction!



T_m of GeTe nanowires: ~390°C

- The melting temperature of the nanowire is identified as the point at which the electron diffraction pattern disappears and the nanowire starts to be evaporated.
- Similar reduction for In_2Se_3 from 890°C to 680°C
- This property is diameter dependent: reduction even more significant for smaller diameters

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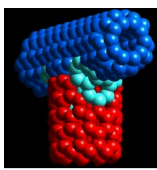
Nano-encoded GST Nanowires



After 5-sec e-beam localized thermal writing from crystal to amorphous

E-beam encoding

100 nm

α-GST nanodot

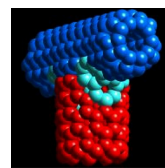
c-GST nanowire

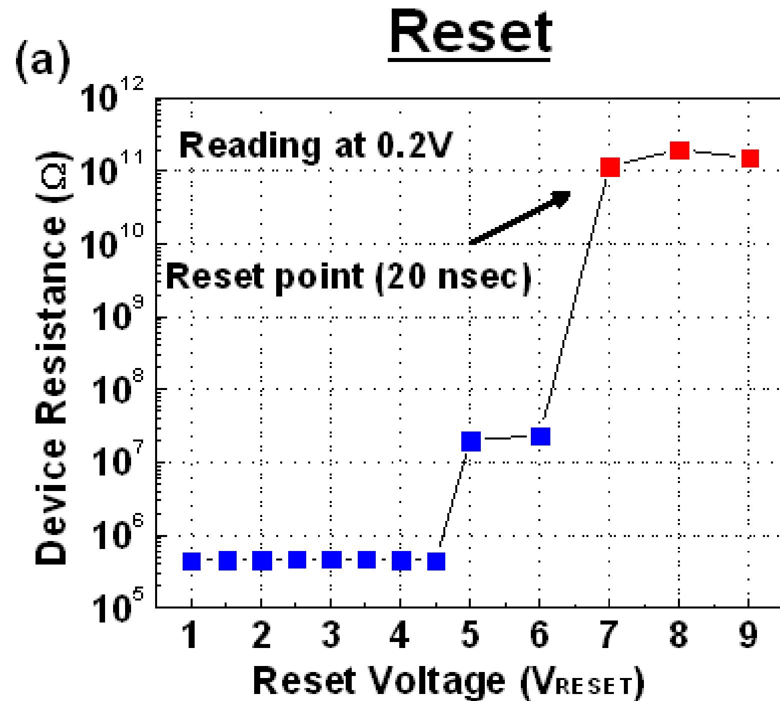
2nm

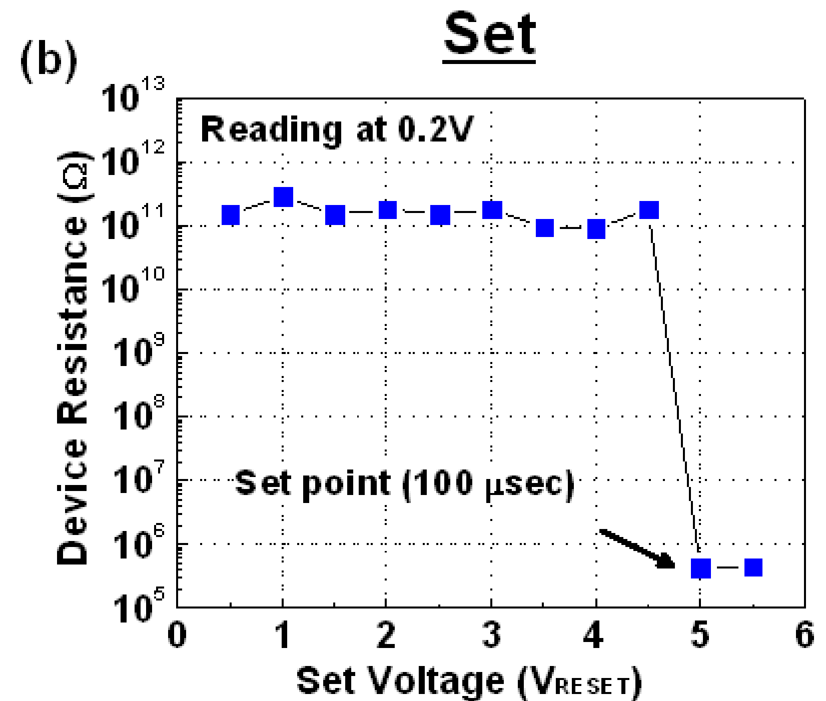
Thermally induced nano-encoding on an individual 1-D GST nanowire with scanning focused electron beam. A series of α-GST nanodots were created by highly localized thermal heating with an e-beam spot of ~25 nm in diameter. The amorphous-to-crystalline boundary is marked by red dash line.

X. Sun et al., APL, 90, 183116 (2007)

In_2Se_3 Nanowire Memory Switching Behavior







Pulse width: (a) Reset at 20 nsec. (b) Set at 100 μsec.

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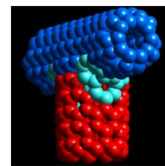
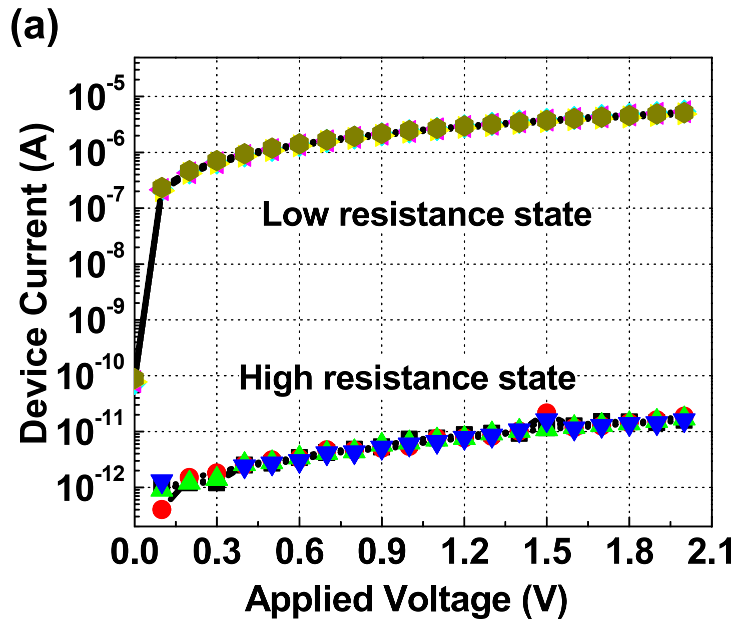
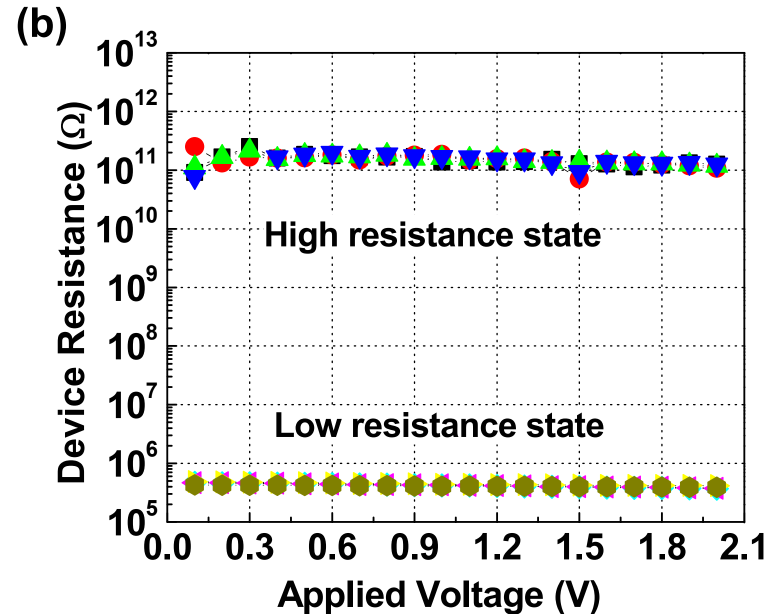
In_2Se_3 Nanowire Memory



I-V



R-V



- Device characteristics in either state with successive measurement sweeps show stable resistive behavior
- Dynamic switching ratio (on/off resistance) is ~10^5

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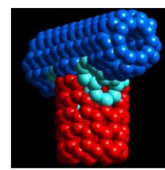
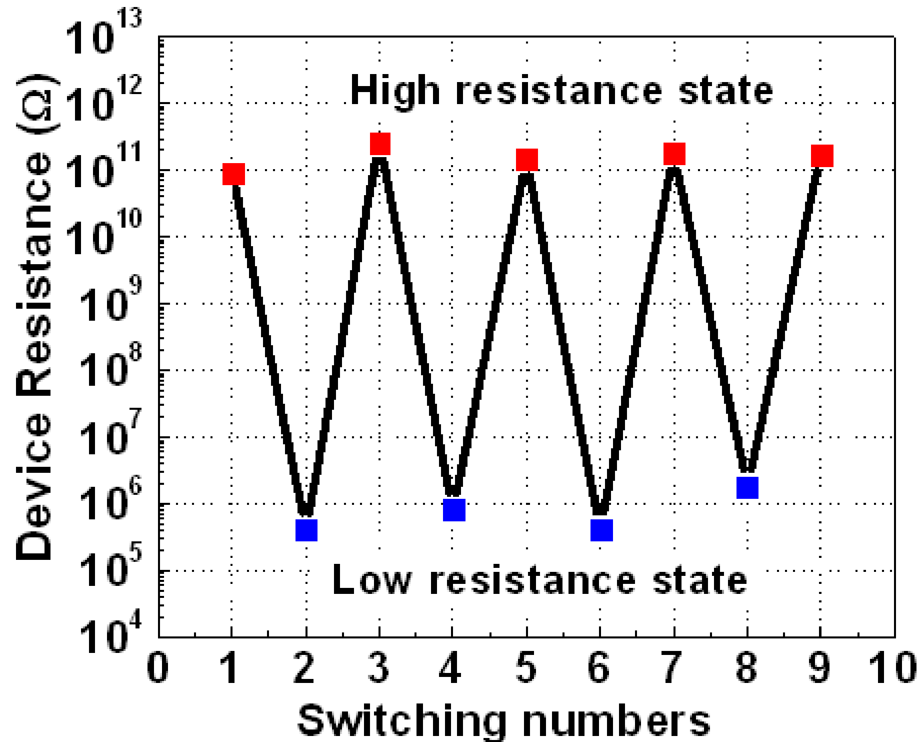
In_2Se_3 Nanowire Memory Repeated Reset-set Cycles





Repeated resistance measurement of In_2Se_3 phase-change nanowire memory device. Device was switched between high- and low-resistive states using voltage pulses: LRS - HRS using 7V / 20 ns reset pulse; HRS - LRS using 5V / 100 μS set pulse.

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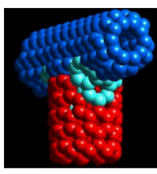
Indium Selenide Nanowire PRAM Performance



- Reset operation: Power (V^2/R) = 80 μW at 7 V

  Input energy = 1.6 pJ for 20 ns pulse
- Set operation: Power (V^2/R) = 0.25 nW at 5 V

  Input energy = 25 fJ for 100 μS pulse

	In_2Se_3 NW	In_2Se_3 Thin Film	GT or GST NW*
Switching ratio	10^5	10^3	10^3 / 10^2
Reset power/Energy	80 μW / 1.6 pJ	16 mW / 1.12 nJ	~ mW
Set power/Energy	0.25 nW / 25 fJ	14 μW / 140 pJ	

* From JACS 128, 14026 (2006)

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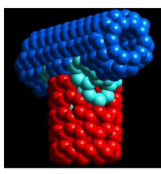
Summary



- The ability to grow Phase-change materials as 1-d nanowires has renewed the interest in PRAMs: lower programming current, power, energy…and scalability

- We have grown and characterized GT, GST and In_2Se_3 nanowires; observed in each case a reduction in melting point compared to the corresponding bulk value

- Fabricated In_2Se_3 and GT nanowire PRAM devices and showed the power and energy levels for reversible switching are far lower than previous reports on thin film devices