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2020 Computing: Virtual Immersion Architectures (VIA-2020)

SRC/NSF/ITRS Forum on Emerging nano-CMOS Architectures

Meeting Date: July 10-11, 2008

Meeting Place: Seymour Marine Discovery Center of UC Santa Cruz, CA

Material Technologies for Immaterial World?

Inspiration: "Immaterialism" philosophy
by Bishop Berkeley (1685-1753)

"Esse est percipi" ("To be is to be perceived"):
Individuals can only directly know sensations

It is indeed an opinion strangely prevailing amongst men, that houses, mountains, rivers, and in a word all sensible objects have an existence natural or real, distinct from their being perceived by the understanding…
…what do we perceive besides our own ideas or sensations; and is it not plainly repugnant that any one of these or any combination of them should exist unperceived?

Perceptual Processing:

Can computer architectures extend human reach into Bishop's Berkeley immaterial world?

Overarching Question

- Given 2020 technologies, how closely can avatar-to-avatar transactions in virtual space approximate the quality of people-to-people transactions in physical space?

Supporting Questions

- How will communication latency impact the quality of virtual transactions?
- To what degree will an end-user machine need to develop and execute predictive models of the other participants?
- Can we expect to implement real-time language translation to support international transactions
- IS the avatar's view of the scene sufficient or other visual cues important?

Supporting Questions

- Are multi-core computers well-matched to computation needs of virtual immersion?
  - Role of centralized versus distributed computing in support of VI?
- What kind of sensor system is needed for each participant to adequately portray him/her to other participants in the virtual meeting?
- What advances in VI software systems are needed to enable the creation of virtual environments and to support peer-to-peer transactions?

Forum Theme

- How will semiconductor nanoscale technology drive a migration to different information-processing and computing approaches?
  - Energy/Power minimization is a universal macro-constraint for on-chip architectures
- What technical capabilities do we need in 2020 to do this IT computing?

A Thought Problem: VIA processor

- The hypothesis is that such chip processor could be a general platform
  - Very high processing power
  - Modeling complex physical systems
  - Image processing (e.g. face recognition, motion capture etc)
  - Real-time decision making
- An ultimate realization of virtual reality would be ‘fully immersive environment’
  - A spatial construct by computer that appears to surround the user
  - The user can act and explore as if it were real
  - Multi-sensations (visual, audio, tactile, smell...)
  - Multi-user interactive network
  - All in ‘real-time’

Panel I:
Computational Platforms for VIA-2020

- What information processing performance is needed to support VIA-2020?
- What are the classes of processors needed for VIA and how many of each class is likely to be required on-chip?
- Can we assess the potential of the three recently emerged multicore platforms as general-purpose computing engine
  - SMP – Symmetric Multiprocessors
  - CBE - Cell Broadband Engine
  - GPU – Graphics Processing Units
- In VIA applications requiring real-time physical simulations, how will be computational load be partitioned between the server and end-user processors?

Panel II:
System Latency Minimization

- Specifications for latency needed at all levels of VIA
- Power-latency-reliability tradeoffs
- A realistic potential for 3D
- A ‘mobile’ supercomputers feasible?

Panel III:
Morphic Computational Architectures for VIA

- What subsystems for VIA 2020 lend themselves to morphic implementations?
- Are there new devices that offer implementation advantages?
- Energy gains due to morphic structures?
- Analog-Digital tradeoffs?

Panel IV:
Turing-Heisenberg Rapprochement

- Connecting Physics to Computer Science
  - Can we obtain guidance from theoretical considerations on architectures for VIA-2020?
- How will semiconductor nanoscale technology impact different information-processing and computing approaches?
  - Can emerging memory and logic technologies impact VIA-2020?
  - How will physical constraints (size,energy…) effect on-chip architectures?
- Lessons from biological computing?

Panel V:
Software environments to support VIA

- What are the new datatypes that will be required?
- Software/hardware trade-offs?
- OS on demand?

Forum Objectives

- Evaluate the system requirements
  - Selected driver application(s)
  - HW/SW considerations
- Examine the limits and trade-offs of integrated technologies (e.g. logic, memory, on/off-chip communication etc.)
- Identify device technologies that have a realistic chance of meeting the system requirements
- Define research directions/opportunities
- Foster interaction between panel specialists and forum attendees