2020 Virtual Immersion Architectures Forum

July 10th, 2008

QorIQ™
Communications Platforms

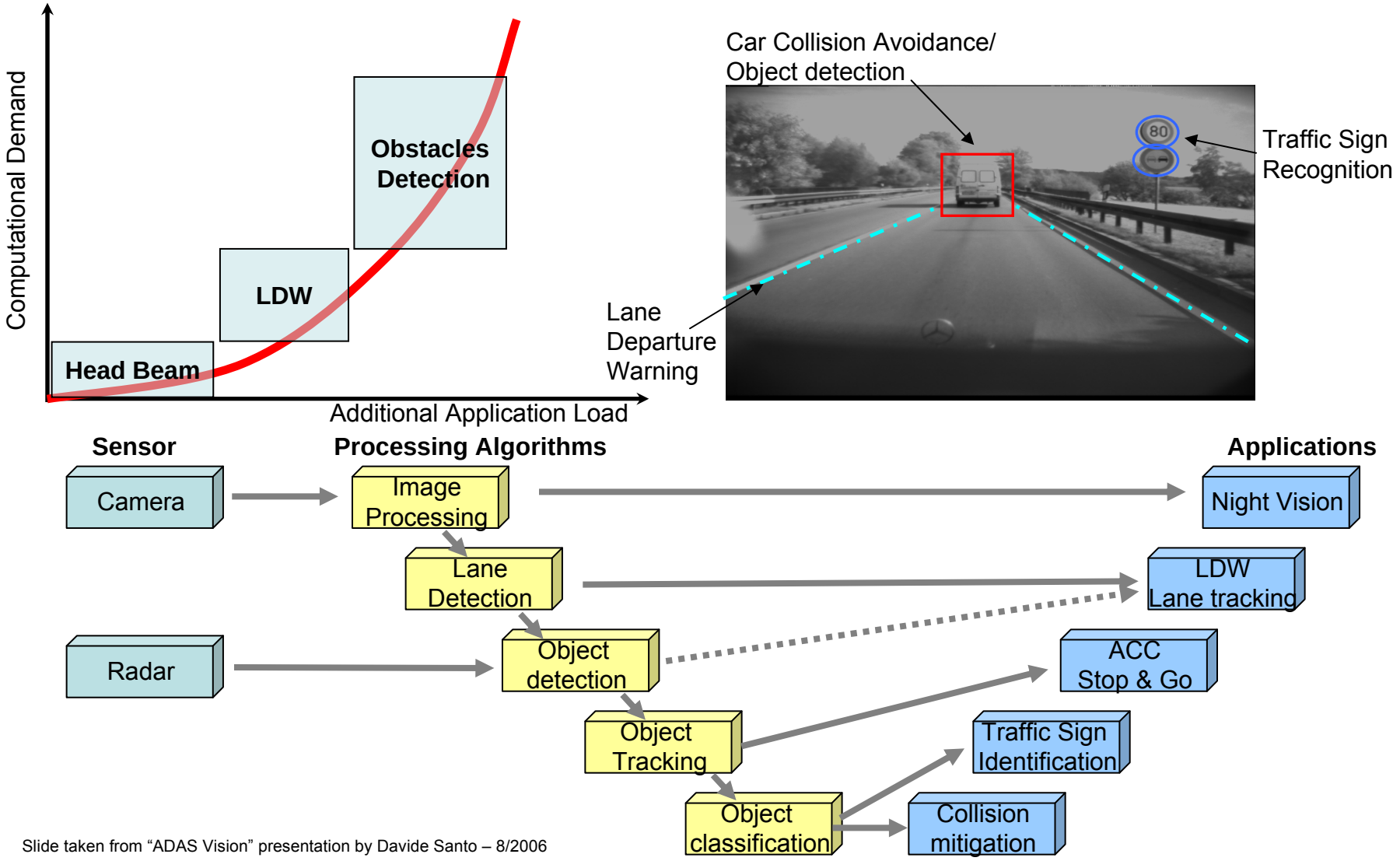
Multicore Communications Platform

Dr. Dac C. Pham
Fellow & Director, Power Architecture and DSP Cores & Platforms,
Freescale Semiconductor

Outline

- The Computational Demand from “Real World” Requirements
- Performance Scaling through Multicore SoC
- Multi-core Platform Design Challenges
  - Performance
  - Bandwidth
  - Efficiency
  - Integration

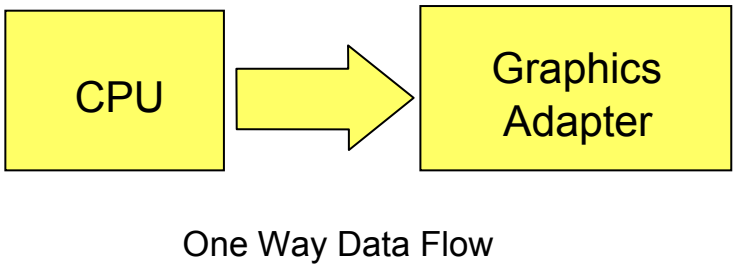
The Computational Demand for a "Safer World"



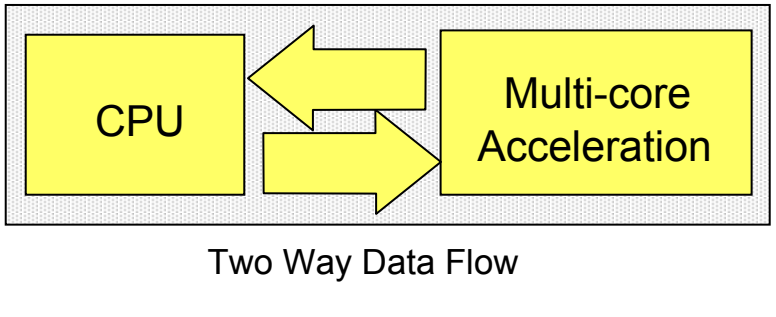
Slide taken from "ADAS Vision" presentation by Davide Santo – 8/2006

The Computational Demand for an “Interactive World”

Yesterday "One Way" Graphics Rendering



Today "Two Way" Physics-Based Modeling

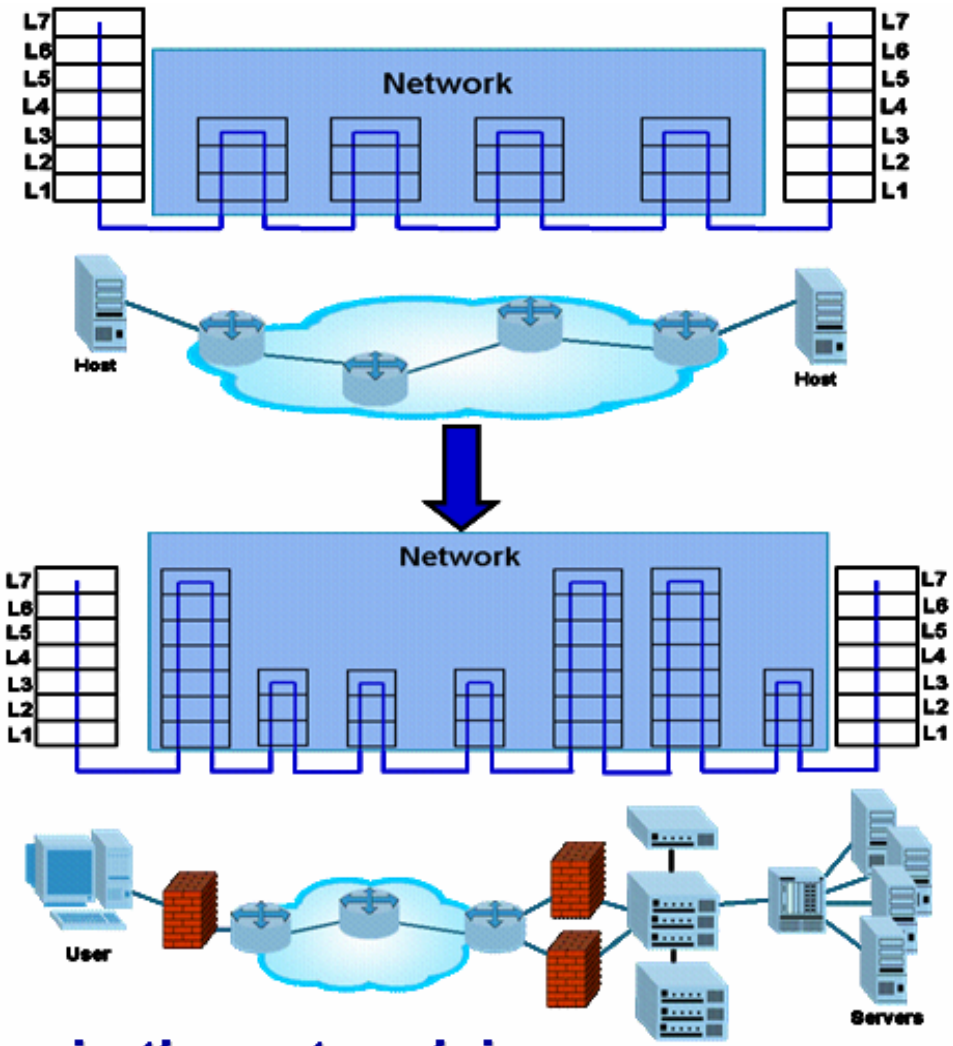


→ Interaction of Physics, AI, Graphics Rendering
….”Indistinguishable from Reality”

Slide taken from “The Cell Processor” presentation by Dac Pham, DATE 2006 Tutorial Session E – 3/2006

The Computational Demand for a “Trusted World”

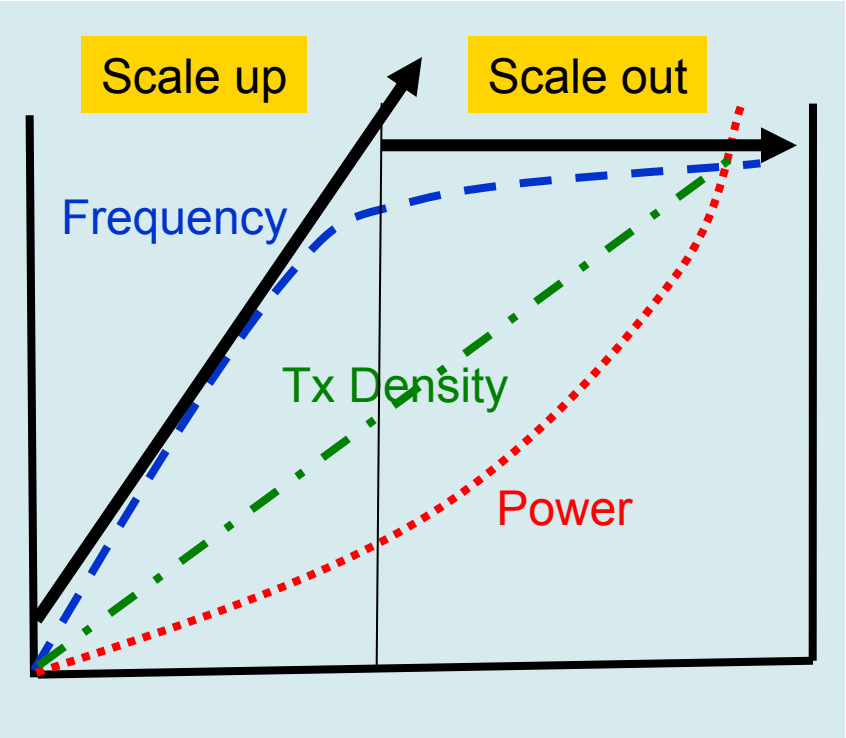
- Traditionally, networking equipment has operated at layer 3 and below in the protocol stack
- The need for improved security, quality of service and traffic control has driven equipment at the networks edge to operate at layer 4 and above:
  - Application-aware network security
  - Application Aware QoS
  - Application Acceleration
  - Content filtering
  - Content billing
  - Protocol compliance checking
  - Server load balancing



Layer 4-7 (Application) processing in the network is now common

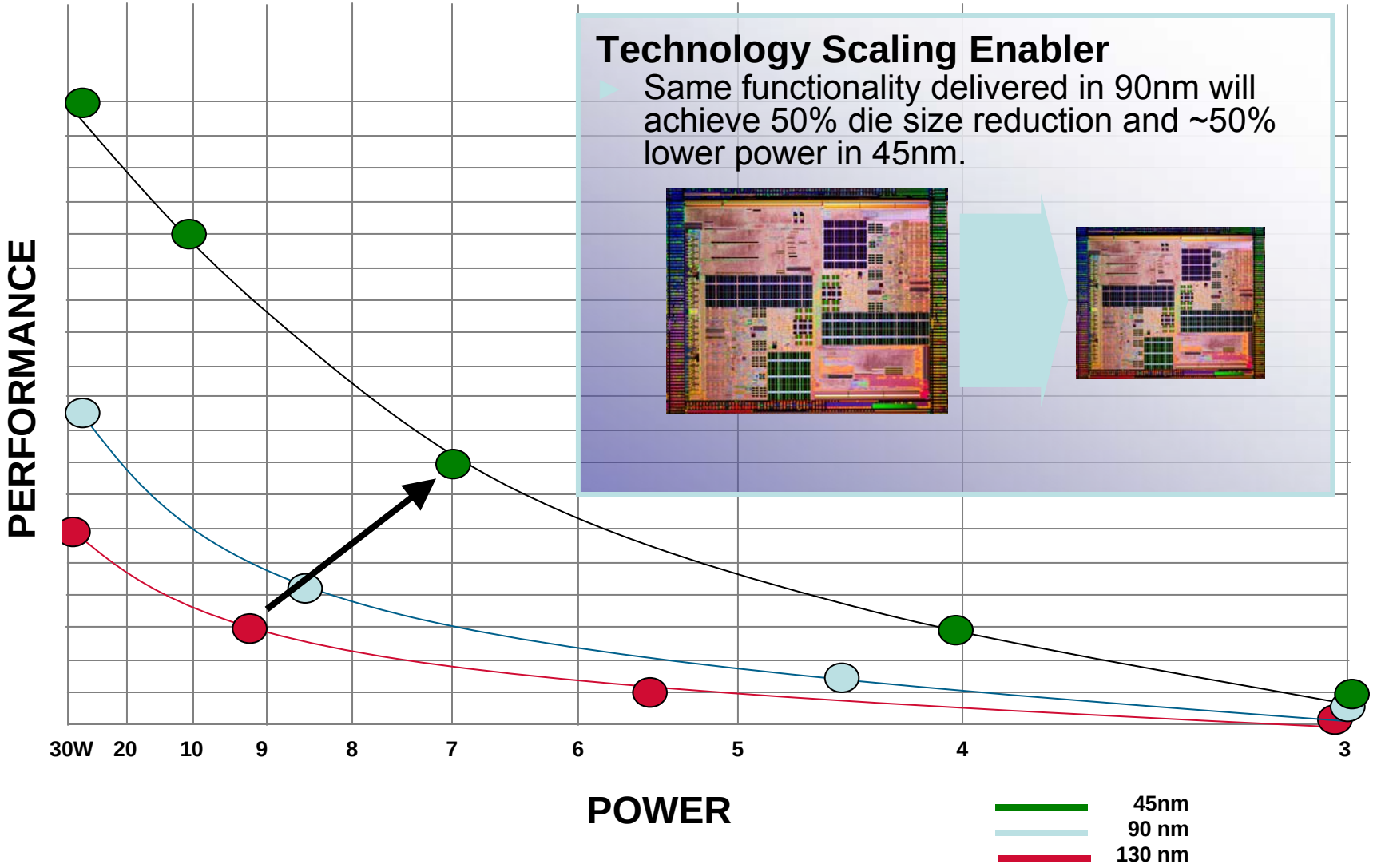
How Multicore Help?

- The Challenge: Double Performance Every 18 Months
  - Superscalar: More Functional Units → Higher Power
  - Super pipelined: Deeper Pipeline → Higher Power
- The Constraint: Power Envelope
  - Power envelope (AC: ~V^3, DC: 20-50%) limits frequency (~V)

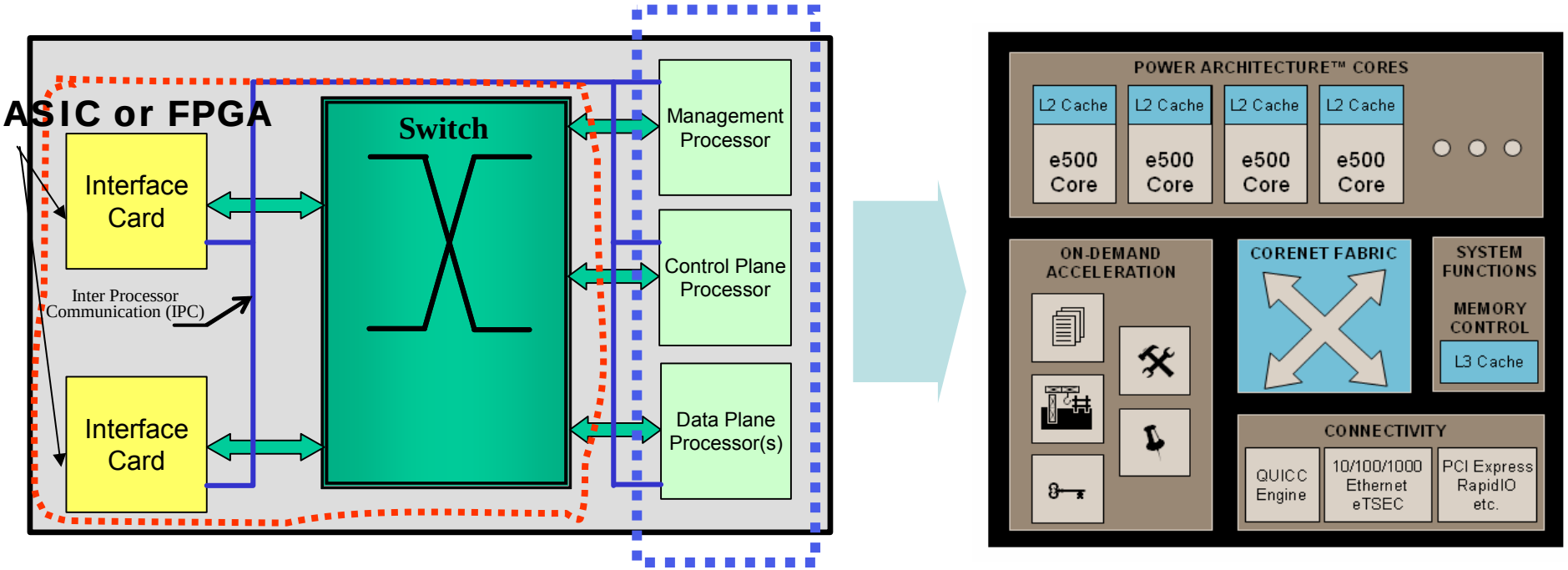


Multi-core SoC created opportunity to increase performance while keeping power in check

Performance Through Technology Scaling



Performance Through System Integration

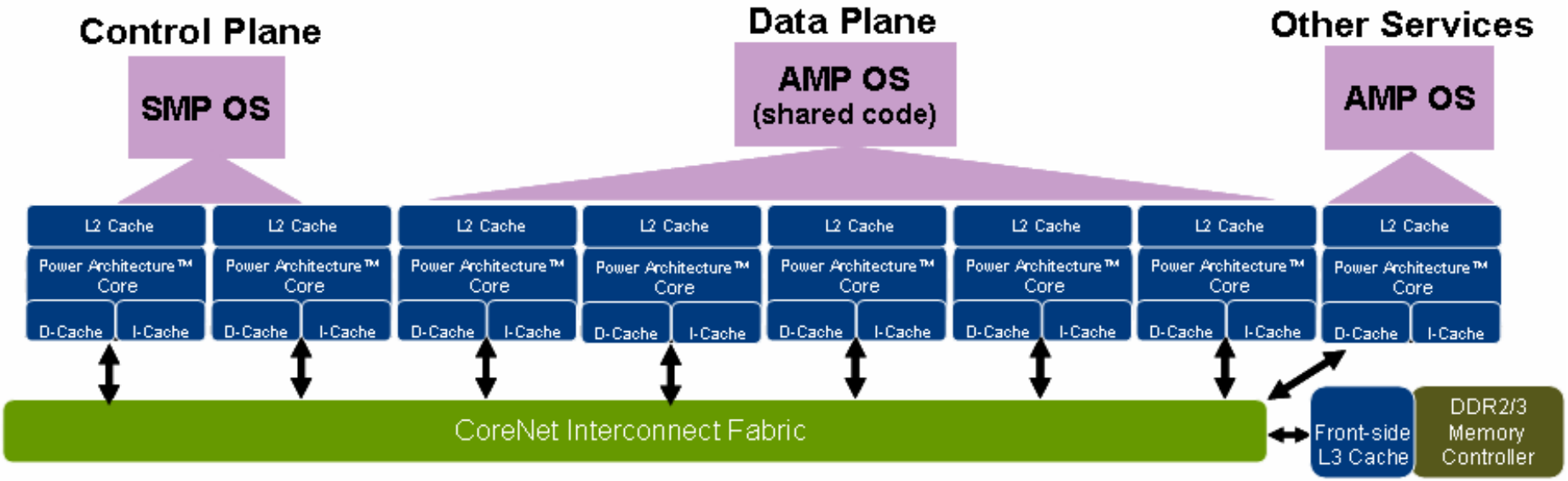


Network Integration: Packet processing, content filtering, and security integration in a chip dramatically shorten the packet data path, eliminate redundant packet processing, simplify board/system design, and reduce cost.

Performance Through SW Virtualization

Run any heterogeneous combination of SMP/AMP Operating Systems (OSes) on cores

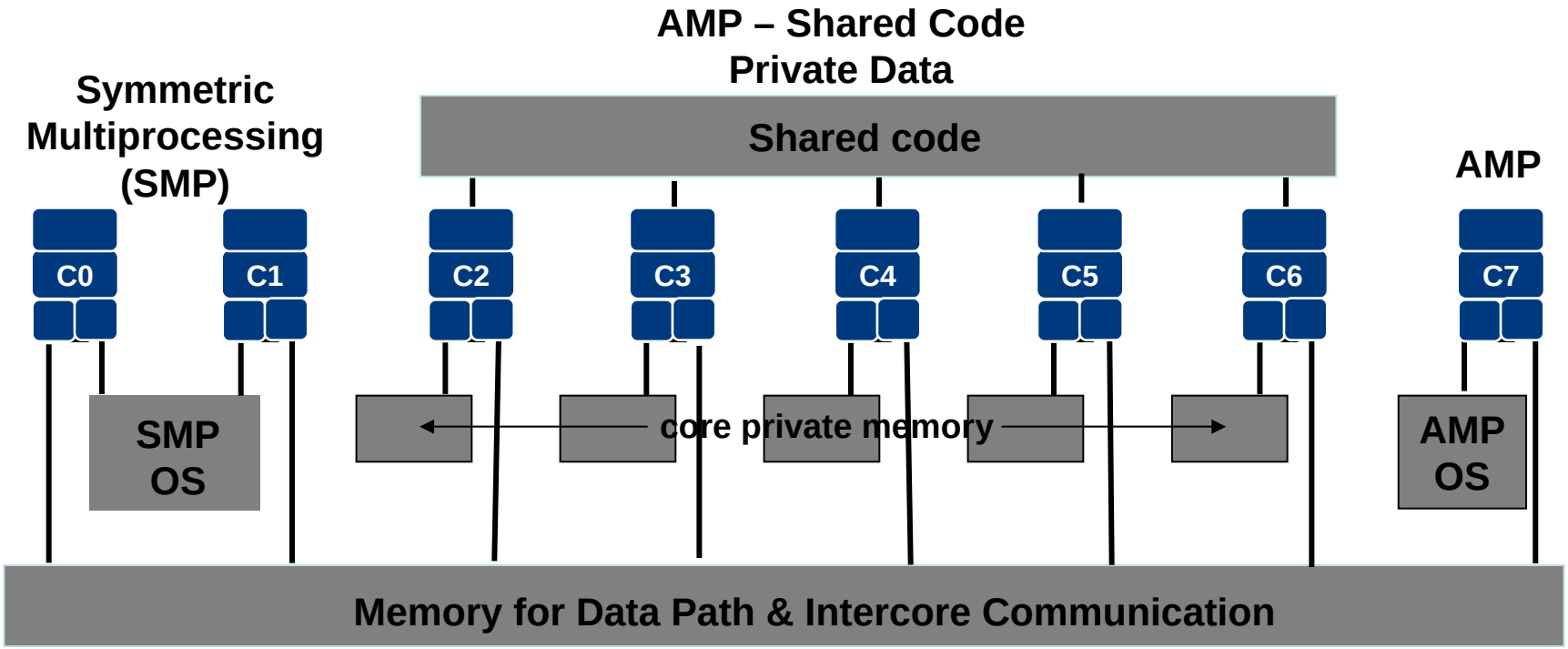
- **Efficiently**
- **Securely (including secure boot support)**
- **Without *large* changes to customer's OS or application software**
- **Supported by 3rd Party OSes and tools**



Multi-core Design Challenges

- **Performance**
  - Core Matters!
  - Balance – uni-core / single thread to multi-core performance
  - Leverage technology to control power and cost
- **Bandwidth**
  - Interconnect Matters!
  - Shared resources: Buses, cache/memory controllers, high-speed serial links, etc.
  - Throughput vs. Latency
- **Software**
  - Efficiency Matters!
  - Virtualization
  - Shared memory and coherency programming

Memory Sharing/Access Control Example



Gray boxes are regions of memory dedicated to or shared by partitions/cores

Same pattern of connectivity used for cache coherency domains

Multicore Challenges and Potential Solutions

- **Technology**
  - Minimize cross chip variations in delay, leakage, hot spot → sensors usage, asynchronous interface, multi-clock domain
  - Array bit cell stability, writability, yield → separate array supply, array repairs, ECC
  - Growing impact of wire RC vs. device speed → Shared Bus vs. Switch Fabric vs. Tiled/Mesh network
  - Power, Clock, Signal Distribution variation due to hot spots, inductance effects, etc. → thermal and 3D analysis, multi-clock domains

- **DF***
  - SER, NBTI → ECC, margins
  - Yield → test strategy for partial good
    - Isolation of bad circuits from one core to other cores
    - Each core individually testable

Multicore Challenges and Potential Solutions

- **Power**
  - Performance on-demand →DVFS, switch fabric (point-to-point), hierarchical memories
  - Shut-down leakage when not needed → multi-voltage domains, sleep device
  - Lower operating voltage → VID, separate array supply

- **Design Methodology**
  - Execution and Quality → Platform verification strategy for first time right and faster time to market
  - Competitive products → Concurrent analysis and optimization: Process/Power/Timing/Thermal
  - Short Channel Effects → Variation-aware tools and methodology

Trends Driving Architecture Innovation

Going **Green**

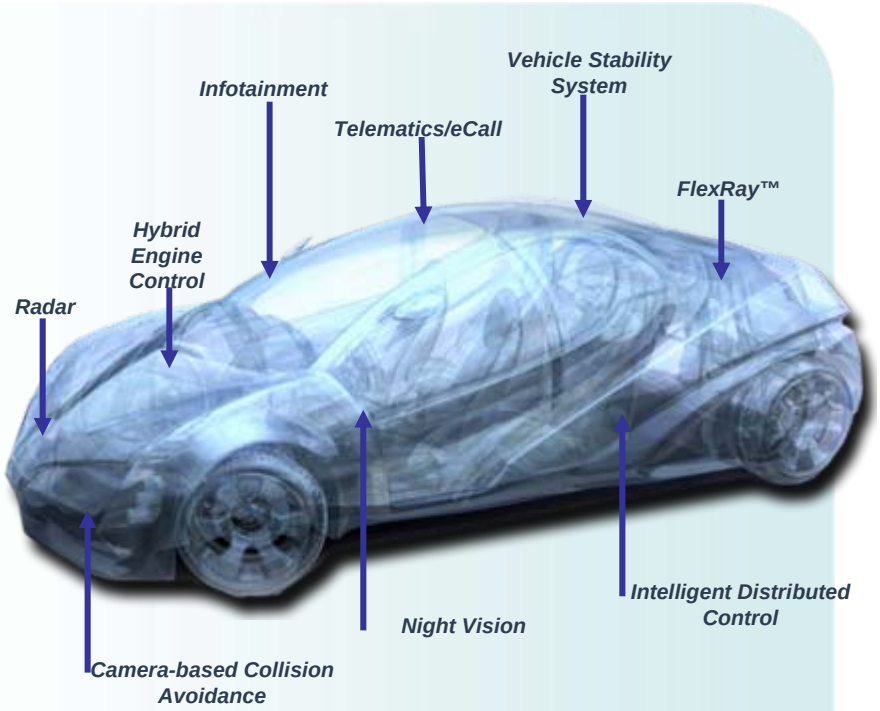
- A critical challenge facing the engineering community today is increasing the energy efficiency of the electronics products we create.

Net **Effect**

- Both consumer and business demand for rich content is rapidly surpassing the networks' ability to deliver it.

The Green Automobile

- Where Architecture Helps:
  - Stringent emission regulation
  - Introducing hybrids, gasoline direct injection
  - Replacing hydraulics with electronic control for weight reduction



For Example: Freescale technology has contributed to significant improvements in automotive fuel efficiency — *helping to reduce fuel consumption by 33%* (between 1978-2004) while greatly reducing harmful emissions.

Freescale continues to expand its array of high-performance powertrain management products. In 2008, GM introduced the world's first full-size hybrid SUVs – *Freescale MCUs are used throughout the drive train of these, fuel-efficient vehicles.*

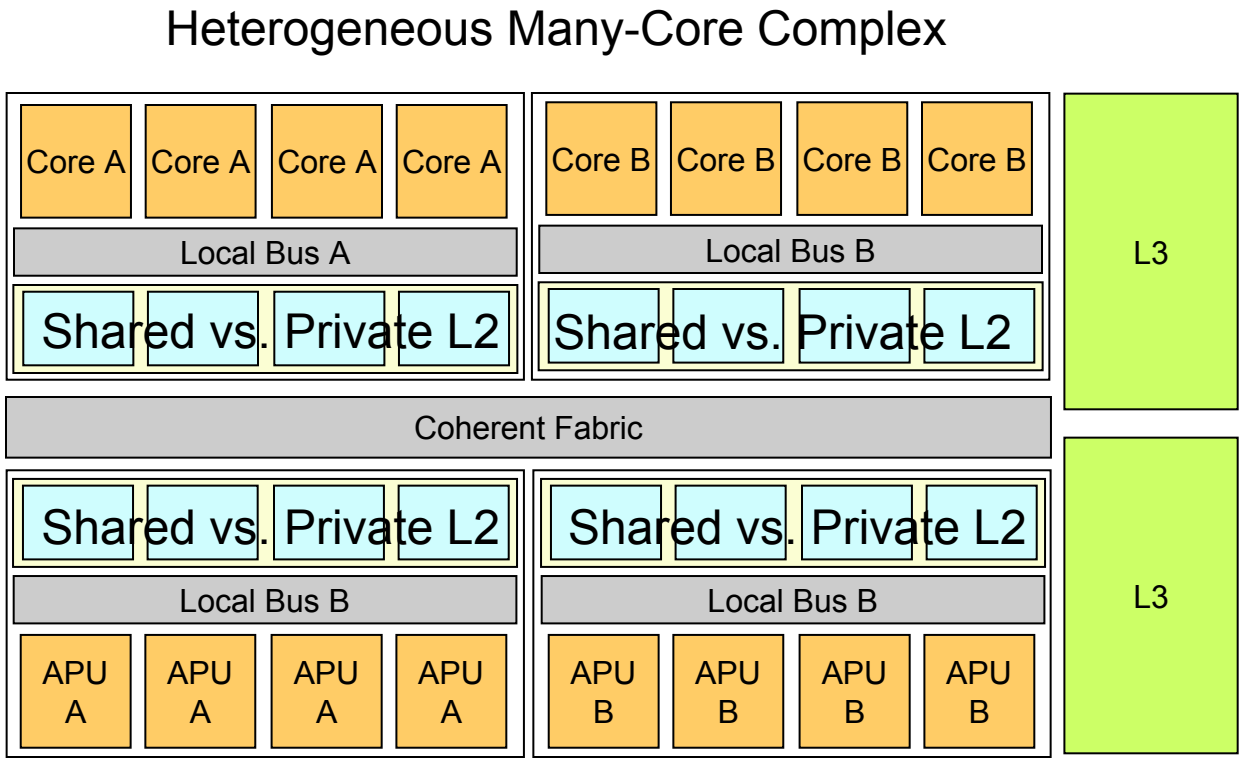
Going Green

The Network Platform

- **Larger/Faster Mem Closer to Cores**
- **Hierarchical MSS**
- **Latency vs. Throughput**

-**Shared Bus vs. Fabric vs. Ring Vs. Mesh**

- **SIMD**
- **DSP**
- **Video**



- **eDRAM?**

Net Effect

Conclusions

- The continuing demand for a “better world” will drive computational performance growth
- Multicore innovations are the force behind this performance improvement
- The potential is great but we must solve key challenges in system, hardware, and software

Acknowledgments

The deep collaboration and the many contributions from the entire Freescale NMG team who worked tirelessly on the design of this Multicore Communications Platform