Future PC Trends

& their Implications on

Traditional Computing Architectures

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Evolving Traditional Computing Values

1960s-1980s

GP PERFORMANCE

1990s

PRICE • GP & MEDIA PERFORMANCE (Mhz, OOO, ISA)

2000s

PRICE • GP & MEDIA PERFORMANCE • WATT (IPC% >= WATT%)

2005

PRICE • GP & MEDIA PERFORMANCE • WATT • FF • USAGE MODEL Single Core → Threading → Multi Core

2010+?

PRICE • FF/STYLE • USAGE MODEL • CONNECTED • PERF • WATT Multiple Devices – Many Mobile

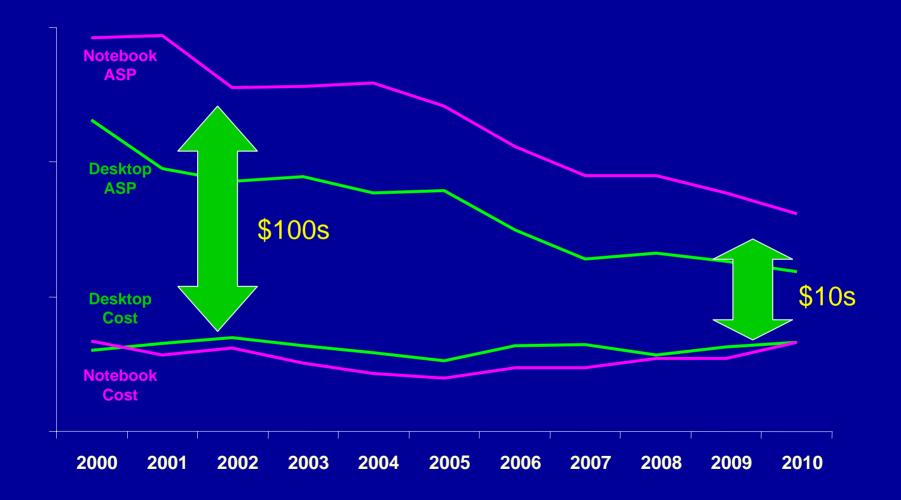


Major Trends and their Implications

Implication Trend Price Declining Cost, Cost, Cost Best mobile Experience **Mobility & Devices is it!!** Longer Battery Life, New usage models Ubiquitous multi-connectivity **Best Performance @ FF SW/Data Spiral extending:** Rich content (Media, Gfx), General Purpose, Special **User generated** Accelerators, Ul Flexibility, Integration, **Growing Segmentation** Customization

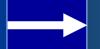


Core Logic ASP vs Cost Trends





Price Declining



Cost, Cost, Cost

- Driving Moore's law is good
 - Moore's Law DOES NOT break over the next ~10 years
 - 450mm is coming
- Multi chip Single chip More integration
- One (big) size chip doesn't make sense
- Cheaper PAT (Package, Assembly, Test)
- Digital I/O that scales with Si process

Driving to advanced process and aggressively addressing other cost factors





Best Mobile Experience
Longer Battery Life,
Ubiquitous multi- connectivity

- Always connected Broadband = Multi-Comm
- Always-On
- Integration also to achieve small form factor
- Outstanding power management & Cooling sharing as Integration increases

All PC Client Devices will become Always on Always connected Compute + Comm capable



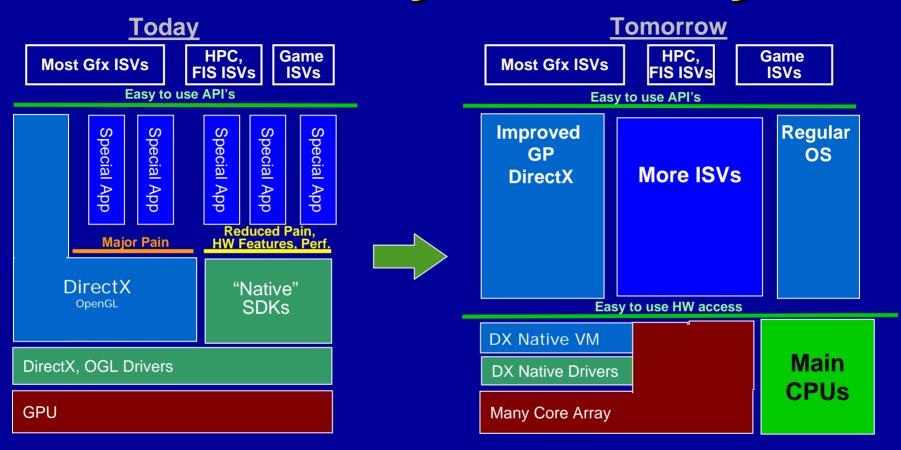
SW/Data Spiral extending:
Rich content (Media, Gfx),
User generated

Best Performance @ FF
General Purpose, Special
Accelerators, UI

- "One internet" -> One arch Top to Bottom
- Single Core to Multi Core Offerings
- More capability specific ISA/Arch extensions
 - SIMD/Vector, Manageability, Security, Content enhancement
- GP IA Many Core Media/Vector Acceleration
 - Discrete and Integrated
 - Supported by new Memory Hierarchies (e-DRAM, PCM, Flash)
- Heterogeneous Computing Model
 - Single programming model and SW compatibility across
 - Apply the right kind of efficient performance where needed



CPUs + Many Core Arrays



Today:

- Few ISVs doing cart-wheels for a 3-4X FP gain
- Tomorrow: ISVs shift to CPUs + Many Core Arrays

IA Top to Bottom + IA many core Media/Vector accelerator under one native programming model

Growing Segmentation



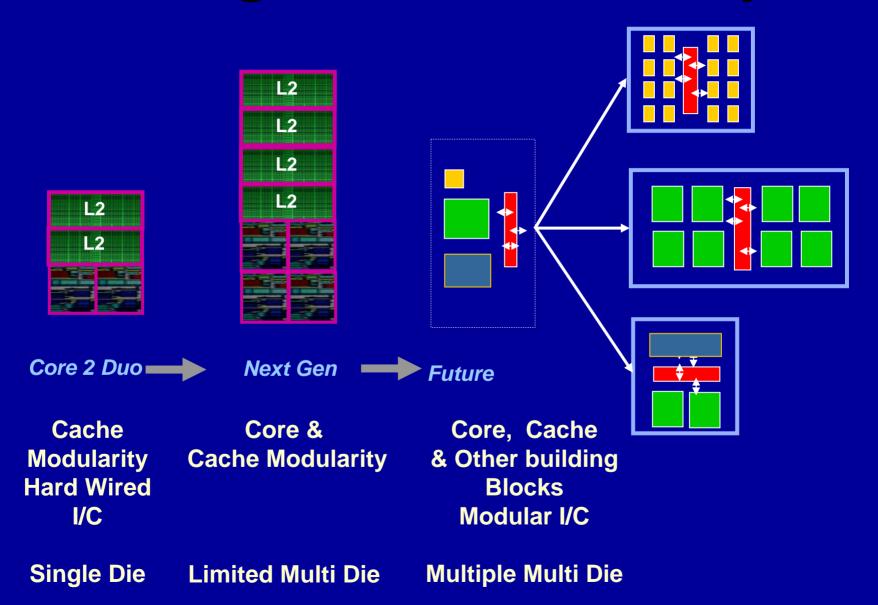
Flexibility, Integration,
Customization

- Highly Modular Design
- Architectures for IP based integration
 - Compute, I/O, memory, communications, sensors, UI, cameras
 - "Standard" internal Interconnects
- SOC Customization

Modular and Customizable "SOC"s coming to traditional computing architectures

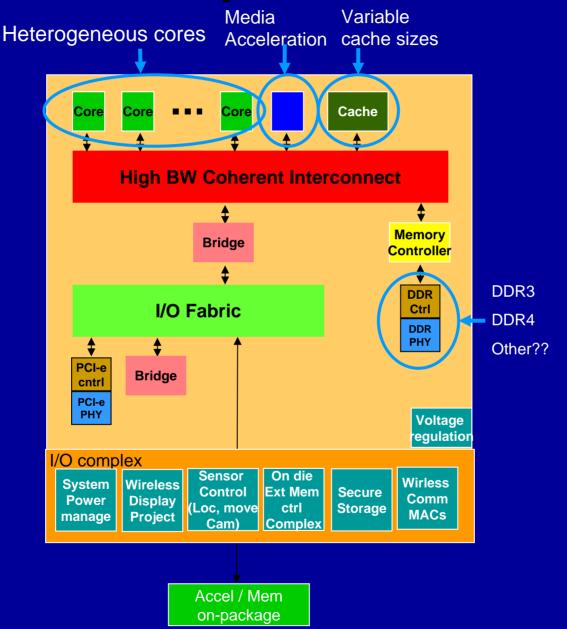


Progress in Modularity





What to Expect in 2014+?





Trend Implications to traditional Computing Arch - Summary

- Price Intel will continue drive to advanced process technology and aggressively address product cost
- Many Mobile Devices All Intel Mobile Client solutions to be Compute + Comm, always on, always connected
- SW/data spiral extending IA Top to Bottom + GP IA many core Media/Vector acceleration under one native programming model
- Growing segmentation Modular and Customizable "SOC like" architectures across all segments

