Pioneers in Collaborative Research®

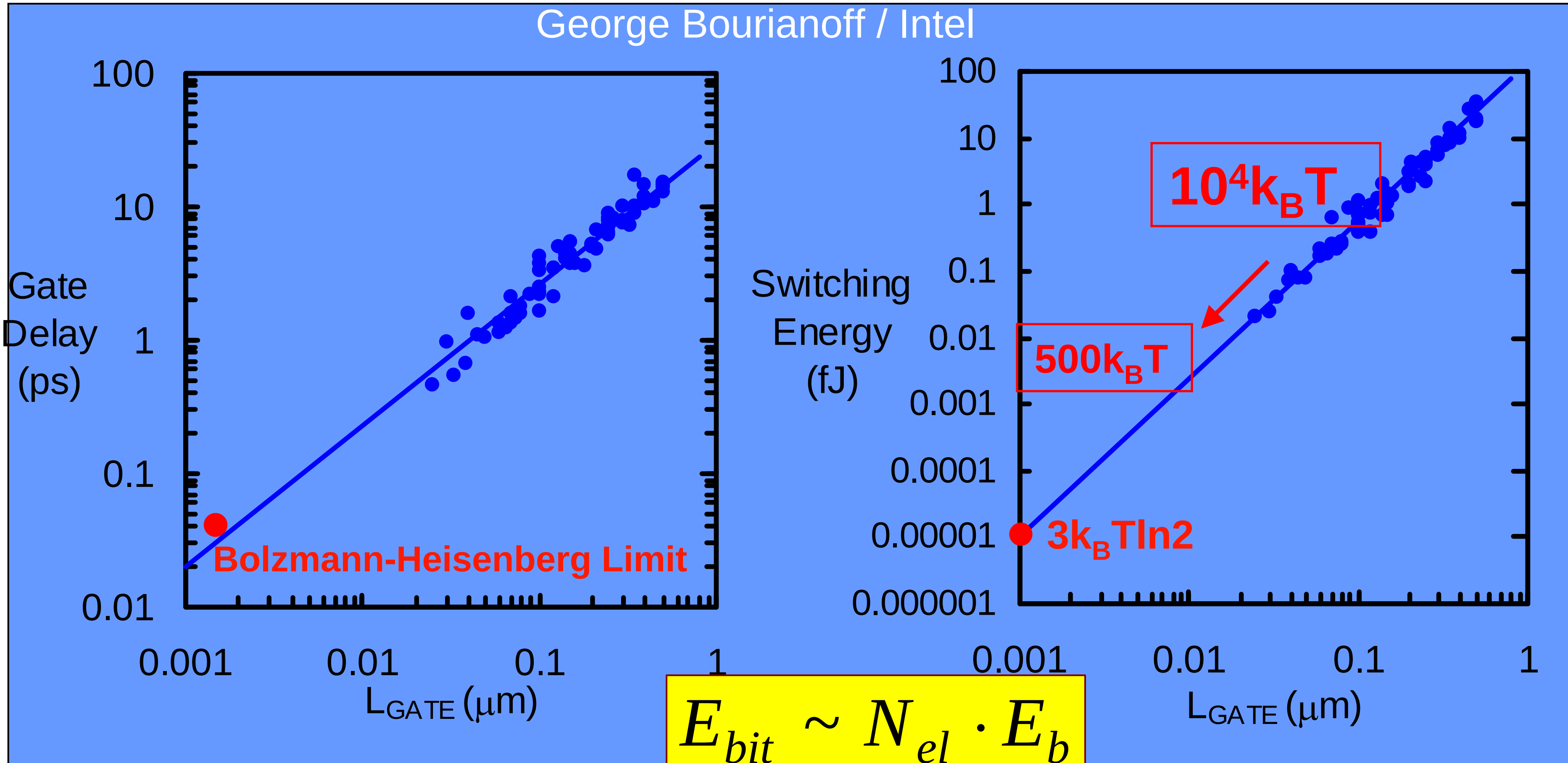
Device Opportunities for Beyond CMOS: A System Perspective

Victor Zhirnov

Question

- How will semiconductor nanoscale technology impact different information-processing and computing approaches?
  - Can emerging memory and logic technologies impact VIA-2020?

CMOS scaling on track to obtain physical limits for electron devices



$$E_{bit} \sim N_{el} \cdot E_b$$

***System reliability costs*: All *N* devices in the logic system operate correctly $E_b = f(N_{tr})$** $N_{tr} \uparrow \rightarrow E_b \uparrow$

***Fan-Out costs*: The need of each device to communicate to several others**

***Long communication costs*: Communication at distance is a very costly process**

} $N_{el} \uparrow$

Minimum number of electrons in interconnect line for communication and fan-out

N - number of electrons *F – fan-out* *k – number of tiles*

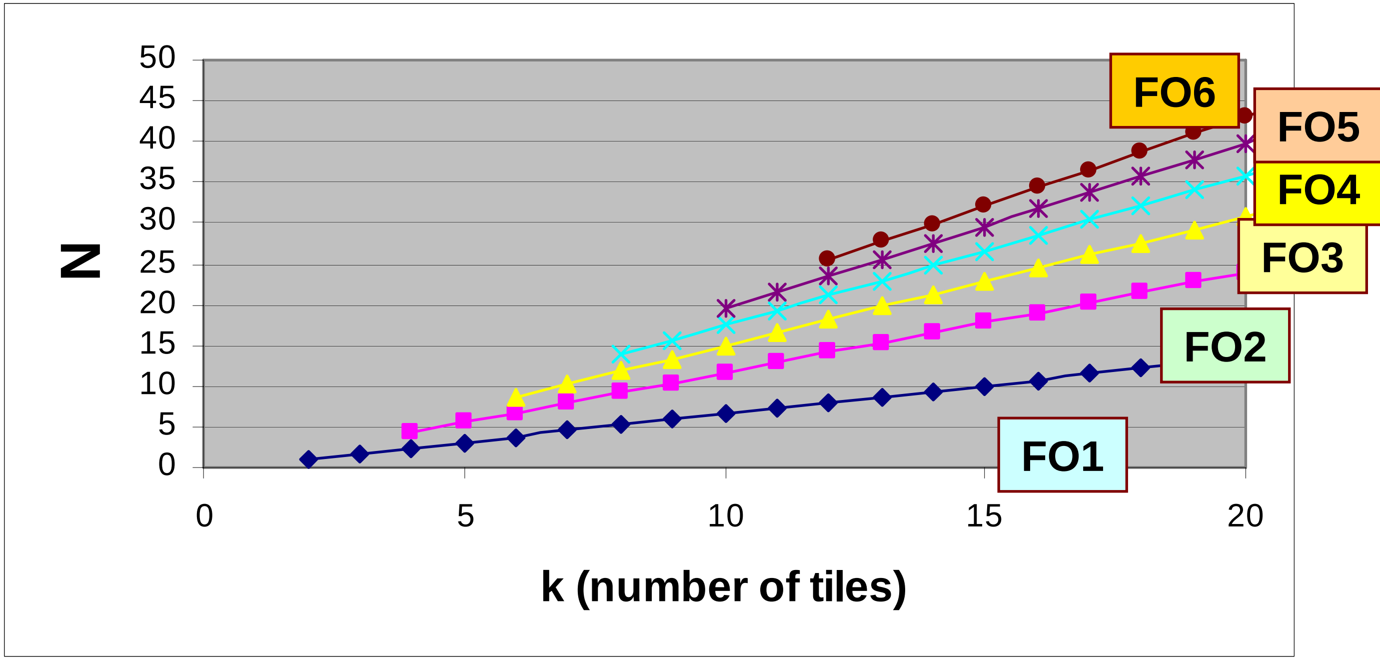
$$\Pi = \left(1-\left(1-\frac{a}{L}\right)^{N}\right)^{F}$$

$$\frac{L}{a} = k$$

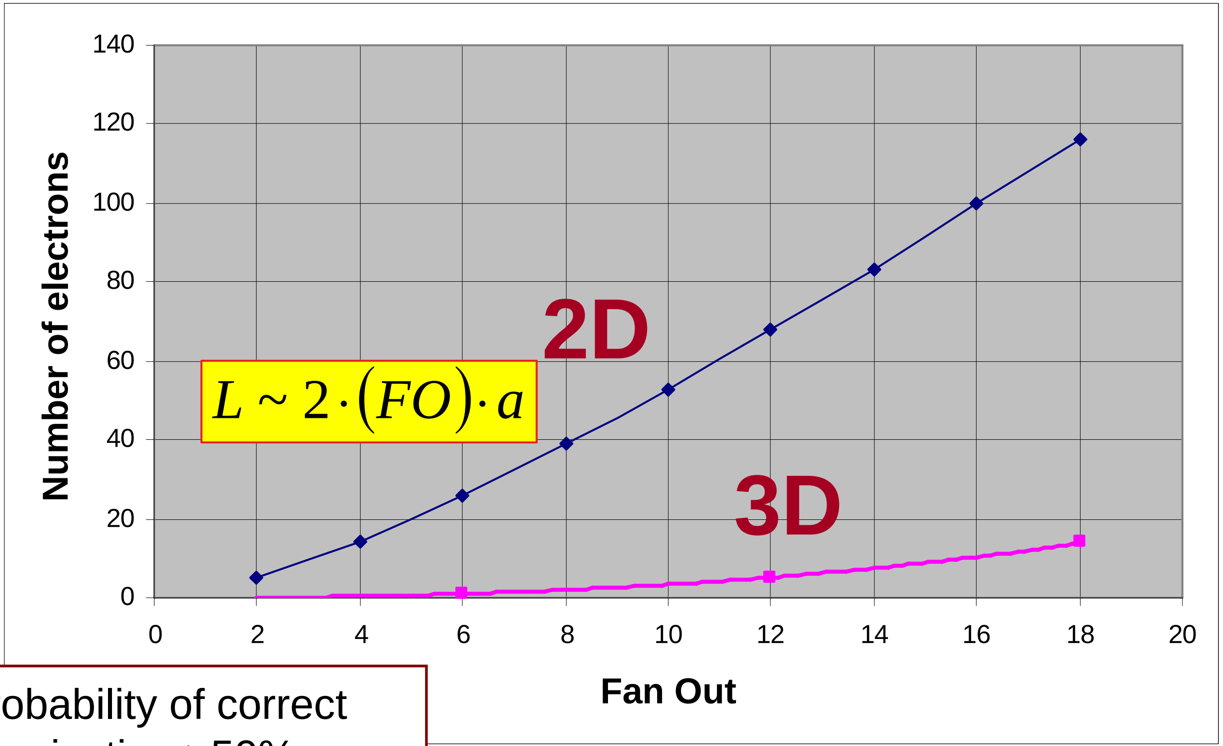
$$\Pi = \frac{1}{2}$$

$$\frac{1}{2} = \left(1-\left(1-\frac{1}{k}\right)^{N}\right)^{F}$$

$$N = \frac{\ln\left(1-\frac{1}{2^{F}}\right)}{\ln\left(1-\frac{1}{k}\right)}$$

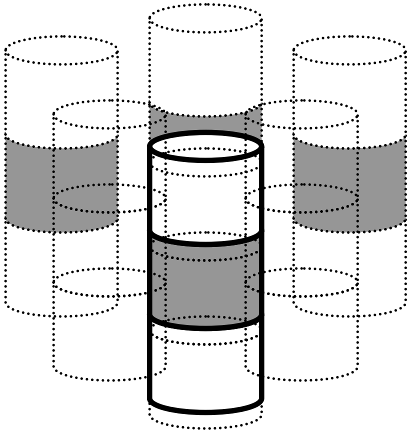


Energy costs for fan-out: 2D vs.3D



$L \sim 2 \cdot (FO) \cdot a$

For probability of correct communication >50%



Generic topology of a 3D binary switch

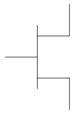
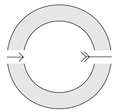
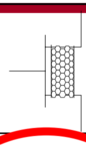
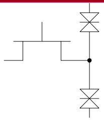
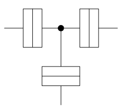
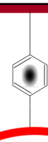
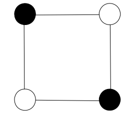
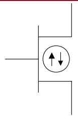
More Fan-Out (Branching) = More Computation

$$E \sim N \cdot E_b = N \cdot e \cdot V_{dd}$$

$$E \sim 3 \cdot 1.6 \cdot 10^{-19} \cdot 0.3 = 1.4 \cdot 10^{-19} J = 35 k_B T$$

Emerging Research Logic Devices

2003 ITRS ERD Chapter

Device								
	FET	*RSFQ*	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*	*Spin transistor*
Cell Size	100 nm	0.3 µm	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
Density (cm^{-2})	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
Switching Energy, J	2×10^{-18}	$>1.4\times10^{-17}$	2×10^{-18}	$>2\times10^{-18}$	$>1.5\times10^{-17}$	1.3×10^{-16}	$>1\times10^{-18}$	2×10^{-18}
Binary Throughput, $GBit/ns/cm^2$	86	0.4	86	86	10	N/A	0.06	86

<u>System driven evaluation:</u> 1D structures appear to be promising

Summary Comparison of Electronic, Spin and Optical State Computing

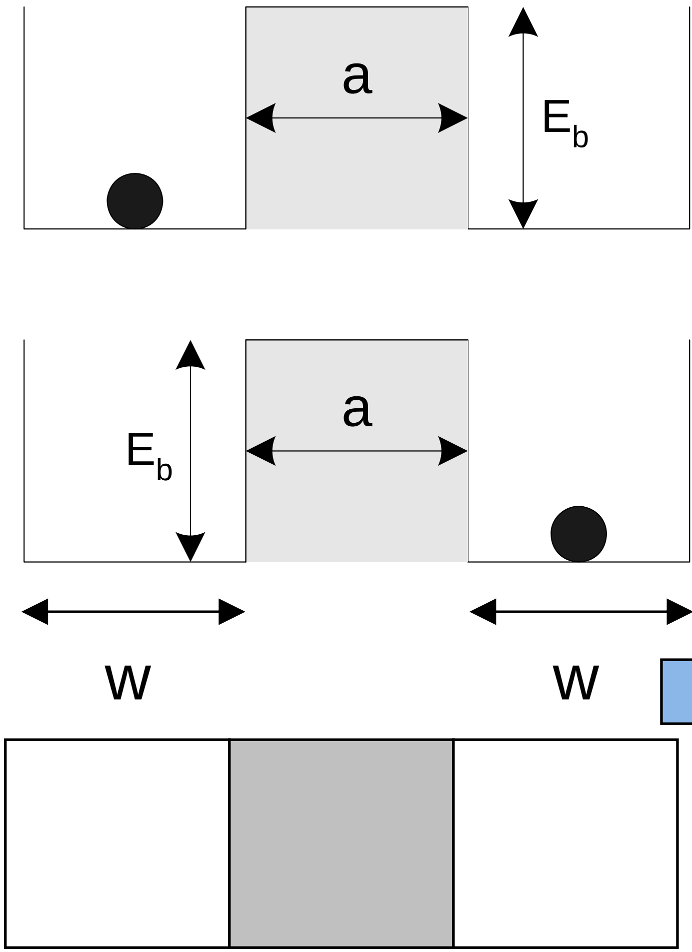
	Lower bound (Impractical Limit)	
Mechanism	Energy	Size
Electronic	$3k_BT$	1 nm
Spin	$70k_BT$	7 nm
Optical	$3600k_BT$	20 nm

→ Practical limit ~3-5 nm

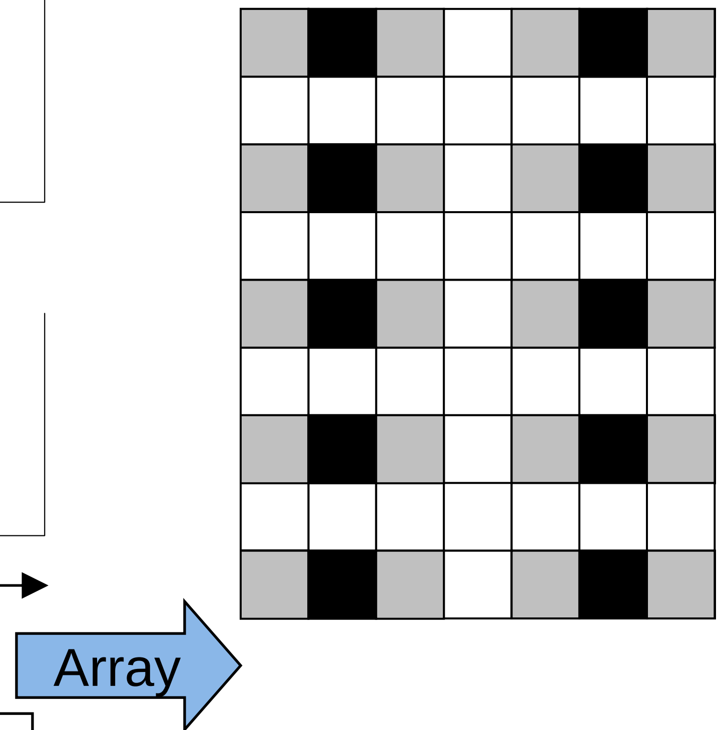
→ Practical limit >20 nm

→ Practical limit >90 nm

Two-well bit – Universal Device Model



Generic Floorplan
of a binary switch



Device density

1) Upper Bound

$$n_{\max} = \frac{1}{8a^2}$$

2) IC (ITRS)

$$n_{MPU} = \frac{1}{(20a)^2}$$

Can we have smaller tile?

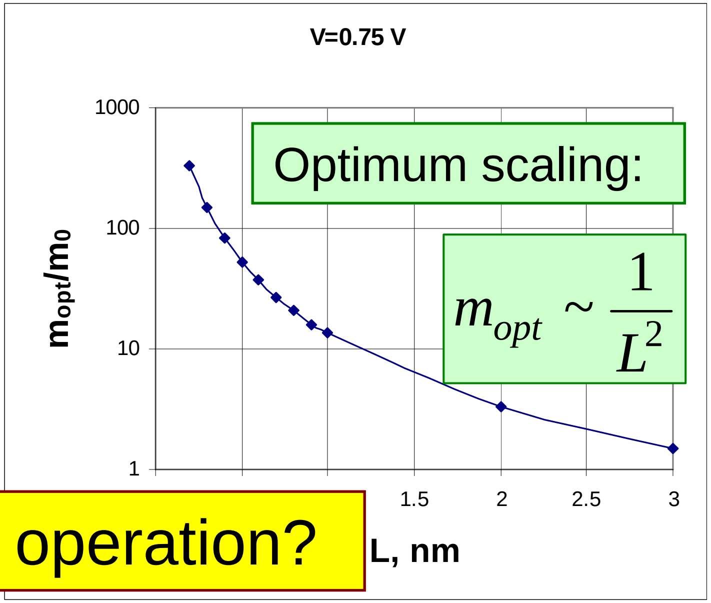
How can we go below 5 nm?

2006 hypothesis: Devices having feature sizes less than 5 nm should utilize particles whose mass is greater than the mass of an electron. Below about 5 nm, the mass of information-bearing particle should exceed free electron mass.

This conclusion resulted from the Heisenberg limit on device size

$$L_{\min} = \frac{\hbar}{\sqrt{2mE_b}}$$

$$L\sqrt{m} = const$$



Does heavier mass always imply slower operation?

$$t_{sw} = \frac{L}{v} = L\sqrt{\frac{m}{2E}}$$

$$E = \frac{mv^2}{2}$$

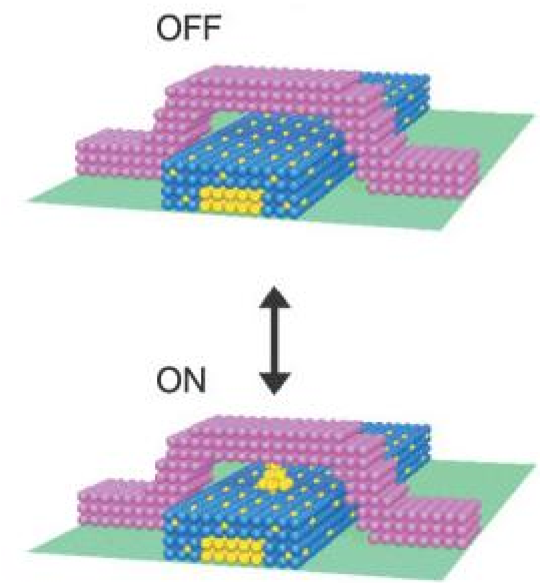
$$t_{sw} \sim L\sqrt{m}$$

Heavy-electron materials?

or

Moving atoms instead of moving electrons?

Moving atoms I: ‘Atomic Relay’



Atomic-scale switch, which opens or closes an electrical circuit by the controlled reconfiguration of silver atoms within an atomic-scale junction.

Such ‘atomic relays’ operate at room temperature and the only movable part of the switch are the contacting atoms, which open and close a nm-scale gap.

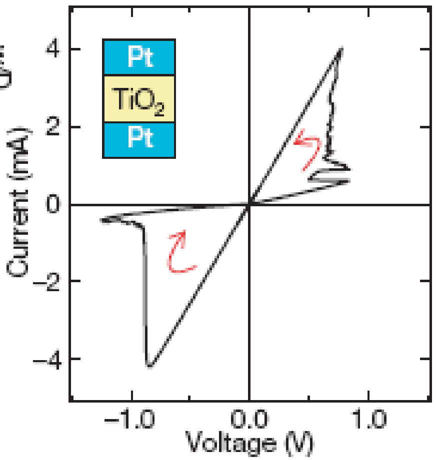
- Small (~1 nm)
- Fast (~1 ns) - projection
- Low voltage (<1V)

Nature **433**, 47-50 (6 January 2005)

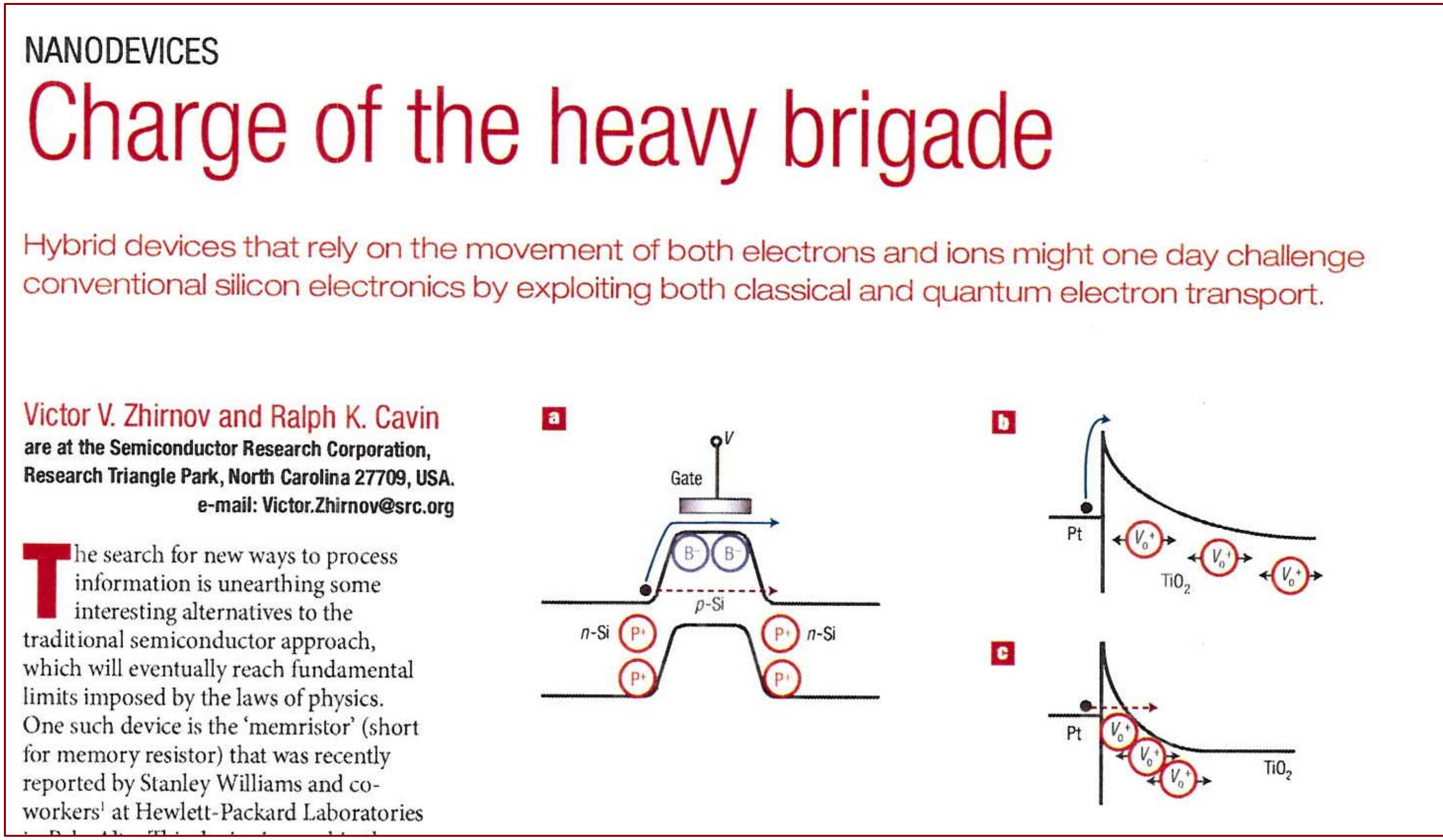
Quantized conductance atomic switch

K. Terabe, T. Hasegawa, T. Nakayama and M. Aono

Moving atoms II: ‘Memristor’



D. B. Strukov, G. S. Snider, D. R. Stewart & R. Stanley Williams, Nature 453, May 2008, 80-83



NANODEVICES

Charge of the heavy brigade

Hybrid devices that rely on the movement of both electrons and ions might one day challenge conventional silicon electronics by exploiting both classical and quantum electron transport.

Victor V. Zhirnov and Ralph K. Cavin
are at the Semiconductor Research Corporation, Research Triangle Park, North Carolina 27709, USA.
e-mail: Victor.Zhirnov@src.org

The search for new ways to process information is unearthing some interesting alternatives to the traditional semiconductor approach, which will eventually reach fundamental limits imposed by the laws of physics. One such device is the ‘memristor’ (short for memory resistor) that was recently reported by Stanley Williams and co-workers[1] at Hewlett-Packard Laboratories

V. V. Zhirnov and R. K. Cavin, Nature Nanotechnology, July 2008

Moving Atoms III: Nanowire phase-change memory

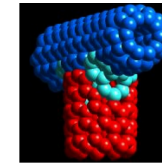
- Nanowire phase-change memory

  M. Meyyappan et al, APPLIED PHYSICS LETTERS 91 SEP 24 2007

- Goal:
  - Low-Voltage Non-volatile memory to replace SRAM
    - Quasi 1D (e.g. nanowire) components

Ultimate Phase-Change Memory ?

Ames Research Center



Technology Goal

Develop low-power high-density data storage using nanomaterial *array*, enabling *10^2~10^3X faster R/W, 10~15X lower write voltage*, and *10~100X higher integration density*

Technology Challenges

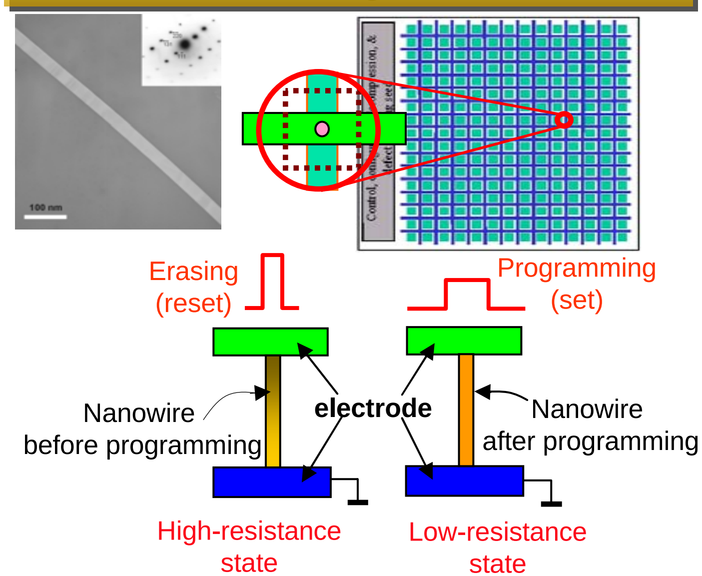
- ❑ Super-scalable R-switching nanowire memory
- ❑ Large-scale self-assembly / patterned assembly
- ❑ 3-D integration / selecting device

Next-generation highly scalable, ultra-low power, resistive switching non-volatile memory chip technology based on phase-change nanomaterials

Technical Approach

- ❑ 3-D vertical nanowire array
- ❑ Non-charge-based (radiation-free)
- ❑ Significantly reduced thermal writing energy (10^2~10^3X)
- ❑ Super scalable memory cell
- ❑ Reduced thermal interference
- ❑ Multi-layer stacking for high integration density
- ❑ Binary or analog data storage
- ❑ Low temperature assembly compatible with Si-IC platform

Resistive Switching in PC Nanowire



Anticipated Performance Metrics

- *Target 0.5~1 V R/W operation*
- *1 μA/cell reset current*

- *1 TB/cm² density*
- *<10^{-12} J/bit switch energy*

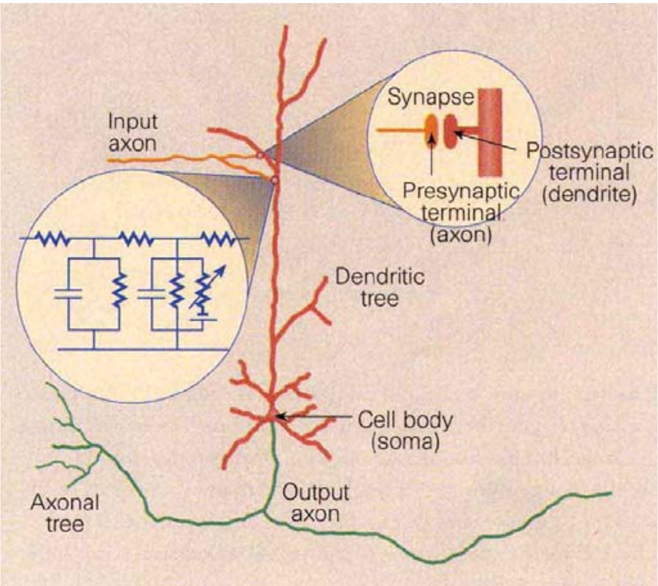
- *Less than 10 ns write time*
- *10^{10} cycle endurance*

Moving atoms IV: Ions in liquid electrolytes

Ions in liquid electrolytes play an important role in biological information processors such as the brain

In the human brain, the distribution of **Ca** ions in dendrites may represent a crucial variable for processing and storing information.

Ca ions enter the dendrites through voltage-gated channels in a membrane, and this leads to rapid local modulations of calcium concentration within dendritic tree



C. Koch, "Computation and single neuron",

Nature 385 (1997) 207

Based on the brain analogy, the binary state can be realized by a single ion that can be moved to one of two defined positions, separated by a membrane (the barrier) with voltage-controlled conductance

Ions are heavy, but brain seems to use them efficiently!

Key Messages

- 1D structures could be enabling!
  - 1D logic devices to reduce fan-out costs
- Topology optimization for energy reduction
  - Quasi 1D (e.g. nanowire) components arranged in 3D structures
- It appears that, in principle, scaling of devices can continue well below the electron limit
  - Below about 5 nm we need particles whose mass exceeds that of the electron