SRC Board Retreat 2009

Research Opportunities at the Interface of Design and Technology

GLOBALFOUNDRIES

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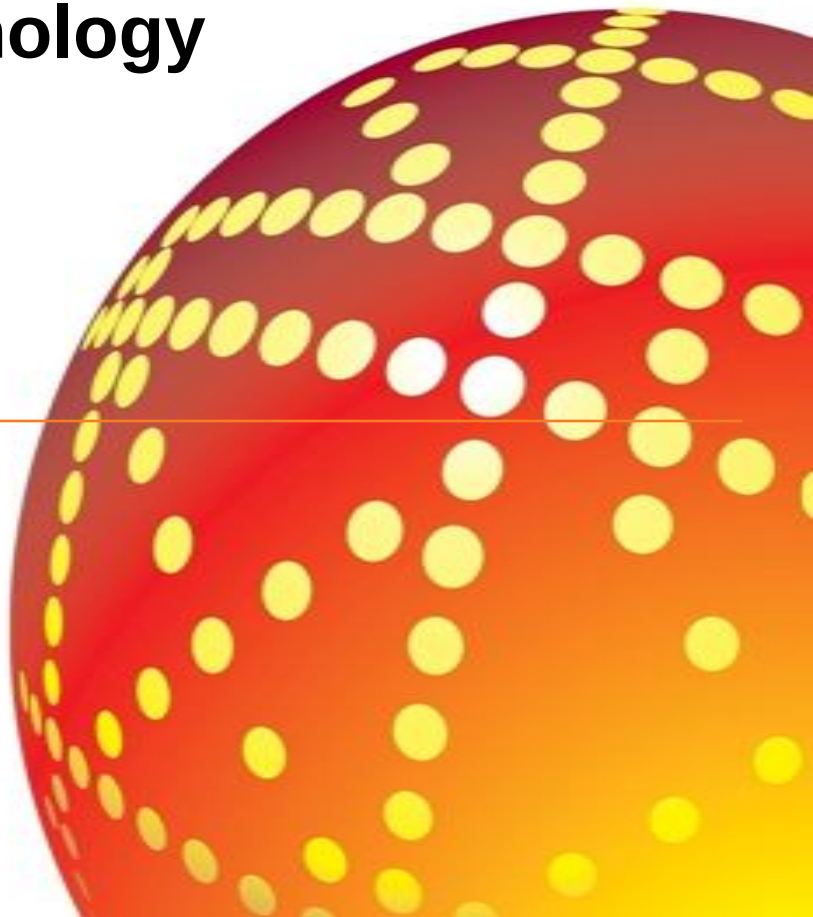
SVP, Design Enablement
July, 2009

Confidential



Agenda

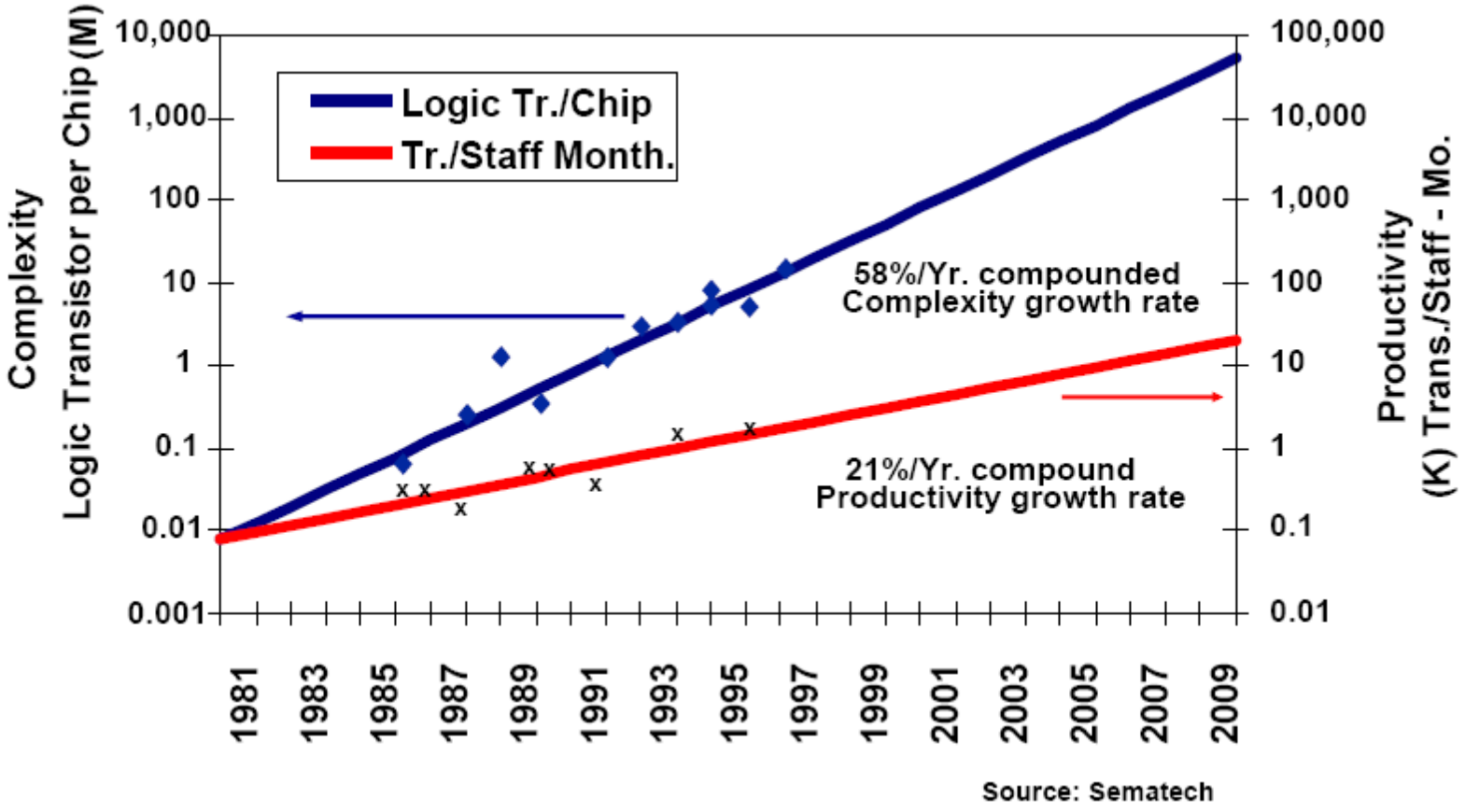
- **Industry landscape**

- **The race for performance (low power that is!)**
- **The race for TTM**
- **The race for lower cost**

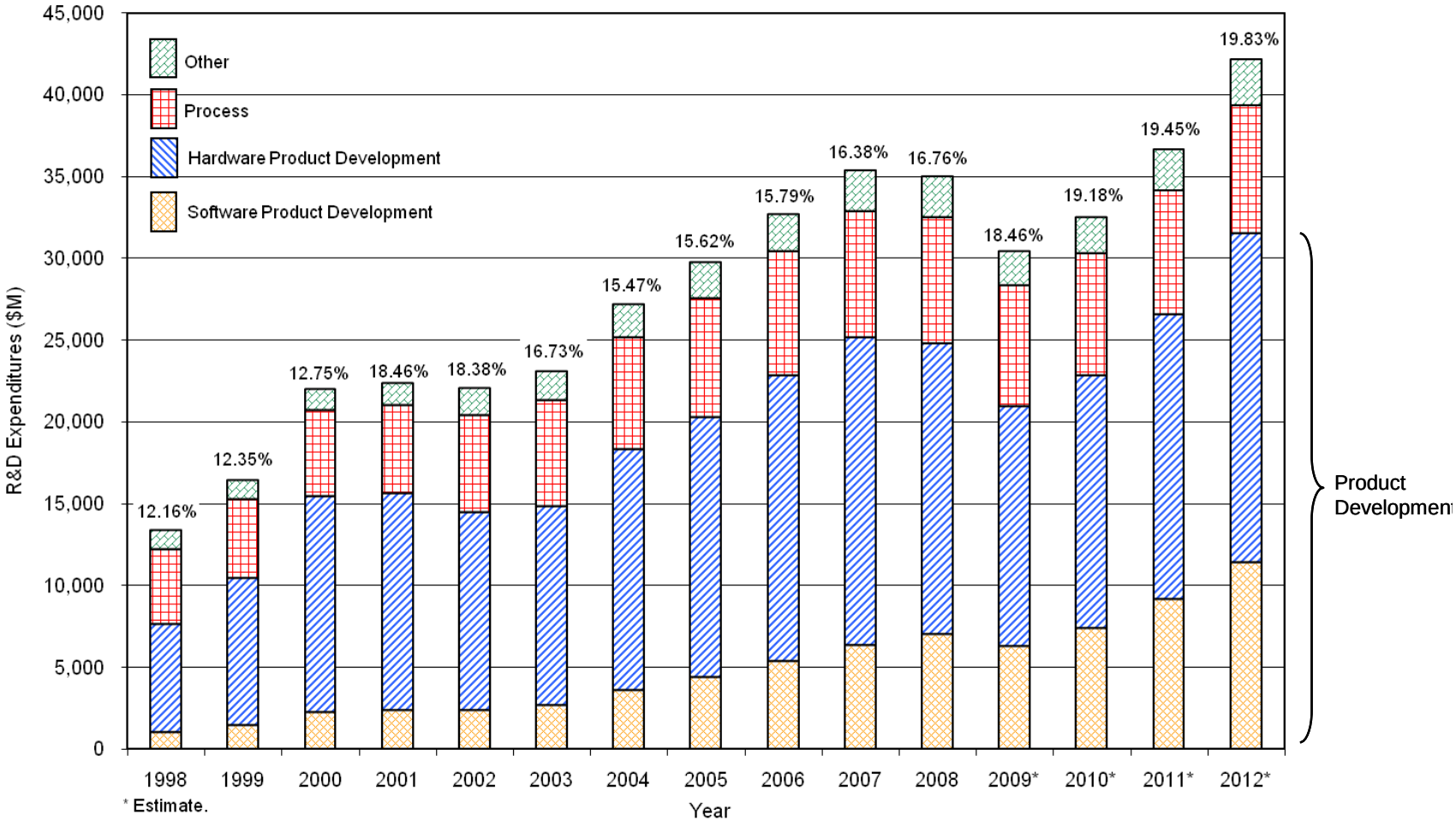
- **Research needs**
- **Conclusion**

Industry Landscape

Complexity Outpaces Design Productivity



R&D Expenditures in the IC Industry

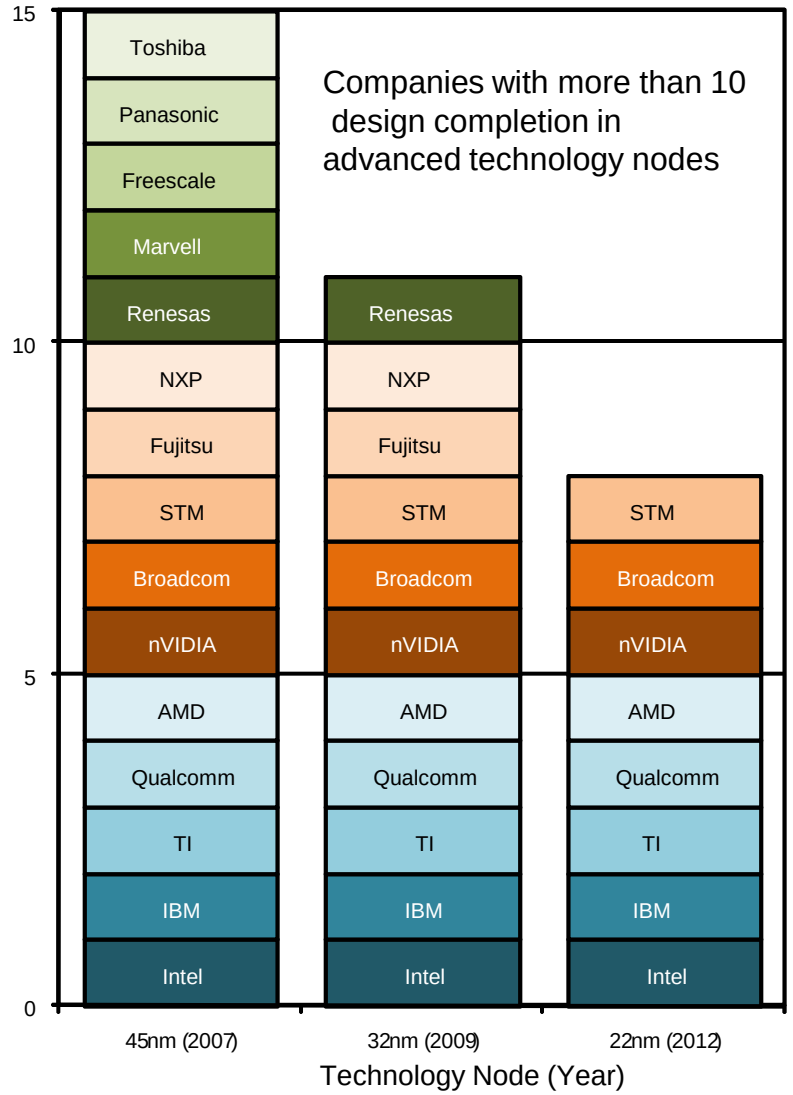


Source: IBS

Bifurcation in Technology Adoption

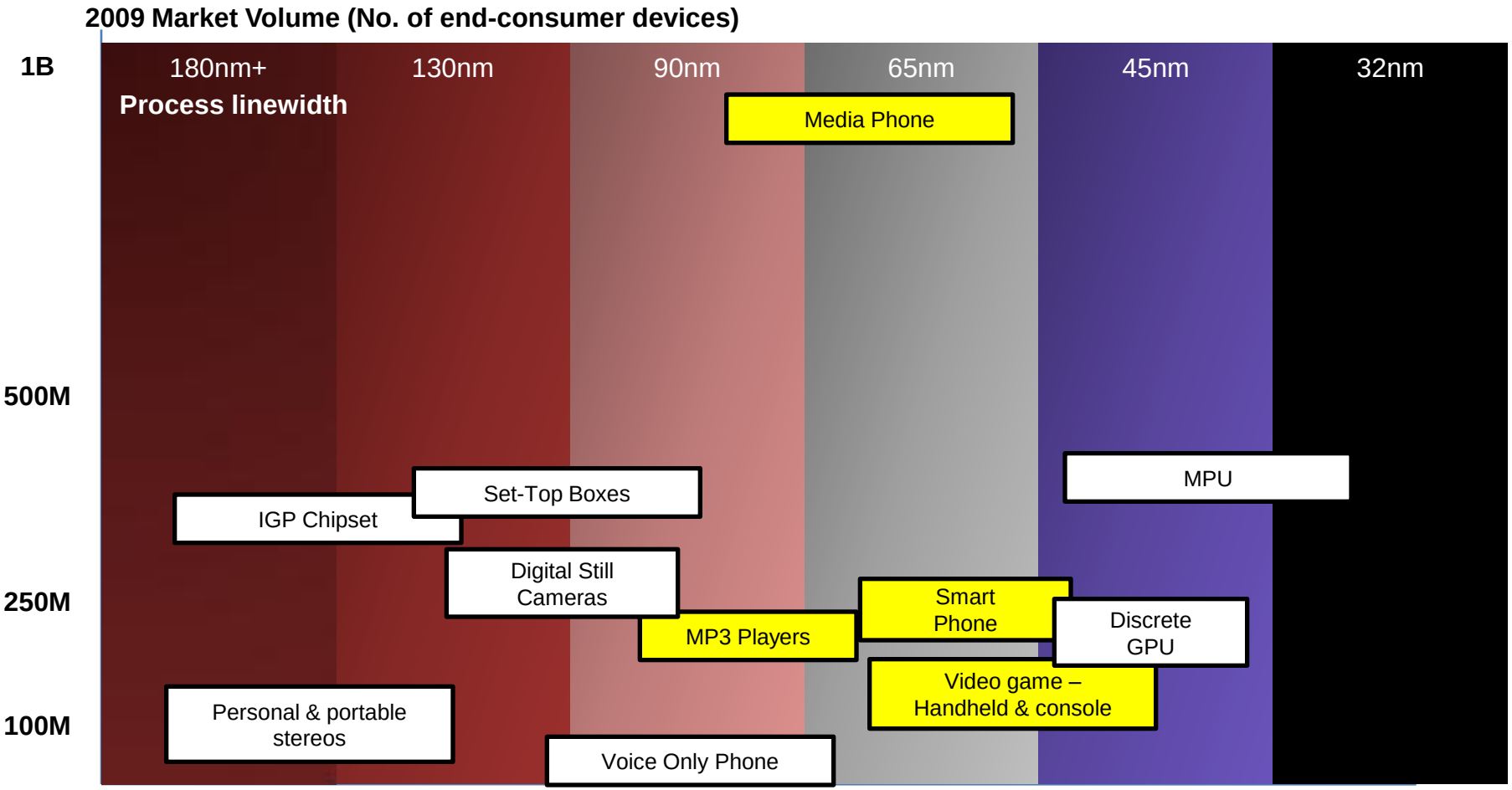
- **Large IC companies are aggressively adopting new technologies**
- **Advanced technologies as a major competitive advantage**
  - **Primarily to reduce cost per function**
- **Bifurcation in technology adoption**
  1. **An elite club on an aggressive technology adoption model**
  2. **The median of ASIC starts is still at 130nm & 90nm**

Declining leading edge product designs?



Source: IBS

Volume at advanced technologies is increasing



Source: Bridge & GLOBALFOUNDRIES analysis, iSuppli Mobile Handset Tracker; iSuppli Consumer Platforms Market Tracker , Mercury Reports GPU, Gartner Reports GPU

Foundry leading customers

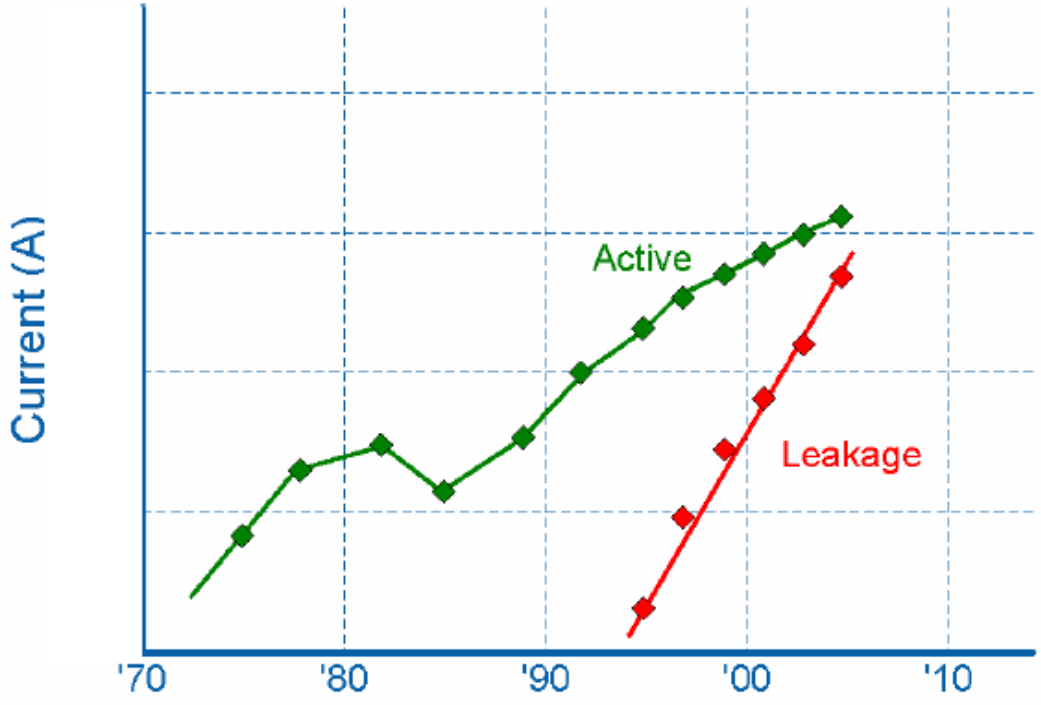
- **Customer base is consolidating**
  - Big fabless IC companies are getting bigger
  - Small players are becoming less significant
- **Revenue from advanced technologies is increasing**
- **IC bets have become larger**
  - Over $500M in R&D to move to a new node
- **Early foundry-customer engagement**
  - Read: early design-technology engagement
- **Technology-circuit analysis and trade offs to maximize value**
  - Process-design co-customization
- **Concurrent design-process development**
  - Customer specific program and interim deliverables

The race for performance

Design-technology co-optimization

Power trend is counter scaling

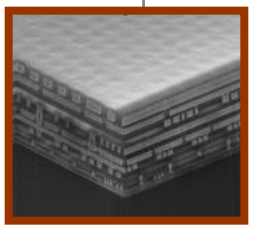
- **Vcc scaling has significantly slowed down**
  - Now dropping only about 50mv per technology node
- **Smaller geometries give rise to higher leakage**



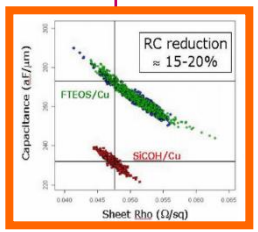
Source: Pant, Mandy, Intel

Technology Innovations

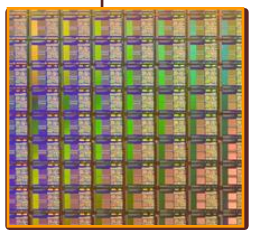
2000	2002	2003	2004	2006	2008	2010
180nm	130nm	130nm	90nm	65nm	45nm	32nm



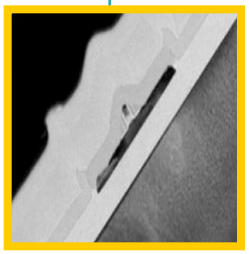
Cu Interconnect



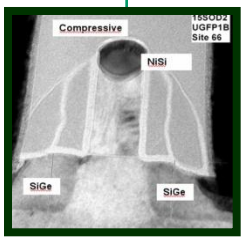
Low-K dielectric



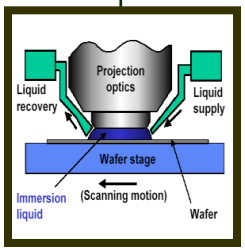
SOI



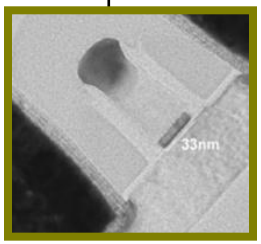
Strained-Si



Multi-Strain Transistor

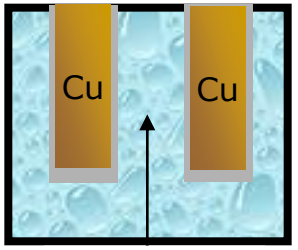


Immersion Lithography



HKMG

- **Technology innovations have enabled economical scaling**
  - **Provided enough value to outweigh the cost**



Pores in dielectric

ULK

But More Can Be Done!

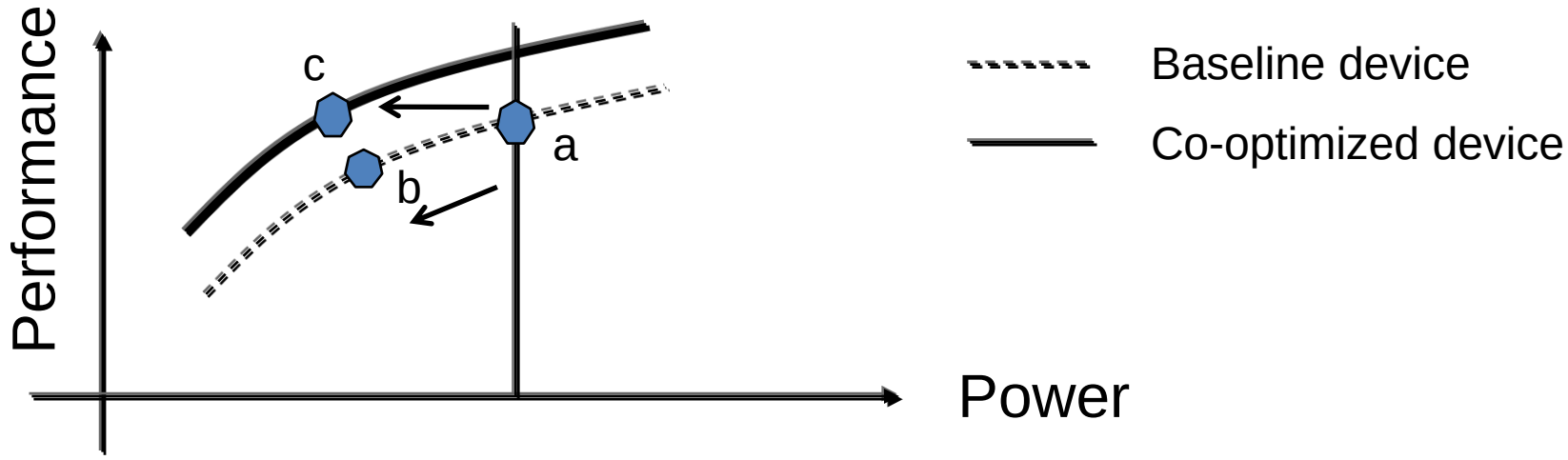
Vectors of Technology-Design Co-Optimization

1. **Power - Performance co-optimization**
   - Moving along the universal curve to attain optimum speed-power point
     - Vcc, Vt, Lgate, back bias optimization
     - Optimizing transistors at different bias points
   - Add new devices to the process

2. **Design - Process Variability co-optimization**
   - Understand circuit margins, critical specs and their process dependency
   - Co-optimize process and design to minimize guard bands for variability

3. **Layout - Design Rule co-optimization**
   - Assess impact of design rules (or DFM rules) on layout
   - Optimize layout to use a subset of design rules with minimal impact to layout

Design/Technology Co-Optimization



- **Co-optimization focuses on tuning critical device parameters to improve product performance**
  - Collaborative work between design and technology is critical
- **In most cases, this would entail moving along the universal curve (a → b)**
  - Same power-performance curve
- **But it can also reduce power at the same performance (a → c)**

A Recent Co-Optimization Example

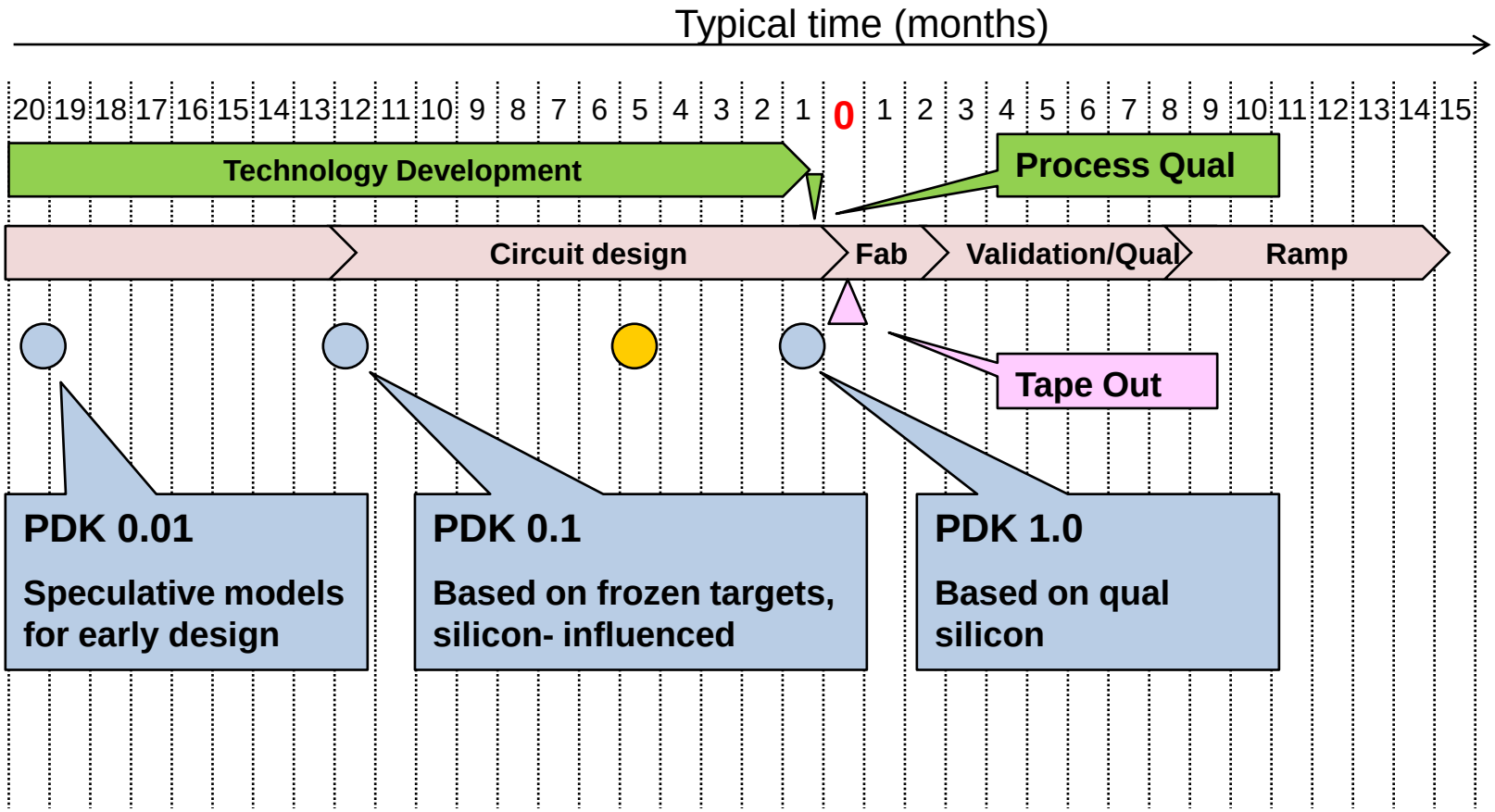
Technology	Performance	Static Power	Total Power
Baseline Device	1	1	1
Co-Optimized Device	1.04	0.7X	1

- **Equivalent of up to about ¼ node advantages can be attained by circuit-technology co-optimization**

The race for TTM

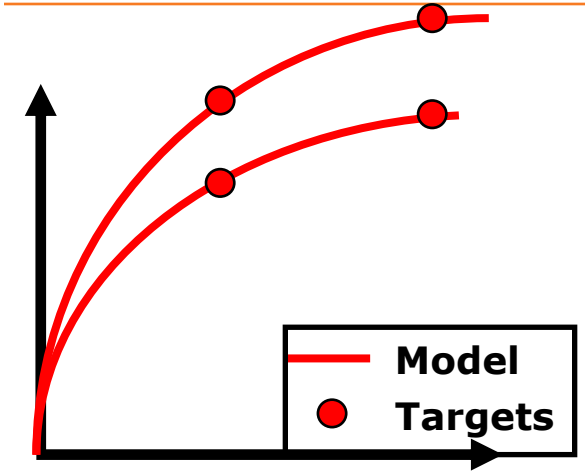
Concurrent design-technology development

Concurrent Technology & Design Development



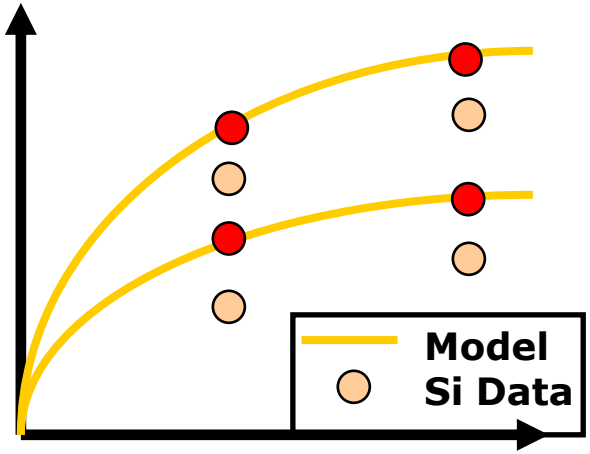
Source: Industry interviews and research; team analysis

SPICE Model Maturity



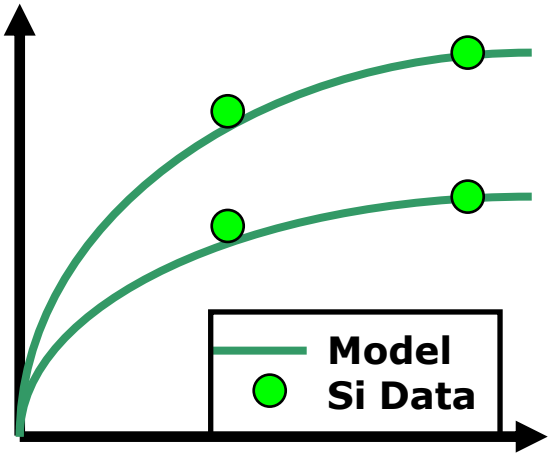
Speculative Model

Rev. S.. (Rev 0.01_xx)



Si-Influenced Model

Rev. P.. (Rev 0.1_xx)

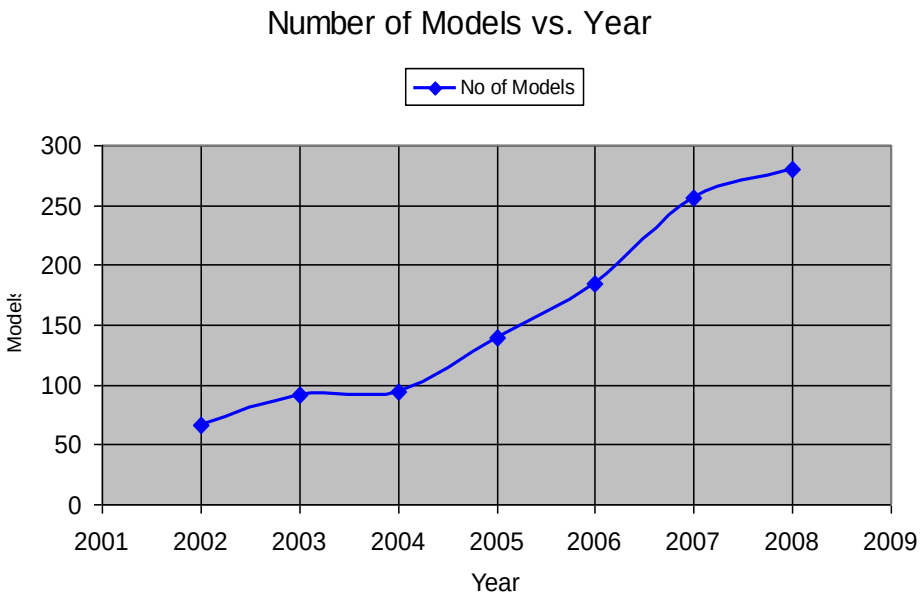


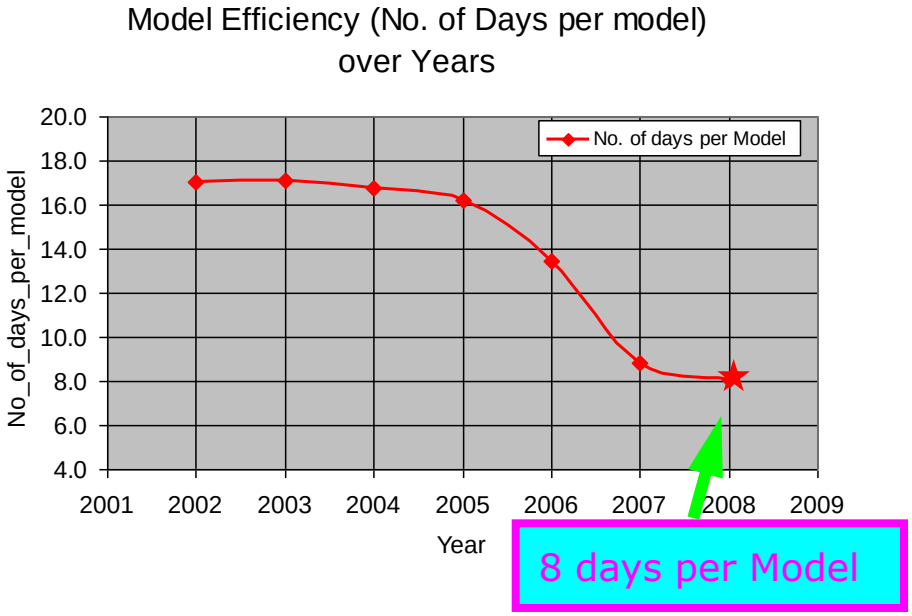
Si-Based Model

Rev. D..(Rev 1.0_xx)

- **Speculative – 0.01**
  - *Based on early prediction of the targets, validated with very early silicon*
  - *Early design start*
- **Silicon-influenced – 0.1**
  - *Based on the frozen targets, validated but does not match early silicon*
  - *Design in full motion*
- **Silicon-based – 1.0**
  - *Based on final, qual silicon*
  - *Not much influence on the 1st tape out*

Model Extraction Efficiency Improvement





Significant increase in number of models over the years

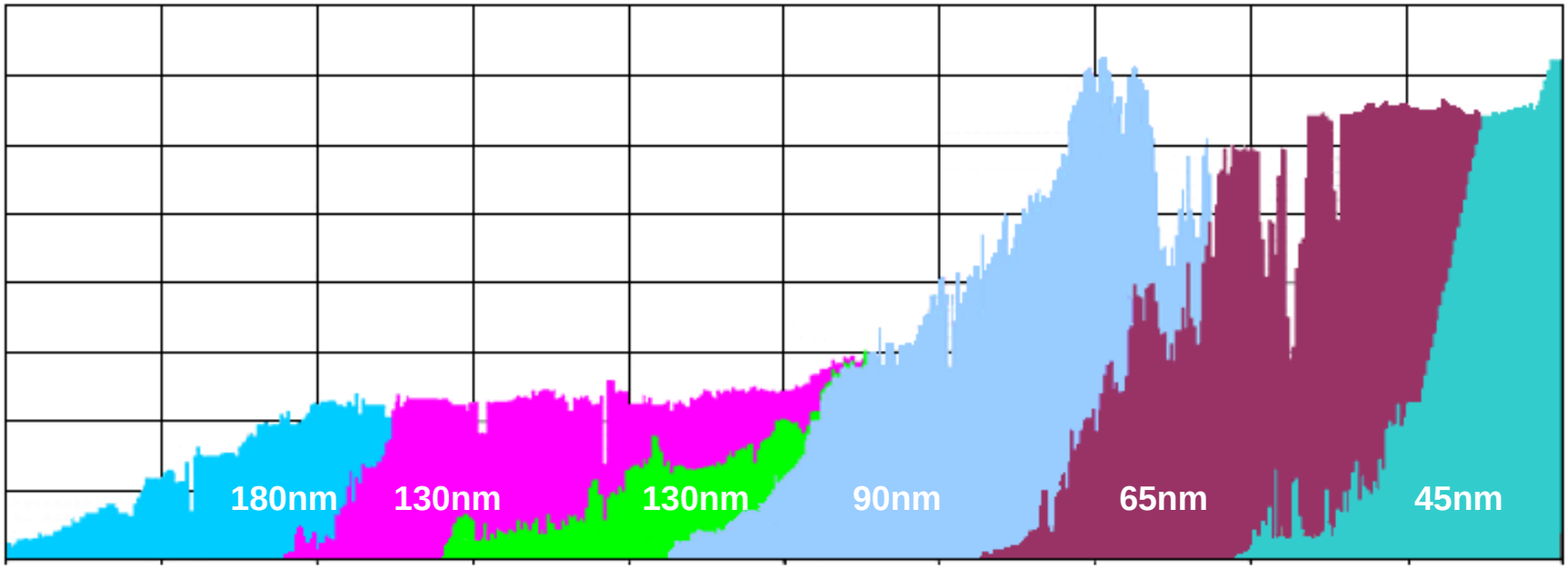
Significant increase in modeling efficiency

The race for lower cost

Improve yield and yield ramp

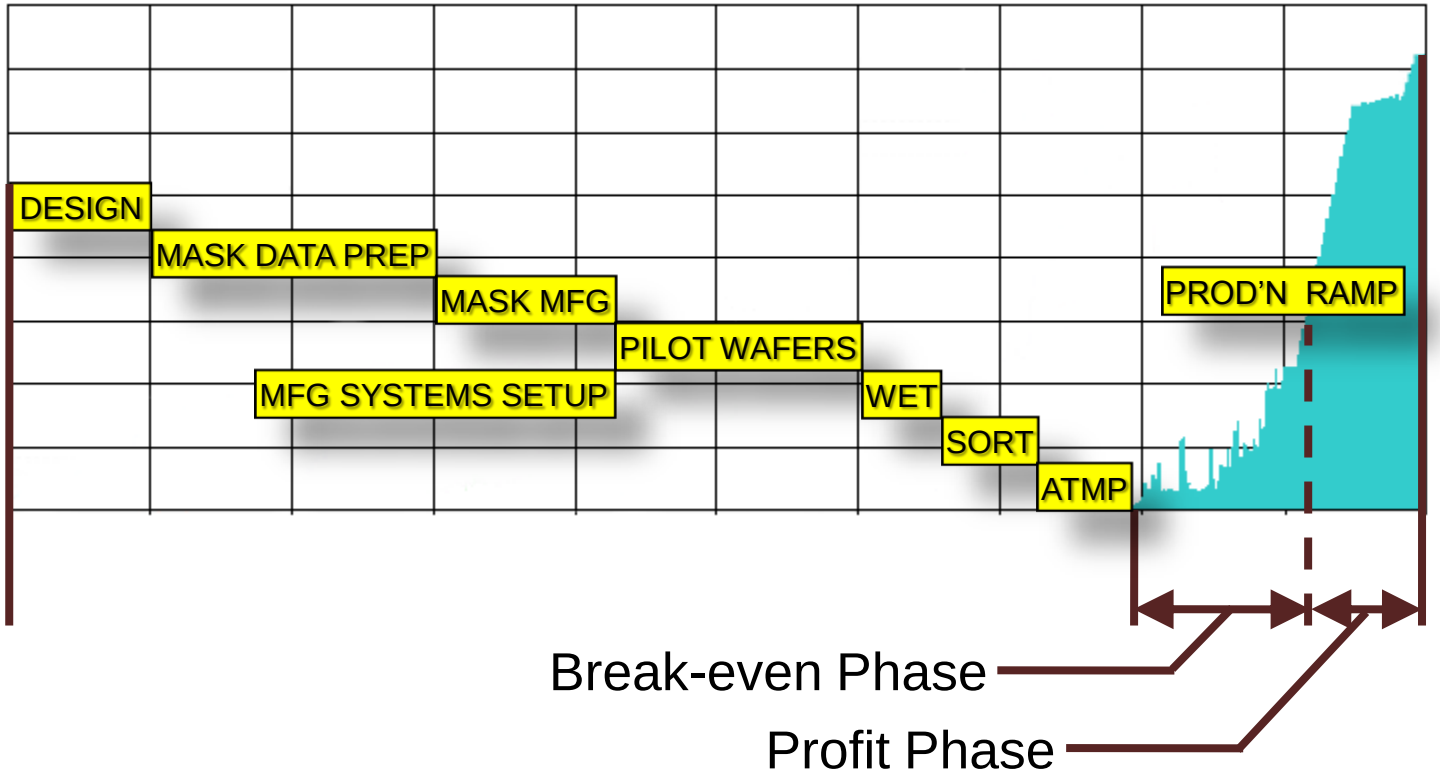
Quick Production Ramp

- **The pace of advanced technology development continues**
- **With quick ramp to high volume**
- **Accelerated defect density reduction and yield ramp**
- **Emphasis on speed, accuracy, and agility across manufacturing**
  - Automated Precision Manufacturing (APM)



GLOBALFOUNDRIRS Production Ramp

Agility Translates into Customer Value



Faster Cycles of Learning + Shorter Time to Mitigate Risk
Result in
Faster Time To Market & Higher ASP's for Customers

Research Needs & Conclusion

Research Needs

- **ROI necessitates maximizing value from advanced technologies**
- **So the race intensifies ……**

- **Research needs:**

  Not a comprehensive list – but a list in support of the topic:

  - **Process technology innovations aimed at lower power**
  - **Target based process development and design methodology**
  - **Tools and methodologies for predicting device performance prior to silicon**

  - **Tools and methodologies for concurrent design and technology development**
  - **Tools and methods for fast development and assembly of tech files and PDK**
  - **Optimizing Restricted Design Rules (RDR) to minimize layout impact**

  - **Integrated DFM and impact of DFM on design and manufacturing**
  - **Manufacturing automation tools**
  - **Tools and methodologies to aid fast silicon volume ramp and fast defect density reduction**

Conclusion

- The sky is the limit
- Gravity is good – research needs to be connected to vectors of value
- Opportunities are often in the interfaces
- Economic trends dictate technical research directions