Semiconductor Roadmap and Bioelectronics

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Outline

- International Technology Roadmap for Semiconductors (ITRS)
- ITRS Emerging Research Devices (ERD) Chapter
  - Lessons from Nanoelectronics roadmap
    - *ERD chapter*
- Roadmapping for Bioelectronics?
  - Can we use some ITRS methodology?

International Technology Roadmap for Semiconductors (ITRS)

- A very detailed industrial perspective on the future requirements for micro/nano electronic technologies
  - Goal is to continue exponential gains in performance & price for the next fifteen years
- Built on worldwide consensus of leading industrial, government, and academic technologists
- Provides guidance for the semiconductor industry and for academic research worldwide

International Technology Roadmap for Semiconductors (ITRS)

- Contains critical requirements and judgment of status
- Projects that by 2020, half-pitch spacing of metal lines will be 14 nanometers and device gate lengths will be 5 nanometers vs. today's commercially produced 45-nm lines and 25-nm gate lengths.
- Major update every two years

ITRS Origins

- **1983-1994:** SRC announces ten year research goals
- **1990:** SRC leads in establishing NACS resulting in MICRO TECH 2000 expert meeting; precursor to ITRS
- **1992:** National Technology Roadmap for Semiconductors (NTRS) effort led by SRC and SIA defines industry five-year goals
- **1994:** NTRS updated and horizon extended to 15 years
- **1998:** Roadmap is internationalized and becomes the International Roadmap for Semiconductors (ITRS)

Chapters of ITRS 2007

http://public.itrs.net

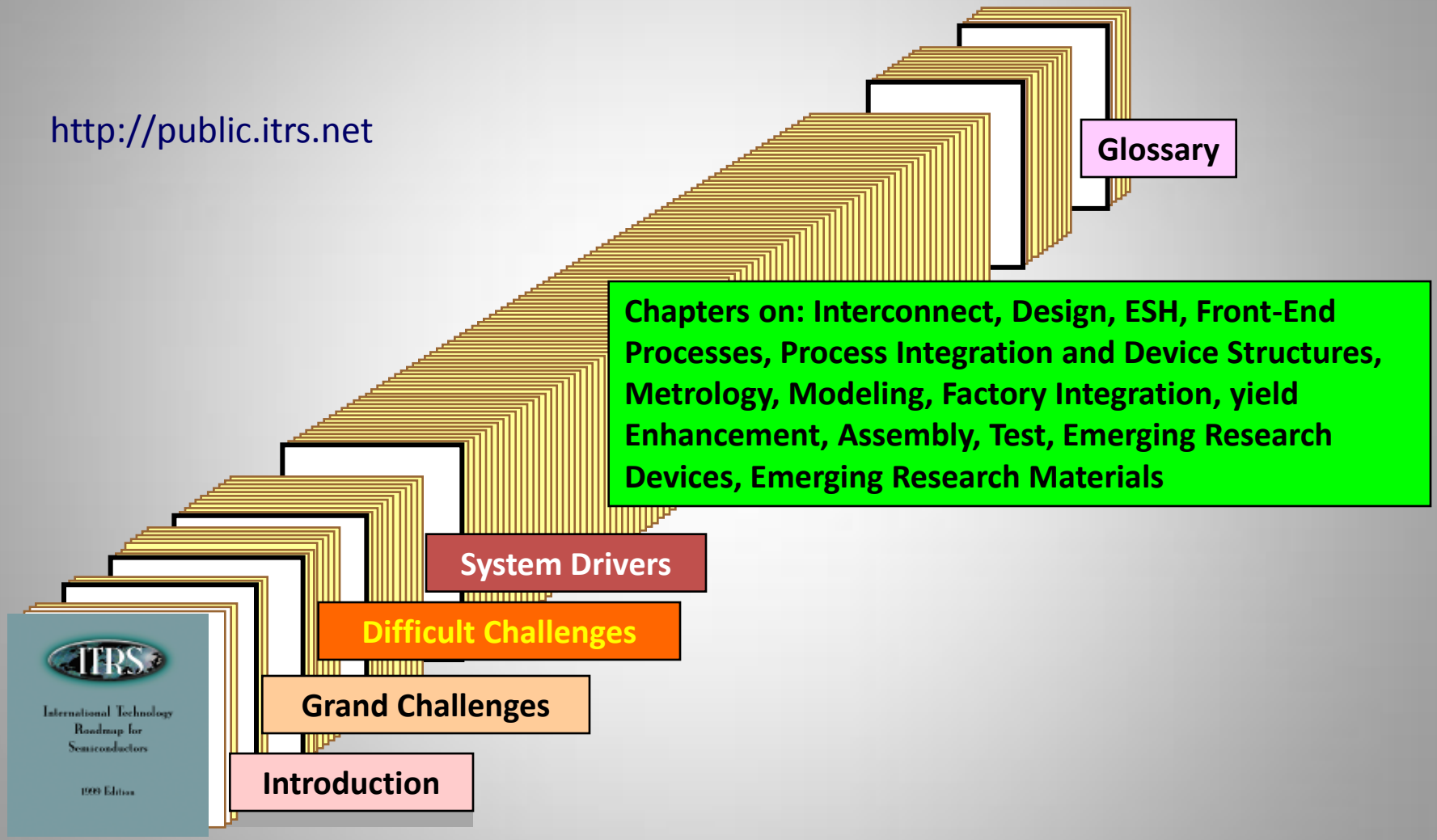


Table Color Scheme

Solutions Exist

White

Solutions Being Pursued

Yellow

No Known Solutions

Red

CMOS Scaling Challenges (2001)

Table 2a High Performance Logic Technology Requirements—2001 ITRS

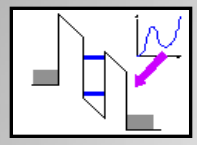
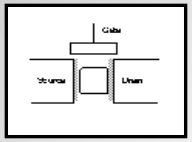
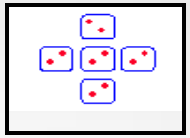
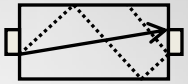
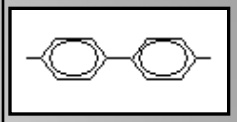
Calendar Year	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
Technology Node	130nm			90nm			65nm	45nm	32nm	22nm
MPU Gate Length	65	53	45	37	32	30	25	18	13	9
Gate Dielectric Equivalent Oxide Thickness (EOT) (nm) [1]	1.45	1.35	1.35	1.15	1.05	0.95	0.85	0.65	0.50	0.45
Electrical Thickness Adjustment Factor (Gate Depletion and Quantum Effects) (nm) [2]	0.8	0.8	0.8	0.8	0.8	0.8	0.5	0.5	0.5	0.5
Tox Electrical Equivalent (nm) [3]	2.25	2.15	2.15	1.95	1.85	1.75	1.35	1.15	1.00	0.95
Vdd (V) [4]	1.2	1.2	1.1	1.0	0.9	0.9	0.8	0.6	0.5	0.4
Sub-Threshold I-off @25°C (uA/um) [5]	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Id-NMOS @Vdd (uA/um) [6]	926	1001	924	905	878	961	1076	1218	1523	1465
Required "Technology Improvement" (SOI/Low-Temp/High-mobility) [7]	0%	0%	0%	0%	0%	0%	0%	30%	70%	100%
Rsd Percent of Ideal Channel Resistance (Vdd/IdNMOS with no RSD) [8]	16%	16%	17%	18%	19%	19%	20%	25%	30%	35%
Parasitic Capacitance Percent of Cgate [9]	19%	22%	25%	27%	29%	29%	27%	31%	35%	42%
Intrinsic Frequency (1/Tau) (GHz) [10]	624	764	873	1013	1166	1282	1531	2603	4424	6460
Relative Device Performance [11]	1.0	1.2	1.4	1.6	1.9	2.1	2.5	4.2	7.1	10.3
Relative Device Switching Energy [12]	1.0	0.72	0.45	0.29	0.19	0.17	0.12	0.04	0.02	0.01

History of ERD Roadmap Development

- **Began in 2000**
  - Initial list of candidates – 3 pages
- **Challenge:**
  - Huge constellation of ideas, concept, prototypes etc
  - Different maturity levels
  - Different application time scales
  - Different operating principles
  - Little quantization initially
- **Approach:**
  - Taxonomy building
  - Quantitative assessments
  - Progress monitoring

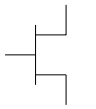
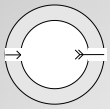
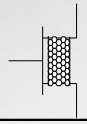
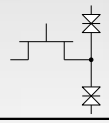
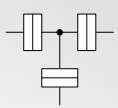
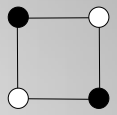
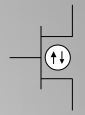
Forms the basis for comprehensive selection and evaluation

2001 Emerging Research Logic Devices

Device	 Resonant Tunneling Diode - FET	 Single Electron Transistor	Rapid Single Quantum Flux Logic	 Quantum Cellular Automata	 Ballistic Devices	 Nanotube Devices	 Molecular Devices
Maturity	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Concept	Concept
Types	3-terminal	Silicon, Metal islands	High Tc Low Tc Superconductors	Electronic QCA Magnetic QCA	3-terminal	FET	
Advantages	Density, Performance, RF	Density, Power, Function	High Speed (GHz), Potentially robust	High functional density, no interconnects	THz operation, might allow analog and digital operation	Density, Power	Identity of individual switches (e.g. size, properties) on sub-nm level. Potential solution to interconnect problem
Challenges	matching of device properties across wafer	New device & system. Room temp operation questionable. Noise (offset charge), lack of drive current	Low temperatures required (even with high Tc), fabrication of complex, dense circuitry	Limited fan out, low temperature, architecture	Impedance matching, operation at room temperature	New device and system, difficult route for fabricating complex circuitry	Thermal and environmental stability; two terminal devices; need for new architectures

The time horizon for entries increases from left to right in this table

2003 Emerging Research Logic Devices

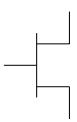
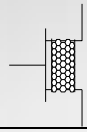
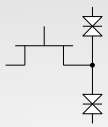
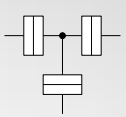
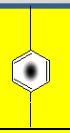
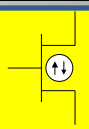
Device	 FET	 RSFQ	 1D structures	 Resonant Tunneling Devices	 SET	 Molecular	 QCA	 Spin transistor
Cell Size	100 nm	0.3 µm	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
Density (cm^{-2})	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
Switching Energy, J	2×10^{-18}	$>1.4\times10^{-17}$	2×10^{-18}	$>2\times10^{-18}$	$>1.5\times10^{-17}$	1.3×10^{-16}	$>1\times10^{-18}$	2×10^{-18}
Binary Throughput, GBit/ns/cm^2	86	0.4	86	86	10	N/A	0.06	86

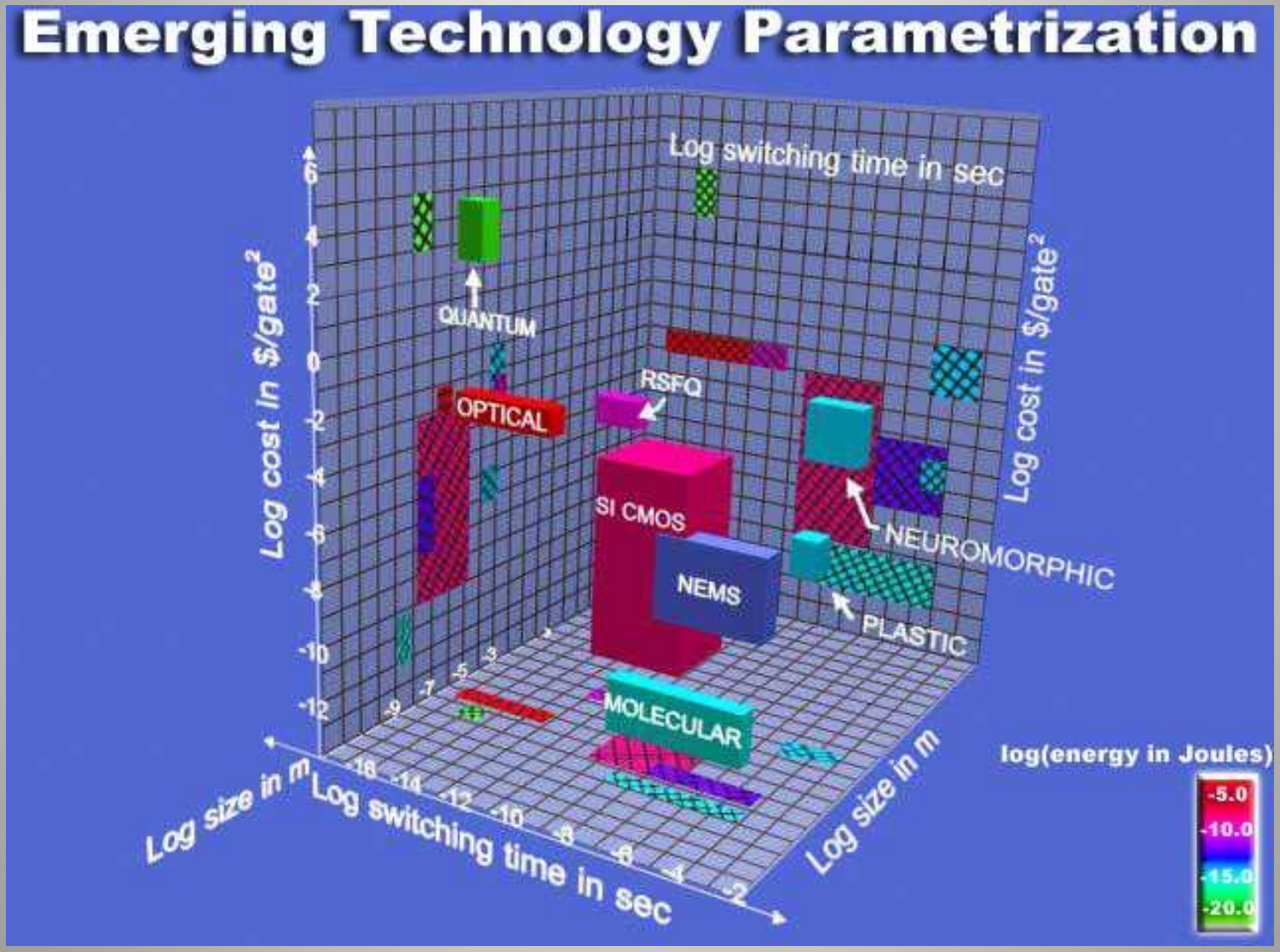
2005 Emerging Research Logic Devices

Min. required

Best projected

Demonstrated

Device								
		FET [B]	1D structures	Resonant Tunneling Devices	SET	Molecular	Ferromagnetic logic	Spin transistor
Types		Si CMOS	CNT FET NW FET NW hetero-structures Crossbar nanostructure	RTD-FET RTT	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin transistor
Supported Architectures		Conventional	Conventional and Cross-bar	Conventional and CNN	CNN	Cross-bar and QCA	CNN Reconfigure logic and QCA	Conventional
Cell Size (spatial pitch)	Projected	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 □m [D]	3μm [H]	~700 nm [M]	~2□m [R]	250 nm [V, W]	100 □m [X]
Density (device/cm^2)	Projected	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known
	Demonstrated	5.6 GHz	220 Hz [G]	10 GHz [Z]	1 MHz [F]	100 Hz [R]	30 Hz [V]	Not known
Switching Energy, J	Projected	3E-18	3E-18	>3E-18	1×10^{-18} [L] [$>1.5\times10^{-17}$] [O]	5E-17 [T]	~1E-17 [V]	3E-18
	Demonstrated	1E-16	1E-11 [G]	1E-13 [K]	8×10^{-17} [P] [$>1.3\times10^{-14}$] [O]	3E-7 [R]	6E-18 [W]	Not known
Binary Throughput, GBit/ns/cm^2	Projected	238	238 [C]	238 [C]	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	0.1	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	4.2 – 300 K	20 K [L]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	III-V Si-Ge	III-V Si	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides


Emerging Technology Parametrization
Log switching time in sec
Log cost in $/gate²
QUANTUM
OPTICAL
RSFQ
SI CMOS
NEMS
NEUROMORPHIC
PLASTIC
MOLECULAR
Log size in m
Log switching time in sec
Log cost in $/gate²
Log size in m
log(energy in Joules)
-5.0
-10.0
-15.0
-20.0

Bioelectronics Roadmap?

- Can we develop a process for a *Bioelectronics Roadmap*?
  - ITRS methodology might be helpful
- Procedure:
  - Selection
  - Categorization/Taxonomy
  - Assessment
    - **Need to be as quantitative as possible**

- Initial Selection/Categorization exercise
  - Based on the input from BERT participants

TARGETS

- Cancer detection/prevention
- Brain chronic degeneration detection/prevention
- Neural prosthetics, e.g .vision, hearing, etc.
- DNA sequencing

DEVICES

Lab-on-Chip
- Protein chips
- DNA chips

Implants
- Telemonitoring devices
- Nanodelivery devices
- Energy sources

ENVIRONMENT

In-vitro
In-vivo

Measurements

- Protein produced in cells
- Non-selective concentration measurements
- Single bio-molecule detection e.g. in Lab-on-Chip Environment
- Live or dead cells?
- Action potential in live cells

Technologies

- MEMS
- bioFET
- PD Arrays
- IC

Cross-cut Research

Selected Cross-Cut Research Needs

- Immune system reaction to bio-electronic implants
- Stimulated adhesion of cells to the sensing surface
- Mechanical stimulation/response of cells
- Bioelectromagnetics
- What else?

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