



2009 GRC ETAB Summer Study
La Quinta Golf Resort, CA
June 29-30, 2009

Session II: Systems, Software, and Applications Research for the Semiconductor Industry



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- David Seeger, SRC
 - Betsy Weitzman, FCRP
 - Shahrokh Daijavad, IBM
 - Steve Hillenius, SRC
 - David Yeh, SRC
 - Bill Joyner, SRC
 - Marie Burnham, Freescale Chair



- Opportunities and New Ideas from the NSF: Dr. Ty Znati, NSF
The NSF CISE Directorate, emphasis on CyberPhysical Systems
- The Big System: Dr. Shahrokh Daijavad, IBM
"Application and Network Optimized Next Generation System Research"
- Consumer: Dr. Pradeep Dubey, Intel
"Massive Data Computing in a Connected World"
- Industrial: Prof. Raj Rajkumar, CMU
Electronic Systems Research for Automotive
- Vision of the Future (Needs): Prof. Jan Rabaey, Berkeley
"The transformation of the semiconductor industry: from integrated platforms to distributed systems"



Objective of Session II



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- Analogous to scaling, our definition of the systems/applications research agenda may be critical to our economic growth and the appropriate growth of academic research.



The Challenge for Everyone



The Good News: You won't be bored. The presentations are very interesting and understandable.

- Each Presenter represents a very different
 - kind of computing
 - business model
 - wafer architecture
 - system integration

- What are the core issues for each presenter's vision?



What are Your Systems/Software/Applications Research Needs?



- Don't try too hard to be consortial
- Jot down your systems/software/application research needs now....
- Each speaker will present research directions, needs, topics
 - Prepare questions
 - What can you ask that better explains their ideas for you?
 - What can you ask that gets us beyond our narrow 'separate concerns'.
- Be prepared to submit the top 2-3 for your company (whether presented or not).
- Circulate highlights (with your comments) later to your companies



NSF CISE and CPS Programs



Dr. Znati received a Ph.D. degree in Computer Science from Michigan State University in 1988, and a M.S. degree in Computer Science from Purdue University, in 1984. He is a Professor in the Department of Computer Science, with a joint appointment in Telecommunications in the Department of Information Science, and a joint appointment in Computer Engineering at the School of Engineering. He currently serves as the Director of the Computer and Network Systems Division at the National Science Foundation. Dr. Znati also served as a Senior Program Director for networking research at the National Science Foundation. In this capacity, Dr. Znati led the Information Technology Research (ITR) Initiative, a cross-directorate research program, and served as the Chair of ITR Committee.

Dr. Znati's current research interests focus on the design and analysis of evolvable, secure and resilient network architectures and protocols for wired and wireless communication networks. He is a recipient of several research grants from government agencies and from industry. He is frequently invited to present keynotes in networking and distributed conferences both in the United States and abroad.

Dr. Znati served as the general chair of IEEE INFOCOM 2005, the general chair of SECON 2004, the first IEEE conference on Sensor and Ad Hoc Communications and Networks, the general chair of the Annual Simulation Symposium, and the general chair of the Communication Networks and Distributed Systems Modeling and Simulation Conference. He is a member of the Editorial Board of the International Journal of Parallel and Distributed Systems and Networks, the Pervasive and Mobile Computing Journal, the Journal on Wireless Communications and Mobile Computing, and Wireless Networks, the Journal of Mobile Communication, Computation and Information. He was also a member of the editorial board of the Journal on Ad-Hoc Networks, and a member of IEEE Transactions of Parallel and Distributed Systems.



Dr. Ty Znati



Automotive Electronics Systems of the Future



Raj Rajkumar (a.k.a. Ragunathan Rajkumar), Professor in the Department of Electrical and Computer Engineering at Carnegie Mellon University. He also holds a courtesy appointment in the Robotics Institute at Carnegie Mellon. In addition, he serves as Director, Real-Time and Multimedia Systems Lab; Co-Director, General Motors-Carnegie Mellon *Information Technology* Collaborative Research Lab and Co-Director, General Motors-Carnegie Mellon *Autonomous Driving* Collaborative Research Lab.



He was a Primary Co-Founder of TimeSys Corporation and has served as a research staff member at IBM T.J. Watson Research Labs. He is interested in embedded systems, real-time systems, wireless sensor networks, resource management, cybersecurity and physical security, cyber-physical systems, networking and QoS.

He is an ACM Distinguished Engineer, has won 5 Best Paper Awards, and has served as Vice-Chair, IEEE Technical Committee on Real-Time Systems

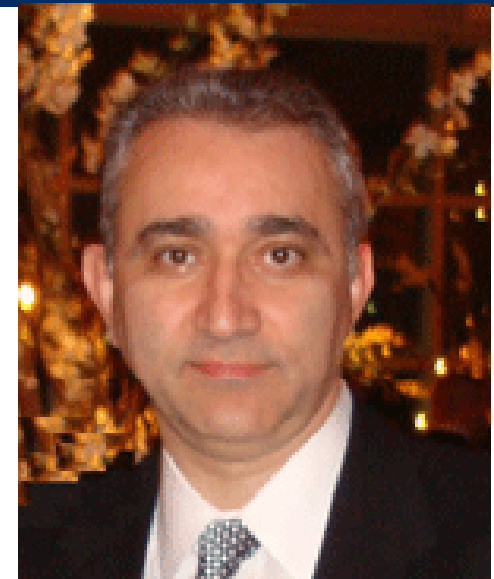
**Professor Raj
Rajkumar**



Application and Network Optimized next- Generation System Research at IBM



SHAHROKH DAIJAVAD is currently the Software Lead for IBM Next Generation Systems, and is responsible for setting directions and executing a number of cross-organizational software activities between System & Technology Group, Software Group and Research Division, in support of IBM's Next Generation Systems. Shahrokh got his Ph.D. in Electrical Engineering from McMaster University, Canada in 1986. After a year of Postdoctorate Fellowship at the University of California at Berkeley, he joined IBM T.J. Watson Research Center (Yorktown Heights and Hawthorne, NY) and worked there from 1987 to 2001, as a Research Staff Member (RSM) first and then as an RSM/Manager.



**Dr. Shahrokh
Daijavad**

From 2001 to 2003, he was the CTO of a Japanese Internet start-up company, CollaboTechnology. He returned to IBM at the end of 2003 and joined the Next Generation Systems group, again at the T.J. Watson Research Center. His role continues to be defining and executing multiple projects that take into account all layers of the software stack, including target applications, for an upcoming network-optimized processor and setting directions for hardware/software designs for IBM's systems that utilize this processor.



Massive Data Computing in a Connected World



PRADEEP DUBEY is a senior principal engineer and manager of Innovative Platform Architecture (IPA) in the Microprocessor Technology Lab, part of the Corporate Technology Group. His research focus is computer architectures to efficiently handle new application paradigms for the future computing environment. Dubey previously worked at IBM's T.J. Watson Research Center, and Broadcom Corporation. He was one of the principal architects of the AltiVec* multimedia extension to Power PC* architecture. He also worked on the design, architecture, and performance issues of various microprocessors, including Intel® i386TM, i486TM, and Pentium® processors.

He holds over 25 patents and has published extensively. Dr. Dubey received a BS in electronics and communication engineering from Birla Institute of Technology, India, an MSEE from the University of Massachusetts at Amherst, and a PhD in electrical engineering from Purdue University. He is a Fellow of IEEE.



**Dr. Pradeep
Dubey**



The transformation of the Semiconductor Industry: From Integrated Platforms to Distributed Systems



- JAN RABAEY received the EE and Ph.D degrees in applied sciences from the Katholieke Universiteit Leuven, Belgium, respectively in 1978 and 1983. From 1983 till 1985, he was connected to the University of California, Berkeley as a Visiting Research Engineer. From 1985 till 1987, he was a research manager at IMEC, Belgium, and in 1987, he joined the faculty of the Electrical Engineering and Computer Science department of the University of California, Berkeley, where he is now holds the Donald O. Pederson Distinguished Professorship. He has been a visiting professor at the University of Pavia (Italy), Waseda University (Japan), Technical University Delft (Netherlands), Victoria Technical University and the University of New South Wales (Australia). He was the Associate Chair (EE) of the EECS Dept. at Berkeley from 1999 till 2002, and is currently the Scientific co-director of the Berkeley Wireless Research Center (BWRC, as well as the director of the GigaScale Systems Research Center (GSRC).
- Jan authored or co-authored a wide range of papers in the area of signal processing and design automation. He received numerous scientific awards, including the 1985 IEEE Transactions on Computer Aided Design Best Paper Award (Circuits and Systems Society), the 1989 Presidential Young Investigator award, and the 1994 Signal Processing Society Senior Award, and the 2002 ISSCC Jack Raper Award. In 1995, he became an IEEE Fellow He is past chair of the VLSI Signal Processing Technical Committee of the Signal Processing Society and chaired the executive committee of the Design Automation Conference. He is serving on the Technical Advisory Board of a wide range of companies.
- His current research interests include the conception and implementation of next-generation integrated wireless systems. This includes the analysis and optimization of communication algorithms and networking protocols, the study of low-energy implementation architectures and circuits, and the supporting design automation environments.



**Professor Jan
Rabaey**



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- Backup



Types of Computing:

Current nomenclature, always changing



- Parallel** : There are several different forms of parallel computing: bit-level, instruction level, data, and task parallelism. Parallelism has been historically employed high-performance computing. Calculations are carried out simultaneously operating on the principle that large problems can be divided into smaller ones, which are then solved concurrently ("in parallel").
- **Heterogeneous** computing uses a variety of different types of computational units: general-purpose processor (GPP), special-purpose processor (i.e. DSP or GPU), a co-processor, or custom acceleration logic (ASIC or FPGA). In general a heterogeneous computing platform consists of processors with **different instruction set architectures** (ISAs). The demand for increased heterogeneity is partially due to the need for highly-reactive systems that interact with other environments (audio/video systems, control systems, networked applications, etc.)
 - **Network** computing refers to **computers working together over a network** as opposed to stand alone computers like laptops and home computers. Cloud computing is an alternate term for network computing. **Cloud** computing is style of computing in which dynamically scalable and often virtualized resources are provided as a service over the Internet. Users need not have knowledge of, expertise in, or control over the technology infrastructure in the "cloud" that supports them. The concept generally incorporates combinations of the following in various business models:
 - ◆ infrastructure as a service
 - ◆ platform as a service
 - ◆ software as a service
 - ◆
 - **Hybrid** computing is the strategy of deploying multiple types of processing elements within a single workflow, and allowing each to perform the tasks to which it is best suited. Conceivably combining heterogeneous, network, and parallel computing, other differences may be seen in a staged workflow, a multi-level system architecture, scalable subsystems, and other complexities required to solve the world's largest problems.
 - **Distributed** computing deals with hardware and software systems containing more than one processing element or storage element, concurrent processes, and/or multiple programs, running under a loosely or tightly controlled regime. In distributed computing a program is split up into parts that run simultaneously on multiple computers communicating over a network. Parallel computing is most commonly used to describe program parts running simultaneously on multiple processors in the same computer while distributed programs often must deal with heterogeneous environments, network links of varying latencies, and unpredictable failures in the network or the computers. Concurrent programming is tightly related.

- Wikipedia and Shahrokh Daijavad



- System functionality is enabled by ever more tightly coupled **hardware and software** that is **invisible** to the end user.
- Most embedded systems increasingly interact with the “real” **analog world**, bringing uncertainty, ambiguity, drift, hysteresis, stuck values, and nonlinear responses.
- Applications demand **robust, resilient, fault tolerant** operation without user intervention, including ability to autonomously detect, compensate, avoid, or correct anomalous conditions.
- System and application development requires extensive **cross-disciplinary** skill and collaboration including hardware/software co-design.
- Software development for chips require highly capable **compilers, assemblers and debuggers**.
- **User interfaces** range from none to complex GUI to web interface

We have entered the world of top down design



Precompetitive Topics that may span across application spaces



- How does one partition a workload so that optimal performance can be met across different processor and controller architectures?
- Background research for standard xxxxxx that is of interest to GRC member companies.
- System level reliability, on-line test and repair.
- Resilient systems including processor architectures, circuits, software ...
- Multi-layer real time control over distributed/networked architectures
- Cross-disciplinary linkages between semiconductor systems research and leading programs in relevant application domains (Energy, healthcare, transportation, networking and communications, industrial control, consumer electronics...)
- QoS-aware system design
- System design, exploration and optimization tools, possibly tailored to specific application domain areas