Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

Focus Center RESEARCH PROGRAM

FCRP Program Directions & Promising Outputs

2009 GRC ETAB Summer Study

June 29, 2009

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Outline

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- FCRP Re-competition
  - Timeline / Status
  - Consideration of Potential 6th Focus Center
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Current SRC Focus Centers …

Sponsors

SIA Semiconductor Industry Association

AMD
Freescale
IBM
Intel
MICRON
Texas Instr.
Xilinx
GlobalFoundries

semi

Applied Materials
Novellus
Cadence

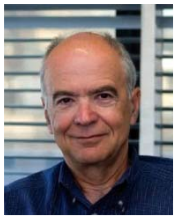
Dep't of Defense

DARPA

Gigascale Systems Research Center [19 Universities]
Director: Prof. Jan Rabaey (UC-Berkeley). Design, verification and test of embedded systems-on-a-chip; concurrent systems; complex heterogeneous platforms; alternative computation.

Center for Circuit & Systems Solutions [19 Universities]
Director: Prof. Rob Rutenbar (CMU). Circuit techniques and system concepts for end-of-roadmap and post-CMOS devices; analog circuits and interfaces.

Interconnect Focus Center [12 Universities]
Director: Prof. Paul Kohl (Georgia Tech). Nanoscale electrical & optical interconnects for future gigascale silicon systems; novel thermal and power management solutions; modeling/analysis methods.



Materials, Structures and Devices [15 Universities]
Director: Prof. Dimitri Antoniadis (MIT). FETs of novel materials; nanotube & molecular devices: hybrid devices for ultra-low power; theory, modeling and simulation to support experiments.

Functional Engineered Nano-Architectonics [17 Univ.]
Director: Prof. Kang Wang (UCLA). Novel materials, structures & processes for nanoscale devices.

2009 Science Advisory Board Membership

Organization	Member	Alternate
AMD	Jim Farrell	
Applied Materials	David Kyser	
Cadence	Andreas Kuehlmann	
DARPA	Jeff Rogers	Cindy Hanson
Freescale	Kevin Kemp	
GLOBALFOUNDRIES	Zoran Krivokapic	Ming-Ren Lin
IBM	Ghavam Shahidi	Michael Rosenfield
Intel	Paolo Gargini	George Bourianoff
MICRON	Scott DeBoer	Chandra Mouli
Novellus	John Kelly	Andy Antonelli
Texas Instr.	Ajith Amerasekera	Allen Bowling
Xilinx	Steve Trimberger	

FCRP Re-competition Status

- FCRP Research Announcement 2009-S200902
  - Re-competition solicitation posted on March 23, 2009
  - 10 proposals received May 29, 2009
- Research Topics (Centers)
  - Nanoelectronic Materials and Processes
  - Structures and Devices
  - Connectivity
  - Circuits & Modules
  - Information Systems Platform Design
  - Proposed New Center: Multi-Scale Systems (expected to attract new defense industry and systems companies)
- Proposal Review Panel – June 23 & 24, 2009
  - Proposal evaluation, Selectability recommendations

Consideration of Potential 6th Focus Center

- DARPA proposed creation of higher-level complex systems research center:

  "The mission of the Multi-Scale Systems Center is to discover and explore architectures, design tools, modeling and simulation tools, and analysis tools and techniques that enable the strategic implementation of complex hybrid systems for impact on technologies in real-world systems. This includes concurrent hardware and software development to optimize overall system performance."

  - Proposed center seen as vital to defense industry recruitment into FCRP
  - Several current sponsors also see value in creation of such a center
- Enabling factors:
  - Incremental funding (defense industries, networking companies, e.g., CISCO, etc.)
  - Clear interest to current sponsors in terms of identified research topics
- Unknowns:
  - Number of new FCRP Participation Agreements executed prior to 7/09 Governing Council meeting (for review/approval of SAB-recommended Focus Centers)

FCRP Re-Competition Schedule

Plan for Executing FCRP Re-Competition for Phase V

Key Activity	Target Date
Release FCRP RA (Fed Biz Ops, ECEDHA, etc) (MARCO)	3/23/2009
Finalize Proposal Review Panel Plans, Participation (MARCO, with SAB)	4/20/2009
Center Proposals due to MARCO	5/29/2009
Upload Proposals to FCRP secure website for Review Panel Members (MARCO)	5/30/2009
-> Submit completed Proposal Evaluation Forms to MARCO (SAB)	6/19/2009
First Proposal Review Panel (MARCO/SAB)	6/23-24/2009
Upload Refined Proposals to FCRP secure website for Review Panel (MARCO)	7/13/2009
Second Proposal Review Panel for final recommendations to GC (MARCO/SAB)	by 7/23/2009
FCRP Governing Council review/approve SAB Center recommendations	by 7/31/2009
Notify selected Proposers, initiate contract negotiations (MARCO)	8/03/2009
Execute Contracts to new Centers to Launch FCRP Phase V (MARCO)	**by 10/31/2009**

Examples of Recent Technical Highlights

- GSRC
  - **Robust Thread-Level Auto Parallelization**: August (Princeton) - *Concurrent Systems Theme* – successfully executed automatically parallelized code on 8-core X86 hardware.
  - **Ultra-Low Cost Checking Hardware**: Iyer (Illinois) – *Resilient Systems Theme* – showed promising results for novel "Critical Value Recomputation" approach, only recomputing such values for very low cost and high fault coverage.
  - **Novel Distributed Routing Algorithm for NOCs**: Bertacco, Blaauw, Sylvester (Michigan) – *Resilient Systems Theme* – developed design that allows network to reconfigure around faulty components, finding these networks to still be 99.99% reliable when 10% of interconnect links have failed.
- C2S2
  - **Design of High Performance Analog/Digital Interfaces in Deep Sub-100nm CMOS**: Carley (CMU) – *Analog Circuits and Interfaces Theme* – in joint team with Intel, successfully demonstrated first CMOS design (in foundry 45nm digital CMOS process) to achieve 7-bit precision and 1.25GHz input bandwidth (i.e., 2.5 Gsamples/second).
  - **Circuit/Architecture Co-Optimization Framework**: Patel (UIUC), Horowitz (Stanford) – *Microarchitecture Design Theme* – reveals cost-performance tradeoffs in 2000-core processor for several different core designs
  - **Reconfigurable Circuits for Memory Intensive Self-Configuring ICs**: Pileggi, Fedder, Schlesinger, Bain (CMU) – *Emerging Circuits and Applications Theme* – have shown first-ever reconfigurable RF application of Phase-Change materials, building essential components. Working with FENA, a novel process was developed to add P-C vias to CMOS chip, successfully demonstrating reversible via switching. - - Opens the way for dramatic cost/configurability improvements for wireless tasks.

Examples of Recent Technical Highlights

- IFC
  - **CNT Nano-relay Circuits**: Chandrakasan, Baldo (MIT) – *Circuit & System Design and Modeling Theme* - demonstrated a multiwall CNT nanorelay with zero leakage and very favorable scaling behavior. A CMOS test chip was designed to test three nano-relay applications: power gating, reconfigurable interconnect, nonvolatile SRAM.
  - **Graphene Layers as Interconnects and High-Heat-Flux Channels**: Balandin (UCR) – *Thermal & Power Management Theme* – demonstrated that graphene interconnects are promising from thermal management point of view, and that few-layer graphene works better than single-layer graphene as an interconnect material.
  - **CMOS Detector with Nanometallic Enhancement**: Brongersma (Stanford) – *Optical Interconnects Theme* – demonstrated first successful integration of a nanometallic detector with commercial CMOS for enhanced photodetection, achieving 3x greater photocurrent per unit detector area than conventional detector.
- MSD
  - **Si/Ge/Si Heterostructure on Insulator: Planar and Non-planar MOSFETs**: Hoyt (MIT) – *CMOS Extension: Si-Ge Channel Materials and Devices Theme* – fabricated and characterized performance of first uniaxial tensile-strained Si nanowire gate-all-around (GAA) n-MOSFETs, with nanowire dimensions down to 8 nm.
  - **Carbon Nanotube Synthesis, Assembly, Metallicity Control and Scalable Devices**: Dai (Stanford) – *CMOS Extension / CMOS Plus Theme* – achieved for the first time SWNT FETs with single chirality SWNTs. The FETs, comprised of separated SWNTs in parallel, gave I_{on}/I_{off} ratio up to 10^6, owing to single chirality enriched tubes.

Examples of Recent Technical Highlights

- MSD (cont'd)
  - **Simulation of Electronic Transport in CMOS Extensions: Si-Ge and III-V Channels and Non-Bulk Structures**: Fischetti (UMass) – *Theory, Modeling and Simulation Theme* - calculated hole mobility in strained GaSb and InSb inversion layers. Theoretical results show extremely high mobilities. This is important due to critical need for a high-mobility p-MOSFET to complement potential III-V n-MOSFETs.

- FENA
  - **Chemical Routes to Single Graphene Sheets for Use in Nanoelectronic Devices Polyaniline Metal Nanocomposites for Nonvolatile Memory Devices**: Kaner (UCLA) – *Novel Materials from Atomic and Molecular Levels Theme* – utilizing a PDMS stamp and manipulation of surface energies, successfully transferred spin-coated materials from one substrate to another. The method is capable of transferring relatively sharp features to precise locations, as confirmed by Raman mapping.
  - **Nanoscale Self-Assembled Patterns Generated by Electric Lithography**: Cheng (UCLA) – *Synthesis and Manufacturing Methods for Nanoscale Materials & Structures Theme* - developed process for DNA-assisted self-assembly of nanowires on a nano template. Plan to use this technique to fabricate nanoscale crossbar circuits.

Recent FCRP e-Workshops

Between January 1 & May 31, 2009, **23** eWorkshops held

Center	Title	Date
GSRC	Exploring Network Properties of Oscillators	1/15/2009
IFC	Single and Few-Layer Graphene for Thermal Management and Interconnect Applications	1/29/2009
Ifc	Field Solver Technologies for Variation Aware Interconnect Extraction	2/12/2009
C2S2	A "Digital-like" RF Beamformer	2/19/2009
MSD	Synthesis, Assembly, Doping, and Electron Transport Properties of High Mobility III-V Nanowires	2/19/2009
GSRC	Stochastic Computation	2/24/2009
IFC	Heteroepitaxial Growth of Ge on Si and Applications to Optical DFetectors and MOSFETs for 3D-ICs.	2/26/2009
MSD	Band-to-Band Transistors: Scaling and Circuit Issues	2/26/2009
MSD	Direct deposition of SWNTs and Raman spectroscopy characterization	3/5/2009
IFC	Highly Digital ADCs and Ultra-Wideband RF Circuits for Wireless Applications	3/12/2009
MSD	Development of InAs(x)Sb(1-x) Channel FET	3/19/2009
IFC	Thermal Transport and Thermoelectric Energy Conversion Across Nanoscale Interfaces	3/26/2009
MSD	Strained QW Channels with High-K Gate Oxide for InGaAs CMOS	4/2/2009
IFC	Resistivity and Breakdown Current Density of Graphene Nanoribbon Interconnects	4/9/2009
MSD	Compact Modeling of Layout-Dependent Stress Effect in Scaled CMOS Design	4/9/2009
MSD	III-V's: From THz HEMT to CMOS	4/16/2009
IFC	CNT and Graphene as Reconfigurable Interconnects	4/23/2009
MSD	Passivation Layers for InGaAs, InAs, Ge Prior to Oxide Deposition	4/23/2009
MSD	Nano-Electro-Mechanical (NEM) Relay Technology for Ultra-Low-Power Digital Integrated Circuits	4/30/2009
IFC	Device Requirements for Optical Interconnects to Chips - Energies and Densities to Meet the Roadmap	5/14/2009
MSD	Molecular Floating Gate Memories	5/14/2009
FENA	Technology and Devices for Nanoscale Application Specific Integrated Circuits (NASIC)	5/21/2009
IFC	Quantum Molecular Conductors as Ultra-High-Performance Nanoscale Interconnects: Fabrication Concepts & Inte	5/28/2009

Soon phasing over to WEBEX along with GRC

Summary

- FCRP re-competition fully underway: Exciting time, with opportunity to strengthen the Program and re-focus each research portfolio
- Outstanding response to Call for Center Proposals
- Excellent outlook for securing defense industry sponsorship
  - Potential for FCRP growth to $50M/yr
- Current Centers continuing to drive 3rd (current) year of dynamic research agenda for Phase IV
  - Highly productive, with outstanding collaborative research efforts
- FCRP Sponsors actively engaged in re-competition process via SAB, Governing Council

Thank You

Consideration of Potential 6th Focus Center

Research Topics Identified for Proposed Center:

- Techniques for global heterogeneous system design and optimization, including
  - analog systems
  - heterogeneous communication fabrics
  - high-level modeling
  - communications systems
  - ubiquitous sensor networks
- Unified, high-level system architectures that efficiently map the complex system workflows, including overall system management, security, and reliability to quickly enable future applications
- Techniques and architectures that enable complex hybrid systems from individually optimized subsystems, e.g., coupling a general-purpose subsystem with a stream-computing subsystem and a computationally intensive subsystem
- Developing computationally intensive hybrid systems, including reconfigurable multi-core and heterogeneous multi-core hardware platforms, architectures, and programming models, tools and techniques
- Developing built-in self-diagnosis and self-tuning, compensation and recovery schemes for heterogeneous and hybrid component systems and subsystems, including digital, high-speed IO, RF, MEMS, optical, and nano
- Solutions for the thermal and power management issues for future complex systems platform designs, including the integration of components such as power management systems, energy harvesting and power electronics for applications like smart grid. This Center should address power management at the full system level, in contrast to the device level cited in the Connectivity Center
- Modeling and simulation of complex hybrid systems and their component subsystems
- Diagnostics and prognostics; decision support systems ...