Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

nanoelectronics RESEARCH INITIATIVE

NRI Program Directions and Promising Outputs

ETAB Summer Study

Jeff Welser
June, 2009

NRI Research Centers

- Leveraging industry, university, and both state & fed government funds, and driving university nanoelectronics infrastructure

WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Iowa, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics Theme 4: Spin Metrology	Task I: Novel state-variable devices Task II: Fabrication & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap Task VI: Metrology	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Nanoscale thermal management Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Theme 1: Graphene device: Thermal, Tunnel, and Spin Theme 2: Interband Tunnel Devices Theme 3: Non-equilibrium Systems Model / Meas. Theme 4: Nanoarchitecture

NSF-NRI Projects – 2009 Additions

Co-funding 18 Projects at 15 NSF Centers

Caltech MRSEC	*2008: Graphene Atomic Switches for Ultracompact Logic Devices and NV Memory*
Columbia NSEC	*2008: Novel Device Arch. based on Quantum Transport Phenomena in Graphene*
Cornell NSEC	*2007: Controlled Orbital Hybridization in the CNT Quantum-Modulated Transistor*
Harvard NSEC	*2008: Tunable Ultra-fast Conductance Switching through External Fields*
Purdue NCN	*2007: Exploratory Theory, Modeling, and Simulation for the NRI* *2008: Experimental Realization of Low-power Transistors with Negative Capacitors* *2009: Exploration of Novel All-Spin Logic (ASPL) for Device-Circuit-Architecture*
Stanford NSEC (UI-UC)	*2008: Ultra-Low Power Pseudospintronic Switching in Bilayer Graphene at Rm T*
U. Maryland MRSEC	*2007: Pseudospintronics (UT-Austin)* *2008: Controlling the Electronic Properties of Graphene*
U. Nebraska MRSEC	*2007: Multiferroic Interfaces: New Paradigms for Functional Switching*
UVA MRSEC (Notre Dame, UCSB)	*2007: Coherent Spin Dynamics in Single Ion-doped Semiconductors: Towards a Coherent or Quantum Spin Switch*
Yale MRSEC	*2007: Design and Fab of Magnetic-based Devices with Complex Oxide Materials*
UC-Berkeley NSEC	*2009: Spin-Oscillators for Non-Charge Based Ultra Low Power Logic and Comm.*
MIT MRSEC (UVA)	*2009: Reconfigurable Array Magnetic Automata (RAMA)*
Northwestern MRSEC	*2009: Generating, Probing, and Manipulating Excitons in Carbon Nanomaterials*
Brown MRSEC	*2009: Direct-Write Synthesis of Graphene Devices*
Univ. of Alabama MRSEC	*2009: Spintronic Logic Devices*

NRI Research Vision

- NRI: A *Goal-oriented*, *Basic-science* Research Program

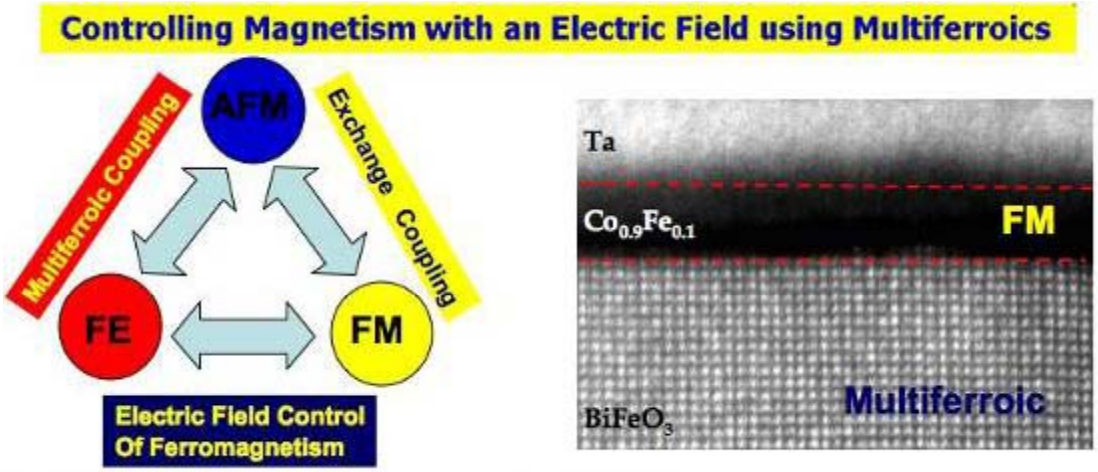
- Focus science work in all centers around specific device ideas
  - **WIN**: Continues spin focus, with particular multi-PI projects on spin-wave devices and multi-ferroics
  - **INDEX**: Created 4 cross-university Centers of Competency and Innovation (CCIs) around device areas:
    - Excitronic, QD Spin, Magnetic, and Graphene Devices
  - **SWAN**: Expanded focus on Graphene, from theory to devices to materials fabrication, including a new pseudospintronic device concept. Expanded metrology program, directly linked to the device work
  - **MIND**: Focus on tunneling and thermal transport for creating non-equilibrium architectures. Also leading cross-center device/architecture benchmarking efforts.

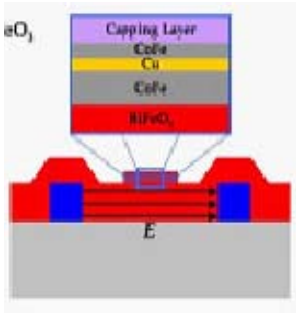
- Comment from industry sponsor at 2008 reviews:
  - "The NRI experiment is working. For understanding graphene, for example, the NRI team is probably one of the best. We learned more about graphene for applications in the last 2 years than we would normally learn in 5 or more years due to NRI focus on science for devices."

Multiferroic Materials

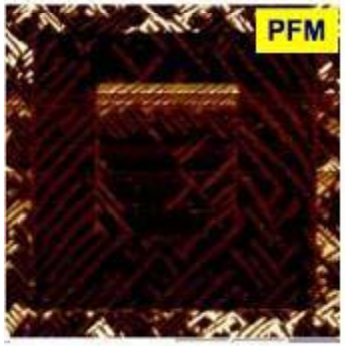
- Achievement: Demonstrated control of ferromagnetism with an electric field applied to a multiferroic.
- Importance: First step in device development so that control of correlated properties is possible via a simple electric field.

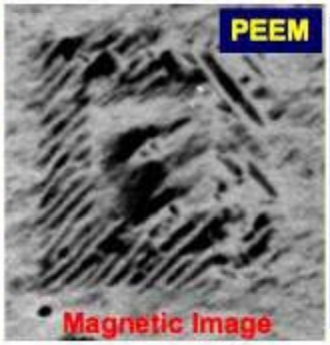
R. Ramesh (UC Berkeley)
J. Orenstein (UC Berkeley)





Next: Electric Field control of spin waves (linked with UCLA and UCSB efforts)

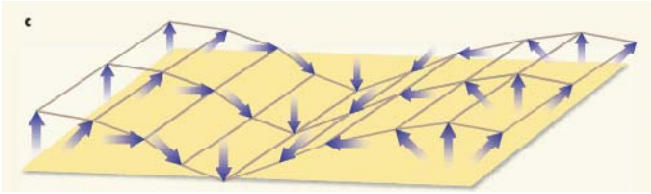




- AFM-FM coupling through exchange coupling
- AFM-FE coupling through Multiferroicity
- First evidence for electric field control of ferromagnetism

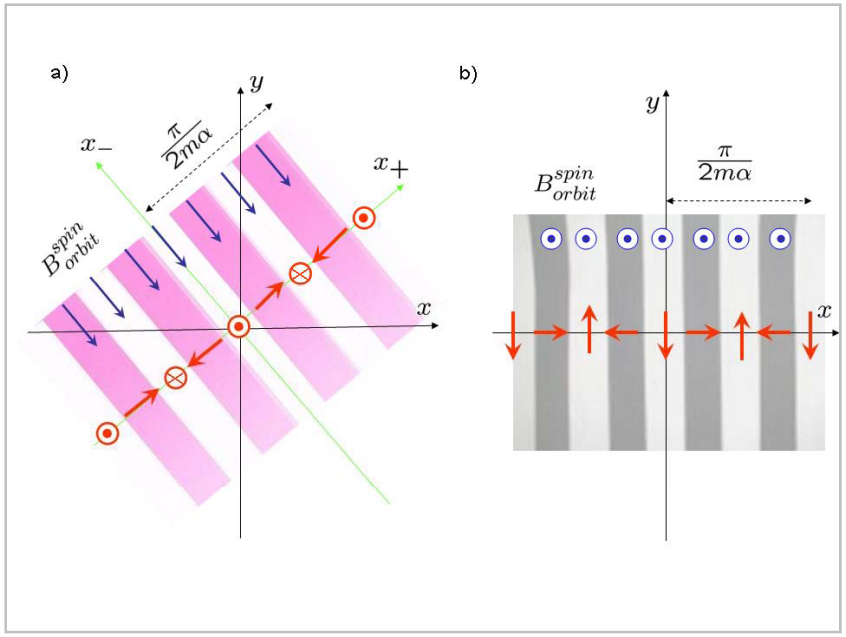
Increasing spin lifetime

- A new spin rotation symmetry is discovered. The symmetry renders the spin lifetime infinite at a “magic” wavevector - Persistent Spin Helix (PSH).
- Importance: PSH extends spin lifetime as the mechanism does not depend on Spin-Orbit coupling.



- **Observed persistent spin pattern with period determined by spin-orbit interaction**
- **Tunable suppression of spin relaxation**
  ➔ 2 orders of magnitude observed

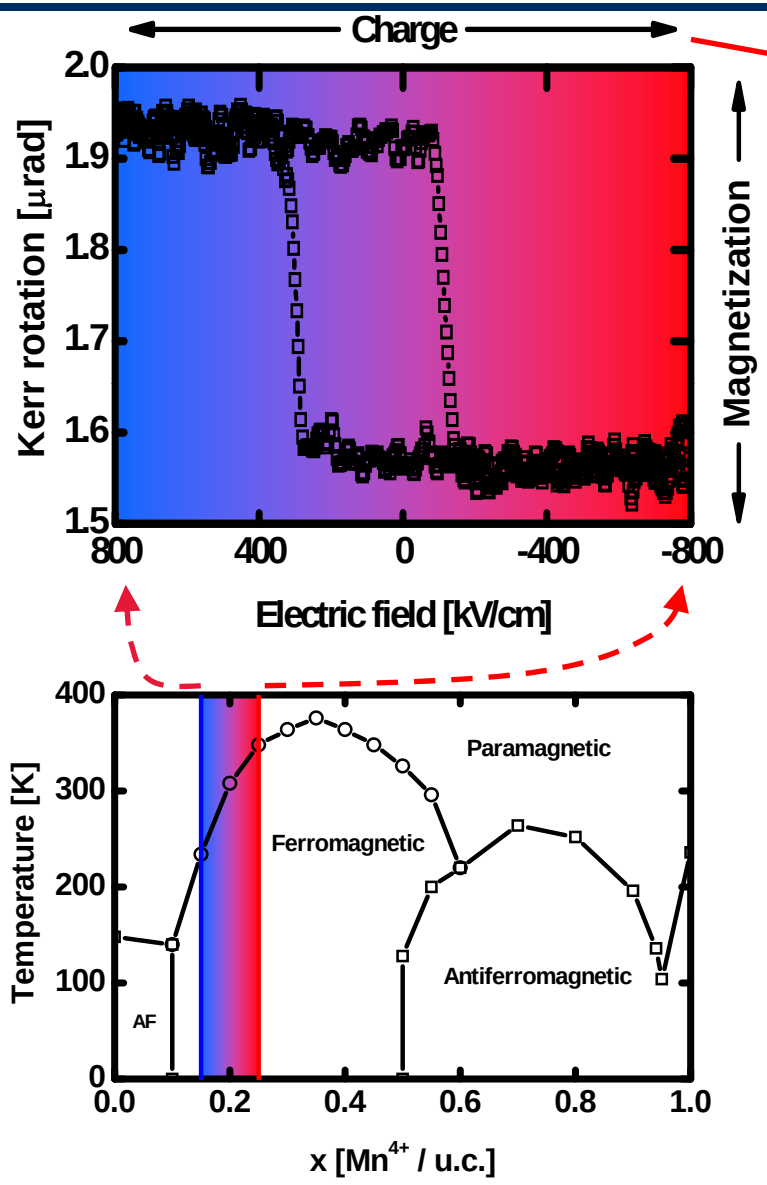
SC Zhang (Stanford)
J. Orenstein (UC Berkeley)
David Awschalom (UCSB)



a) PSH for the HReD model. The spin orbit magnetic field is in-plane (blue), whereas the spin helix for the choice of the relative signs is in the *x; z* plane.
b) The spin-orbit magnetic field *B* spin orbit, in blue, is out-of-plane, whereas the spin helix, in red, is in-plane.

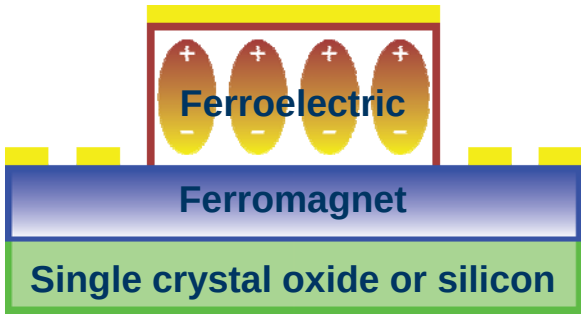
Magnetoelectric Coupling in Multiferroics

C. Ahn, Yale



Coupling between M and E

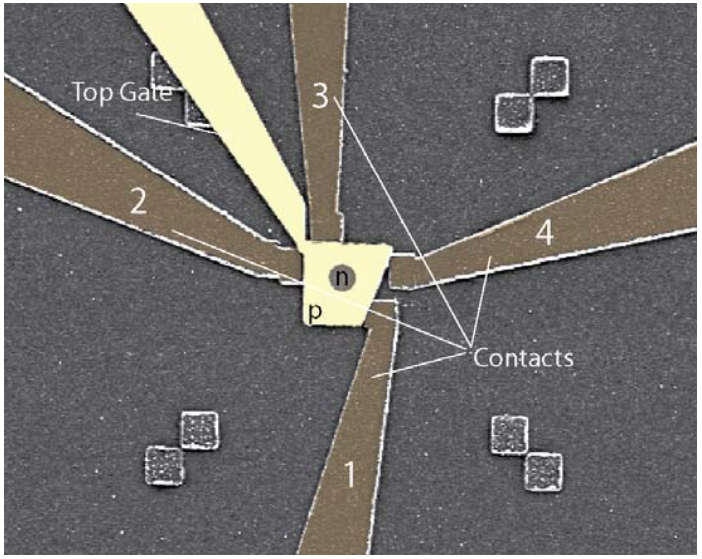
- **New type of charge-mediated magnetoelectric coupling**
  - Transparent physical mechanism
- **Novel electric field control of spin**
  - Nonvolatile, low power operation
  - Room temperature operation through new materials
- **Incorporate into realistic spin device architecture**
  - Integration with silicon platform

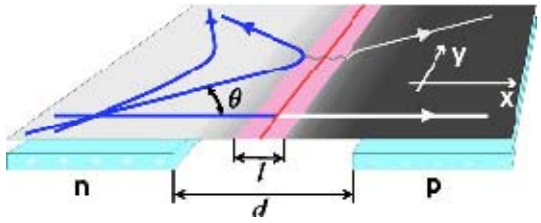


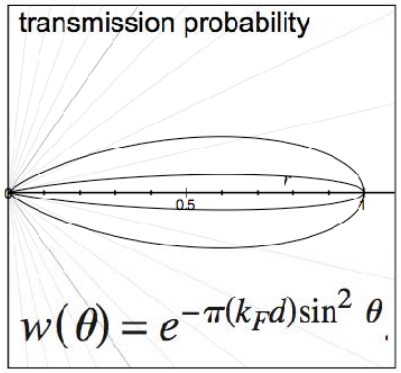
Graphene Progress

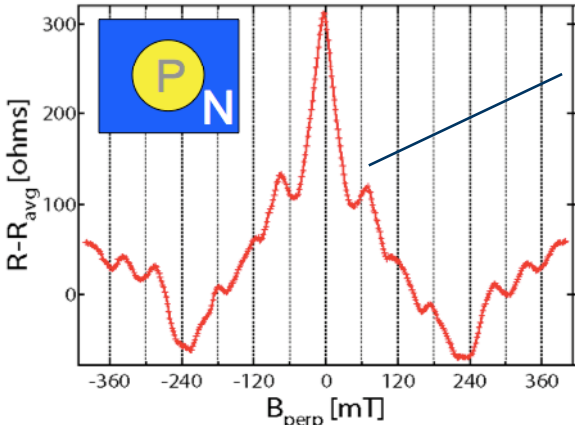
C. Marcus, Harvard

- **The graphene p-n interface acts like a fiber optic: small angles are reflected, large angles are transmitted**
  - **Demonstrated confinement in a p-n region**
- **Potential for Veselago Lens devices**
- **Also developed improved ALD oxide with less mobility impact**



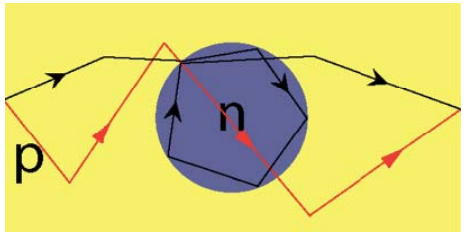


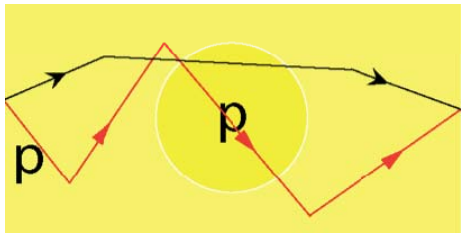




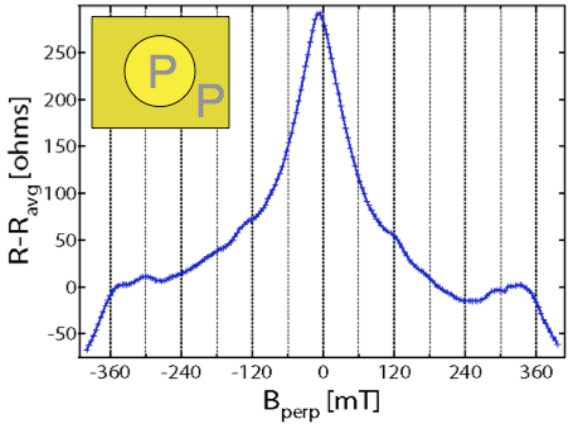
Aharonov-Bohm interference shows confinement

Confined





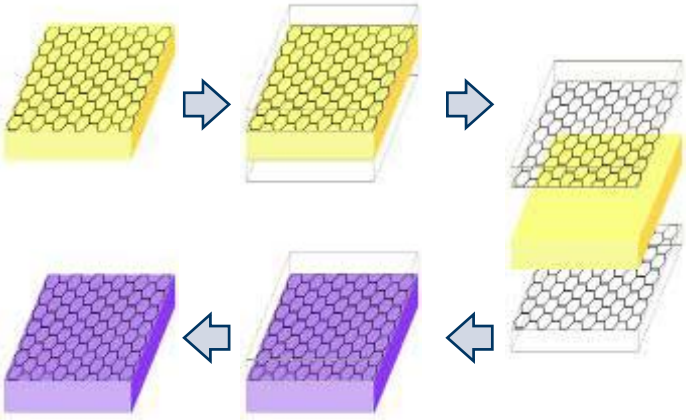
Unconfined

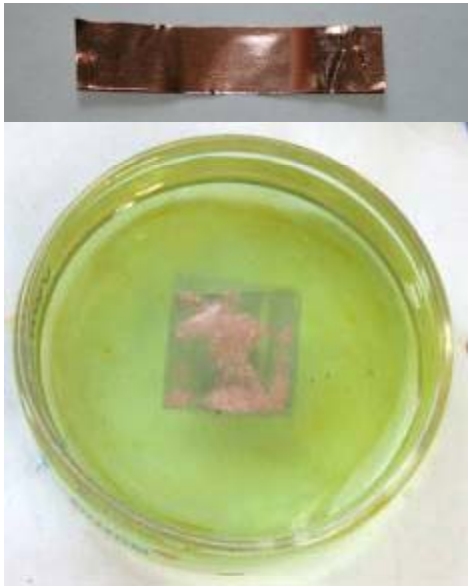


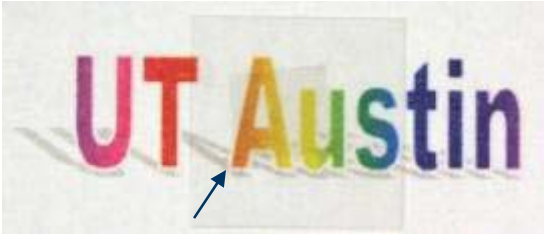
Graphene CVD Growth on Cu Foil

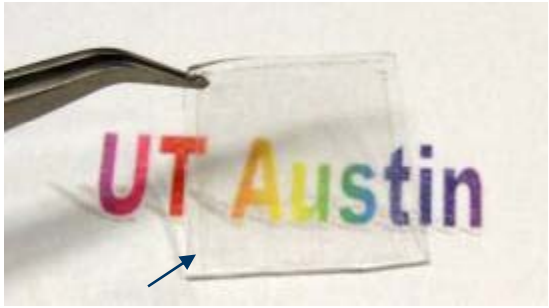
R. Ruoff, UT-Austin

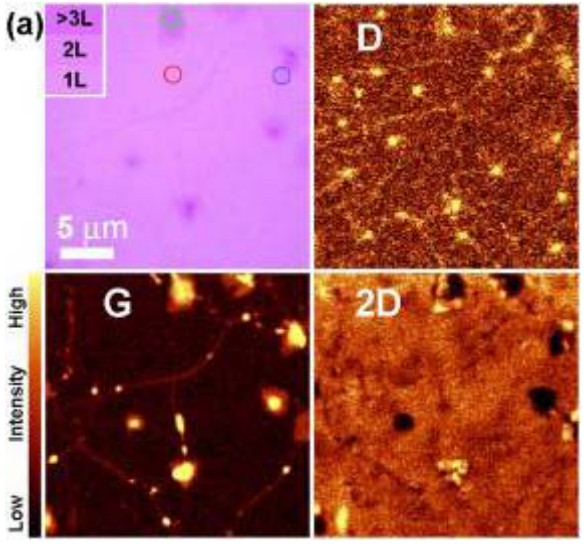
Transfer

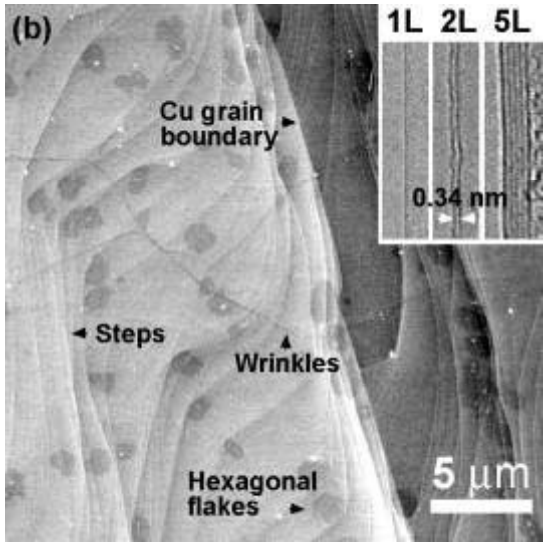


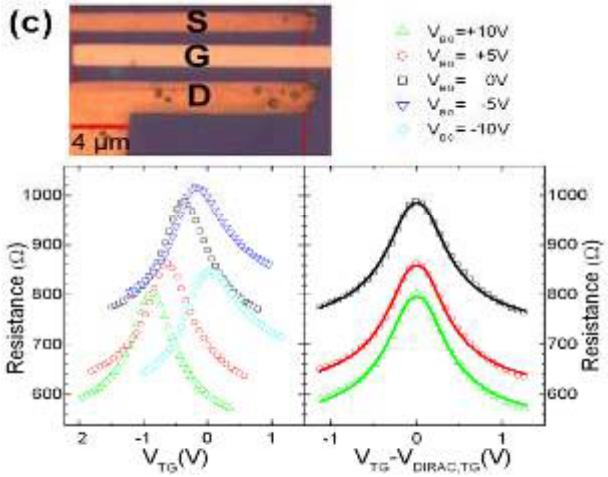








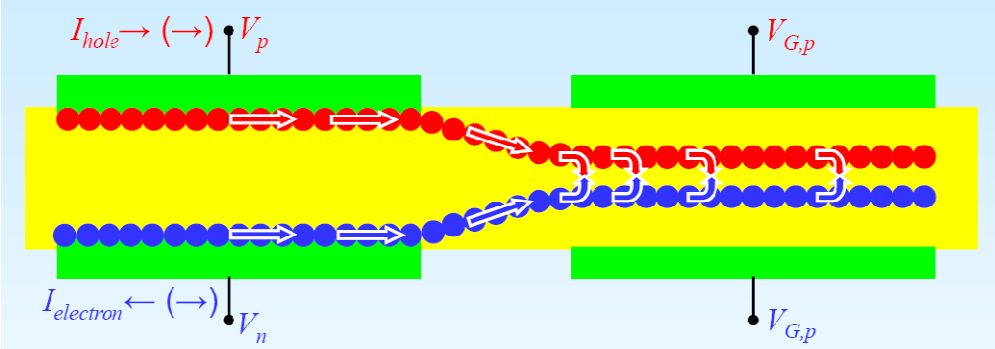


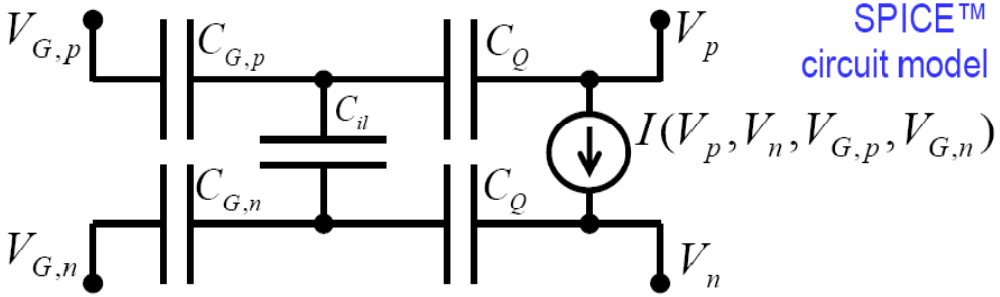


carrier mobility ~4050 $cm^2V^{-1}s^{-1}$, residual carrier concentration at the Dirac point $n_0 = 3.2 \times 10^{11}$ cm^{-2}

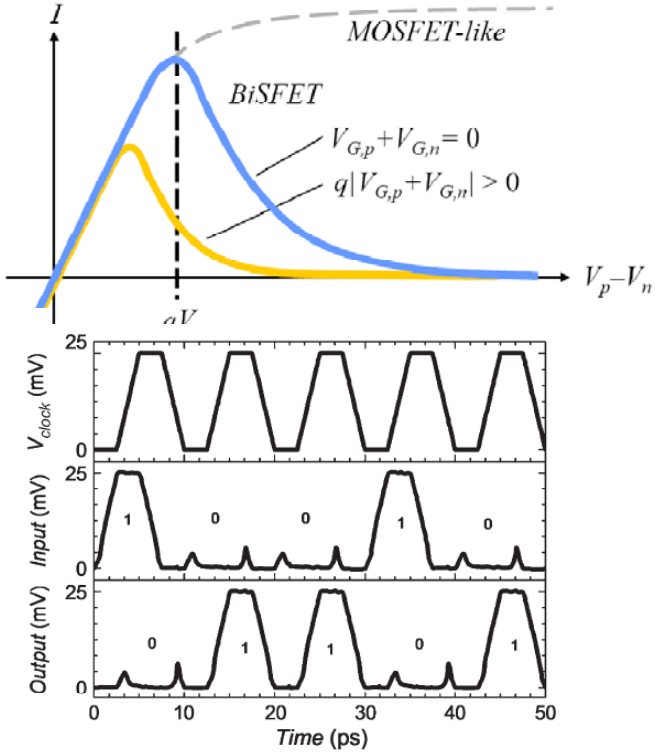
Bi-layer pseudoSpin Field Effect Transistor (BiSFET)

- Utilized new theoretical concept of room temperature electron-hole condensates in bi-layer graphene to propose a novel device
- Simulated devices and basic logic gates in SPICE
  - Inverter with complementary BiSFET design simulated at f_{CLK} = 100 GHz with V_{DD} = 25 mV at $E_{inverter}$ = 0.008 aJ → just 2x the Landauer limit





SPICE™ circuit model



"Bilayer pseudoSpin Field Effect Transistor (BiSFET): a proposed new logic device"
S.K. Banerjee, L.F. Register, E.Tutuc, D.Reddy and A. Macdonald., EDL 2009.

NRI Benchmarking Work

Led by MIND & Kerry Bernstein

Four premises to guide benchmarking work:

1. CMOS is not going away anytime soon
   - Charge (state variable), and the MOSFET (fundamental switch) will remain the preferred HPC solution; any new switches is a long term replacement in 10-20 years.
2. Hardware Accelerators can execute selected functions faster than software on a GPU – can offer substantial improvements in throughput
3. Alternative switches often exhibit idiosyncratic behavior we could exploit
   - Some operations may be superior to digital solutions.
4. New switches may improve high-utility accelerators
   - The shorter term supplemental solution (5-15 years) would focus on improving accelerators "built in CMOS", either on-chip, or on-planar, or on-3D-stack

Benchmarking process:

- Establish benchmarks, figures of merit for evaluating candidate devices
- Identify effective alternative circuits, architectures, and/or compute systems in which specific, promising new structures can extend or supersede CMOS
- Explore architectures / designs which support hybrid technology apps
- Estimate technology generation timeframe when cross-over to Post-CMOS alternatives is likely to occur, and which products may be the first to exhibit new models.

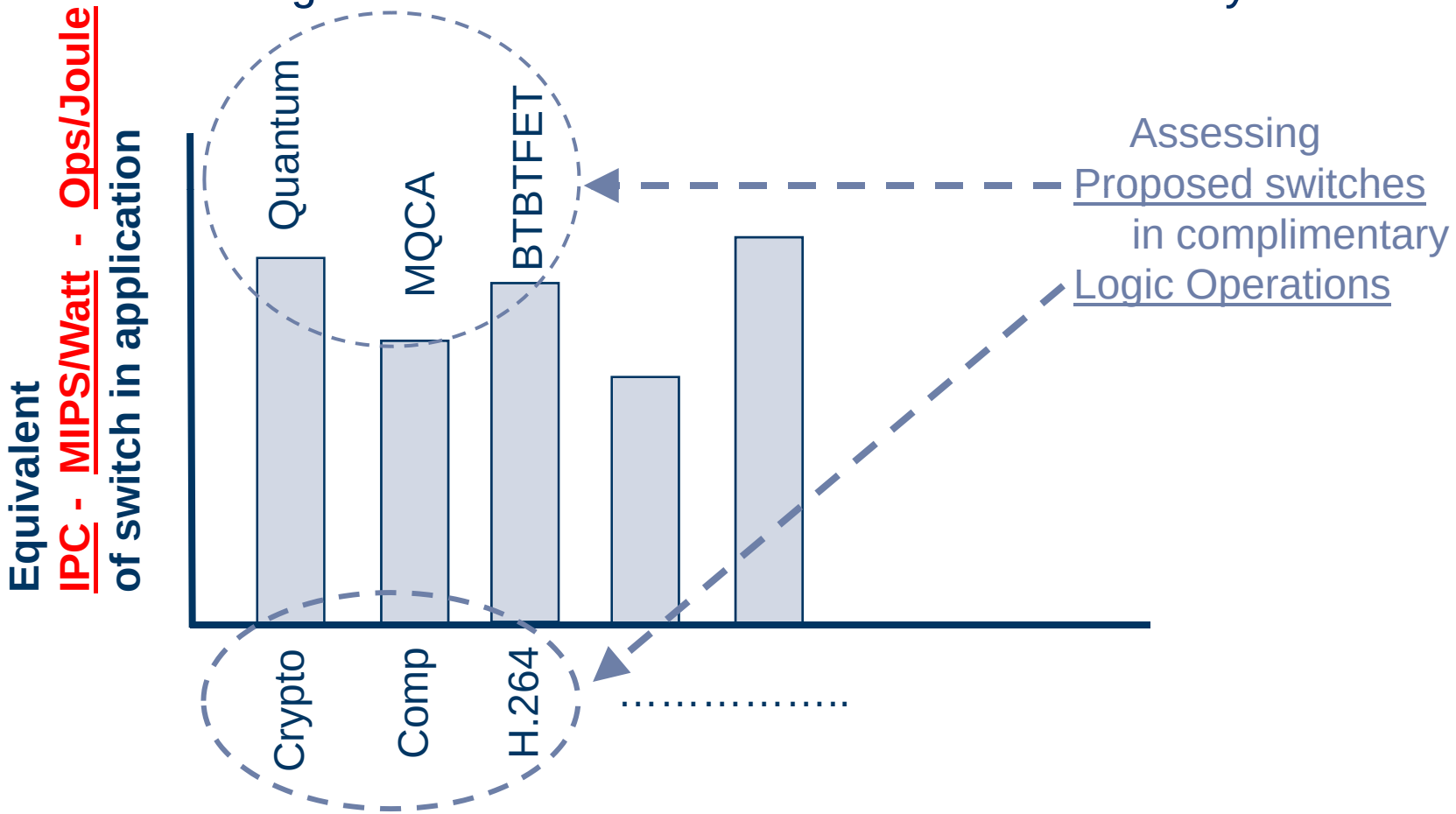
Benchmarking Work

Date	Deliverable
1-Jun	Devices to be benchmarked identified
10-Jul	First Pass Device Assessment
12-Jul	First Pass ITRS Arch, Roadmap Draft
1-Aug	Final Device Benchmarking
18-Aug	Summary at NRI Architecture Workshop
30-Aug	Final Draft, ITRS Architecture Roadmap

Magnetic Tunnel Junction	Markovic	UCLA	WIN
Spin Wave Devices	Khitun	UCLA	WIN
Mag Dot Logic	Roychowdhury	UCLA	WIN
BiSFET	Register	UT	SWAN
Graphene Veselago Devices	Lee	SUNY	INDEX
Excitons	Baldo	MIT	INDEX
Magnetic Rings	Ross	MIT	INDEX
Tunnel FETs	Seabaugh	ND	MIND
Nanomagnet logic	Niemier	ND	MIND
Plasmonic logic	Mazumder	Univ Mich	MIND
Graphene thermal logic	Chen	Purdue	MIND
Graphene spin transport	Ye	Purdue	MIND
Binary Decision Diagram Arch	Datta	PSU	MIND

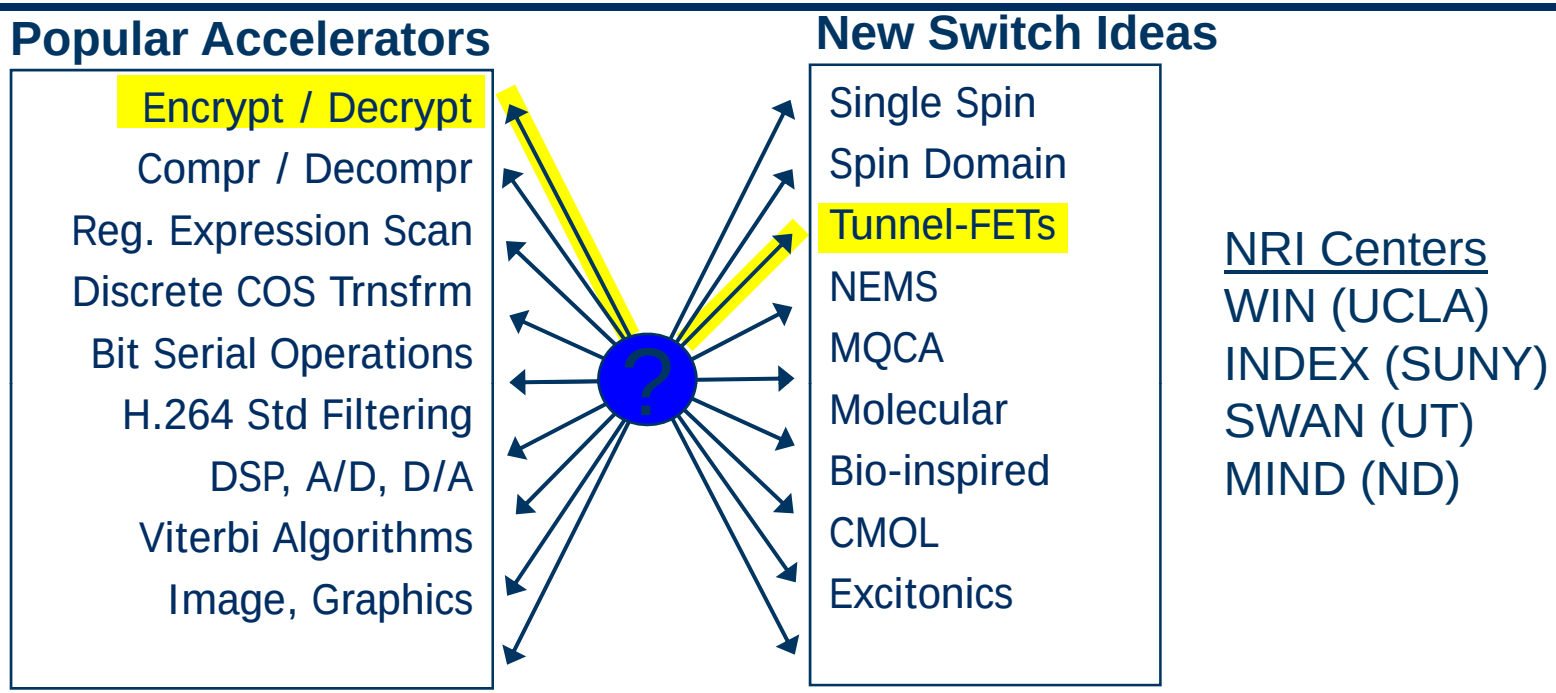
Accelerator Equivalent Performance

- Goal: extend performance after scaling by:
  - Moving more function into accelerators
  - Finding new switches that match function effectively



Compare apples-to-apples, independent of particular strength

Matching Logic Functions & New Switch Behaviors



NRI Centers
WIN (UCLA)
INDEX (SUNY)
SWAN (UT)
MIND (ND)

Example: Cryptography Hardware Acceleration

Operations required:	Rotate, Byte Alignmt, EXORs, Multiply, Table Lookup
Circuits used in Accel:	Transmission Gates ("T-Gates")
New Switch Opportunity: (example)	A number of new switches (i.e. T-FETs) don't have thermionic barriers: won't suffer from CMOS Pass-gate V_T drop, Body Effect, or Source-Follower delay.
Potential Opportunity:	Replace **4** T-Gate MOSFETs with **1** low power switch.

NRI Directions

- Specific areas of technical focus for 2009:
  - Room temperature demonstrations of all phenomena
    - Plan to show RT results next year, or a “roadmap” in simulation to reach RT
  - Accelerate work to demonstrate theory – on simplified structures if needed
    - Theorists need to provide insight on how to verify effects in “realistic” structures
  - Increase focus on logic gate / computational system potential for devices
    - How to connect the devices, how to do logic, how to scale functional density

- Focus on the benchmarking work, for devices and architecture
  - Key questions for a device / architecture:
    - Does it offer the prospect of operation / energy storage lower than CMOS?
    - Does it offer the prospect of non-equilibrium (e.g. ballistic) operation?
    - Does it offer the prospect of energy recovery?
  - Will form basis for selection in the next phase of NRI: 2010 and beyond

- Look for new opportunities with Federal and state partners for:
  - Direct Fed-Ind partnerships on post-CMOS nanoelectronics – creating a Government Observers’ Group to encourage new agency involvement
  - Fed and state investments in nanoelectronics infrastructure at universities
  - Interaction with national labs (NIST, DOE) for expanded work

Questions? More Information?

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