AGENDA : 2009 GRC ETAB Summer Study
Session III: Design Challenges for 3D Packaging Integration

- 8:00 Introduction - John Darringer, IBM
- 8:15 An IFM Perspective of a 3D Design Eco-System
  - Riko Radocic, Qualcomm
- 8:45 Co-Design of Future Architectures with 3D Technologies
  - Mike Rosenfield, IBM
- 9:15 Future Challenges From A Thermo-Mechanical Perspective For 3D Chip Stacks –
  - Gamal Refai-Ahmed, AMD, Bahgat Sammakia, SUNY Binghamton
- 9:45 Break
- 10:00 Taller vs. Smaller: 3D Development and Moore's Law
  - Frank Schellemberg, Mentor
- 10:30 Coping with the Vertical Interconnect Bottleneck
  - Jason Cong, UCLA
- 11:30 Architecture and Application Perspectives for 3D Integration
  - Yuan Xie, Penn State
- 12:00 Panel ? What are the top areas for 3D research? ? Moderator - John Darringer
- 12:30 Lunch
3D Design Eco-System
Now – Soon – Future : an IFM Perspective

prepared for : 2009 GRC ETAB Summer Study
Session III: Design Challenges for 3D Packaging Integration

RikoR

Tuesday, June 30
Background Landscape
Integrated Fabless Manufacturer

- Bifurcation of the Traditional Fabless Model
  - Required for leadership on the (b)leading edge
  - Required for Supporting the Scale of our Business

- Vertical Entity
  - System Design
  - Chip Design
  - Production/Assembly

- IDM
- IFM
- Fabless/Foundry

Challenge in Harmonizing:
- R&D with Value Based Culture
- IP Ownership with Multi-Sourcing
- Risk Mitigation with Agility
- Different Business Models & Interests
  - etc...

- Fabless: Focused on Differentiated Value-Add
  - By culture, definition and heritage
  - Roots are differentiated: buy vs make

- Not vested in the Vertically Integrated Model
  - With roots in make vs buy integration

- (Fabless) Designers are Technology Un-Aware
  - Used to Experiencing Technology through EDA Tools
### Qualcomm TSS Roadmap

<table>
<thead>
<tr>
<th>Stage</th>
<th>TSV</th>
<th># TIERS</th>
<th># VIAS</th>
<th>TSV Diameter Si Thickness</th>
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</thead>
<tbody>
<tr>
<td>STAGE1</td>
<td>Cu via after FEOL</td>
<td>2</td>
<td>1000’s</td>
<td>6um/ 50um</td>
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<tr>
<td>STAGE2</td>
<td>Cu via after FEOL</td>
<td>2-3</td>
<td>10,000s</td>
<td>2-3um/ 25um</td>
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<tr>
<td>STAGE3</td>
<td>Cu via after FEOL</td>
<td>3 or more</td>
<td>&gt;</td>
<td>&lt;2-3um/ &lt;25um</td>
</tr>
</tbody>
</table>

- Projections based on current realities and outlook
- It is still early days in the technology and sourcing life cycle

**Develop Design Infrastructure for Stage 1 but with Focus on Road Map**

TSVs => smaller / Si => thinner / options & challenges => proliferating
What We Are Trying to Build: **Through-Si-Via Stack (TSS)**

### Complex Integrated Heterogeneous Die Stack

#### Tier 1: CMOS SoC
- TSV (connect frontside to backside)
- Very thin Wafer (manage TSV aspect ratio)
- Active face down

#### Interface uBump
- Backside Metal (interface to uBump + ltd routing to allow offset of uBump vs TSV)
- uBump (Tier to Tier interconnect)
- Very thin underfill

#### Tier 2: Memory or Analog or…
- Regular die
- Frontside Metal (interface to uBump)
- Active face down

#### Package Bump
- Regular flip chip bump
- Regular underfill

#### Package
- Regular substrate
- Regular plastic potting
Product Design Eco System...

- **Generic View of the Chip Design Eco-System**
  - a structured flow with many procedures and steps
- **Manufacturing Process Information**
  - flows UP the flow - *in form of constraints*
    - Rules, tech files, models, etc.
- **Product Design Information**
  - flows DOWN the flow - *in form of specifications*
    - RTL, NL, GDS, etc.
- **Historically the Hand-Offs and Interfaces were Reasonably Well Defined**
  - Open and ‘de-facto’ Standards
  - Between ‘ecosystems’ and Across the Levels of Hierarchy
Design Eco-System Challenge: Costs

• Chip Design Expensive = 10’s of M$

• Part of the Cause: Iterative Re-Dos and Re-Spins
  • Instability in System Specifications
  • Instability in Process Technology

• This is an Especially Acute Concern with 3D Technologies
  • Allows new and untried degrees of freedom in architecture
  • Allows new and untried sensitivities in the manufacturing process
Eco-System for 3D Design

- Segment Design Eco-System into 3 Groups
  - “Design Authoring” – actual chip design
    - (Expensive) Actual Chip Design – Output GDS
  - “PathFinding” – system space exploration
    - (Cheap) Quick & Dirty System Design – Output Clean Specs
  - “TechTuning” – physical space exploration
    - (Cheap) Multiphysical Chip Simulation – Output Clean Constraints
PathFinding

a Design Co-Optimization Methodology for TSS
System Level – to – Chip Level

RikoR

May 09
Challenge: Disruptive Technology Adoption

- How to connect a Technology Concept with real, in-product, implementation

- Explore design and architecture possibilities to leverage a given technology opportunity
- Address risk concerns early enough and well enough to attract product teams towards exploiting the technology
- Tune concurrently the architectural degrees of freedom to optimize the target product characteristics

* see ICICDT ’08 and DAC ’08 papers

Let's Call it … “PathFinding”
Infrastructure for PathFinding

**Past:** Exploratory Analyses
- Use ‘guru’ model & Excel
- Evolutionary Process
- Trials in Design Authoring flow

✓ *OK in domain of predictable ‘happy scaling’*

**Future:** PathFinding
- Cannot rely just on experience
- Relative Fidelity vs Accuracy
- Cannot use Design Authoring flow

✓ *Required for ‘fast failing’ with many options*

**Output:** ESTIMATE of cost, power, performance…
- **Requirements:** Maintain FIDELITY, use predictive models, sensitivity estimates & behavioral descriptions

**Require Specialized Design Space Exploration Flow**
- PathFinding
  - vs. Design Authoring
  - Spatially Aware
  - vs. Functionality & Performance only

✓ *Required for ‘fast failing’ with many options*

**Output:** Working and Yielding Si parts & Systems
- **Requirements:** exact and based on full Design Enablement infrastructure
What is this “PathFinding” anyways...

**Ideal**: Black Box Design System that Seamlessly Optimizes Process & Design
- Leverage Existing Design Flow Paradigm
- Optimization = Looping Through the Flow
  - otherwise it is not ‘optimization’
- Current Practices
  - Do Nothing
  - Informal, ad-hoc, guru wing it…. or
  - Complete Trial Design

**PATHFINDING IS a Design Flow that allows**: 
- **Fast & Iterative Looping**
  - Adjustable trade-off of speed vs. accuracy
- **Structured & Holistic Analyses**
  - A systematic ‘practice’ for optimization
- **Predictive Analyses**
  - It has to be based on predictive models

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I/P Variables:
- Process option A, B, C
- Design option X, Y, Z ... etc..

Magical “Black Box”

O/P Estimates:
- Die Area
- Power
- Yield
PathFinding: from System to GDSII in ‘no time’

Product requirements

1. System-level design exploration for 3D
   - IP-models (virtual tech.)
   - Functional Model: Blackbox, behavioral, RTL
   - Parametric Model: Performance, power, cost
   - Functional partitioning
   - Block-diagram (spreadsheet)
   - System-level design (incl. 3D partitioning)

2. RTL-elaboration: bridging gap between system & physical design
   - Component lib (virtual 2D tech.)
   - Gate lib (virtual 2D tech.)
   - Component-level synthesis (Optional)
   - RTL synthesis (for various Technologies)
   - Architecture in SystemC (RTL/behavioral/black boxes)
   - Gate-level architecture (soft, hard macro, gate-level netlist)

3. Physical design prototyping for 3D
   - Physical design lib (virtual 2D tech.)
   - DRM (virtual 3D tech.)
   - 3D stack design
   - 3D Thermal/Cost analysis
   - Constraints for design authoring

Performance/Power/Cost
PathFinding Next Steps?

- **Next Phase Development Opportunity**
  - Past: Spatially Un-Aware Design Space Exploration
  - Phase 1: Physical PathFinding
  - Phase 2: Architectural PathFinding

- **Phase 3: Integrated Product PathFinding?**
  - From Architecture through Physical Si Design through to Packaging
  - Output Specs (Design, Process & Package) rather than Working Si
  - Output ‘virtual prototype’

**Phase 1: Physical PathFinding**
- Partition / Floorplan & Virtual Route
- Existing Design Specification
- but at Multiple Levels of Hierarchy
- 3D Technology ‘knobs’

**Phase 2: Architectural PathFinding**
- Different Architectures
- Different Target Technologies
- Physical Prototyping
- Scripted Flow with all Knobs

**Phase 3: Product PathFinding**
- Package Level Exploration
- Different MCM/SiP solutions
- Fully Integrated Exploration
- Architecture to Product
TechTuning
Technology Co-Optimization Methodology for TSS
Chip Level – to – Process Technology

May 09
New 3D TSS Stack Design Considerations

- **Traditional Thermal & Mechanical Domains of Concerns**
  - Thermal & Mechanical analyses typically ignored at chip design level
  - Mostly a Package or System level concern
  - At chip level, managed through max die size & max power rules

- **3D Technology is a Chip Level System Integration Technology**
  - 3D Technology = Direct & Intimate Interaction Across Several Die
  - With TSS - where does the Si chip end and the package begin?
  - Cannot Ignore Thermal and Mechanical Interactions during Stack Design
    - Cannot manage thermal & mechanical issues at package level only
    - Cannot treat a die as a monolithic slab of Si only
    - Cannot manage empirically ⇔ Need Ability to Simulate
Thermal Concerns & Requirements

Example Concerns:
- **Hot Spot** (T > X°C) on any Tier due to Stack Power Dissipation
  - vs. physical and layout factors
    - thickness, uBump distribution, underfill & potting properties, etc…
  - vs. chip design factors
    - floorplans, routing, power management schemes, PNG, etc…
  - vs. use and application factors
    - power distribution and densities on each tier vs P and V corners, etc..
- **Thermal Effect on Device Performance & Variability**
  - Use conditions, layout configurations, package specs…

Stack Design Requirements
- Design rules for bump and TSV placement and density
- Thermal application rules and guidelines inc Chip Design
- Thermal hot spot analysis and TSS stack sign off

Infrastructure Needs
- **Model Format** + Metrology System & Test Structures
- **DATA:** thermal material properties + Validation Data
Mechanical Concerns & Requirements

Example Concerns:

- Effect of Warpage on Stack Manufacturability
  - vs temperatures, die sizes, process flow, underfill properties, thickness...
- Die size constraints for tier1/tier2 combinations
  - relative alignments, temperatures, process flow, underfill properties, thickness
- Strain Effect on device Performance and Variability
  - strain booster relaxation vs thinning, TSV & uBump proximity..

Product Requirements

- Design rules
- Mechanical application rules and guidelines inc Chip Design
- Mechanical hot spot analysis and TSS stack sign off

Infrastructure Needs

- Model Format + Metrology System & Test Structures
- DATA : mechanical material properties + Validation data
TechTuning Requirements

- Simulators
  - Baseline Software tool(s) and Methodologies
  - Suitable EDA Partners
  - ....
- Models
  - FEA vs more abstract behavioral model?
  - Absolute values vs values relative to some reference point?
  - Modeling of individual layers vs. smear a stack of layers?
  - Compact Modeling methodologies
  - ....
- Data
  - FEOL, RDL, uBump, FC Bump, Underfil, Substrate, Package ...
  - Material, Young’s Modulus, Poisson’s ratio, TCE, Stress Free T..
  - Thermal Conductivity
  - Geometric Properties….
  - ....
- Standards
  - Model Formats (not coefficients)
  - Interface Format for Handoff Between Tools…
  - Metrology Systems & Definitions
  - ....
- Use Flow
  - Use Flow
  - Calibration QA Methodology
  - Validation QA Methodology
  - Use Environment QA Methodology
  - ....

THIS IS A LOT OF WORK + NEW STUFF !?!?

BUT necessary if TSS technology is to go mainstream

SO LET US BEGIN
-If not us - then who?
-If not now- then when?
Modeling and Simulation Granularity

- Simulation (modeling) Occurs at Different Design Abstraction Levels
- Dependent on Granularity of Process and Design Input
  - Granularity of Material parameters
  - Granularity of Layout parameters
- Only Some Combinations Make Sense
  - e.g. if process input is monolithic Si slab - there is no point of any design input beyond die footprint (as used for package level sim)
  - e.g. if the design input is a LEF/DEF there is no point of detailed material properties
- TechTuning Goal is to Get Thermal & Mechanical Simulations Analyses for:
  - DEF Level floorplanning & package design
  - GDS level verification
- Ergo require “Smear” models and/or “Compact” model
  - Should be easier to manage at both, the source and the use end
  - Encrypted Models would work as well
TechTuning Hierarchy

- **Challenge: Multi-Scale & Multi-Physics**
  - No single integrated solution (today)
  - Use sub-modeling approach w/ Hierarchical Model & Infrastructure
  - Leverage existing infrastructure as much as possible

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<th>Multi-Scale</th>
<th>Thermal</th>
<th>Stress</th>
<th>Comments</th>
<th>Elect.</th>
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<td>Package</td>
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TechTuning RoadMap?

- This is a loooong term project

Need to define a practical and synchronized methodology for Model Formats, Material Characterization and Simulation Solutions

- But a necessary one to enable proliferation of 3D technologies

SPICE-like
- Industry Standards
- Model Formats
- Competing Simulators

CMC-like
- Standardization
  - Participation by Supply Chain
  - Standardization of User Requirements

GSA
- Standardization

CMC
- Simulator Technologies
- Model Format Taxonomy
- Characterization Infrastructure

R&D proposed Methodologies

Package Level FEA Capability

Need to have an entire ecosystem to support the thermal and mechanical considerations – just like we have one for electrical parameters
TechTuning Next Steps?

- **Next Phase Development Opportunity**
  - Past: Gross Global Constraints
  - Phase 1: Thermal & Mechanical Rules based on Analyses Tools
  - Phase 2: In Situ Design-for-Stacking flow

- **Phase 3: Commoditization?**

  - **Phase 1: TechTuning**
    - Interface to design: complex rules
    - Compliance: hot spot checker
    - Tools focus: ANALYSES
      - Input models: COMPACT models
      - Performance req: must be fast
    - Past:
      - Simple constraints
      - Die size / max power
      - Some placement limits
      - No specific DRC

  - **Phase 2: Design for Stacking**
    - Interface to design: in situ flow
    - Compliance: design simulation
    - Tools focus: CORRECTION
      - Input models: Quasi PHYSICAL
      - Performance req: slow is OK

  - **Phase 3: Commoditization**
    - Standard Model Formats
      - Not models – just formats
    - Standard Calibration & Validation
      - In general knowledge domain

- **Phase 3: Thermal & Mechanical Infrastructure Commoditization**
  - Open Standard Model Formats
  - General Practices for Calibration Practices (Test Structures, Measurements..)
  - General Practices for Validation to Si and Compact Model to TechTuning model
Design Authoring
a Physical Design Flow for TSS Stack Design
Spec – to – GDS

RikoR
May 09
2.5D Design Authoring: Stage -1 Requirements

**Required EDA Tool UpDates**

Mostly require recognition of Double Sided Die:
- Physical Design (P&R) – may need ability to do timing driven TSV placement & connect
- Extraction – need ability to understand TSV and backside RDL all in a single netlist

**Limited need for Two Tier Awareness:**
- Verification - need to be able to verify whole stack – including TSV, u-Bump, RDL, up through T2 pad locations

**Ability to deal with TSS specific factors:**
- Thermo-Mechanical signoff & “TechTuning”
- Voltage Dependent RC for STA
- Design of Chip Utilities (PNG, Clocks..)
## 2.5D EDA Tool Requirement for Stage-1 Product

- **If No RDL Routing = Simplified EDA requirements for PD**
  - No need for 2.5D double side aware floor planner or router
- **Fixed μBump -TSV alignment = Simplified EDA requirements for Extraction**
  - No need to extract TSVs – use drop in component model

<table>
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<tr>
<th>Function</th>
<th>2.5D EDA Requirement</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synthesis</td>
<td>NO</td>
<td>• Assume Synthesis is all in 2D, with clean Specs for partitioning and Tier to Tier communication defined in PathFinding</td>
</tr>
</tbody>
</table>
| Floorplan     | MAYBE                | • If Assume that complex TSS floor planning restrictions dictated by Tier-2 are Defined in PathFinding this can be done manually off line  
                  • i.e Need for TSV and Backside awareness is case dependent |
| Layout        | NO                   | • Layout is all in 2D. No need for any Up Dates                          |
| STA           | NO                   | • Assume that the voltage dependence of TSV capacitance can be handled as a corner case |
| PDN           | NO                   | • Assuming basically different power networks that have been well spec’ed out in PathFinding |
| P&R           | MAYBE                | • If Assume 2D routing between fixed I/O’s  
                  • If Need Backside routing between TSVs and-uBumps |
| Extraction    | MAYBE                | • My not be required if use of a fixed Composite Model is allowed by prohibitions in variability in layout |
| Verification  | MAYBE                | • Physical verification across both tiers – based on a scripted approach |
Design Authoring Next Steps?

- **Next Phase Development Opportunity**
  - Current: "2D" Design = multiple layers on single one-sided die
  - Phase 1: "2.5D" Design = multiple layers on single two-sided die
  - Phase 2: "3D" Design = multiple layers on multiple two-sided die

- **Phase 3: Integrated 3D Design Eco-System**
  - Phase 3: 3D Integrated Eco System
    - Integrated PathFinding
    - Integrated TechTuning
    - Integrated Co-Design
      - Si
      - Stack
      - Package

- **Phase 3: 3D Integrated Eco System**
  - Structured & seamless integration of PathFinding / TechTuning ‘side lobes’
  - Integrated Package – Stack – Si Co-Design Practices
  - Standardized Tool Interfaces for easy integration
How Should it all Play Together

Trade Off Sensitivities
Predictive Models
Specifications
Design Enablement
Chip Utilities
Hot Spot Sign-Off

Products

✓ Optimize Specs by Looping in PathFinding
✓ Optimize Technology by Looping in TechTuning
✓ Design Products without Looping
Wild & Wacky Opportunities?

- **Regenerative Cooling**
  - a la Regenerative Braking – when energy becomes expensive
  - Does having multiple die, and the stuff between them enable some form of conversion of heat back into electricity somehow more possible?

- **Charge Re-Cycling**
  - a la Water Recycling – when a commodity resource becomes expensive
  - Does having multiple die, and the stuff between them enable some form of recycling of charge somehow more possible or practical?

- **Distributed Utilities**
  - a la Urban Planning – when centralization causes traffic congestion
  - Seems like managing clocks / PDN / DFT across multiple tiers and technologies becomes a huge headache and there is an opportunity for some structured methodology to redistribute