Architecture and Application Perspectives for 3D Integration

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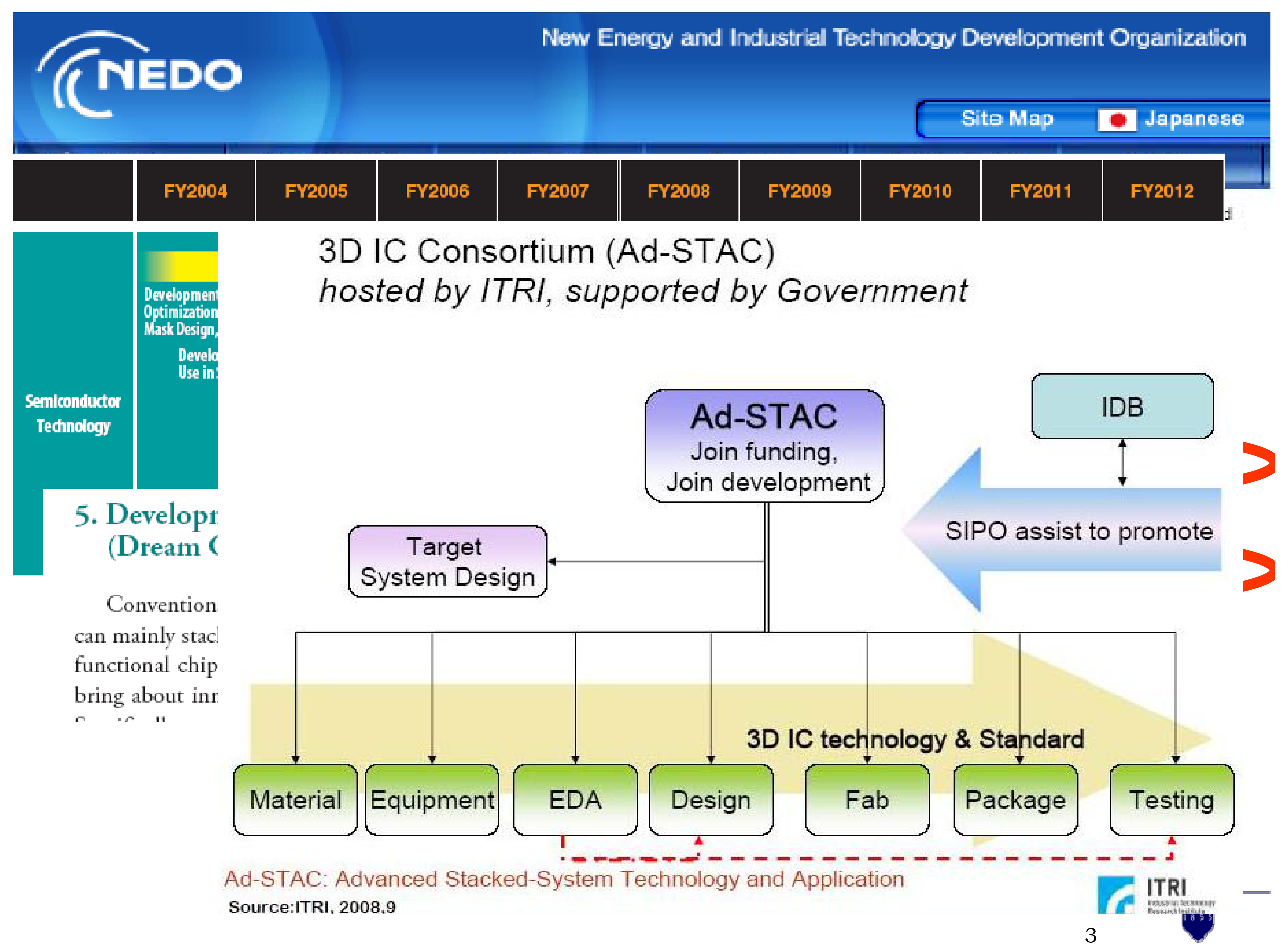
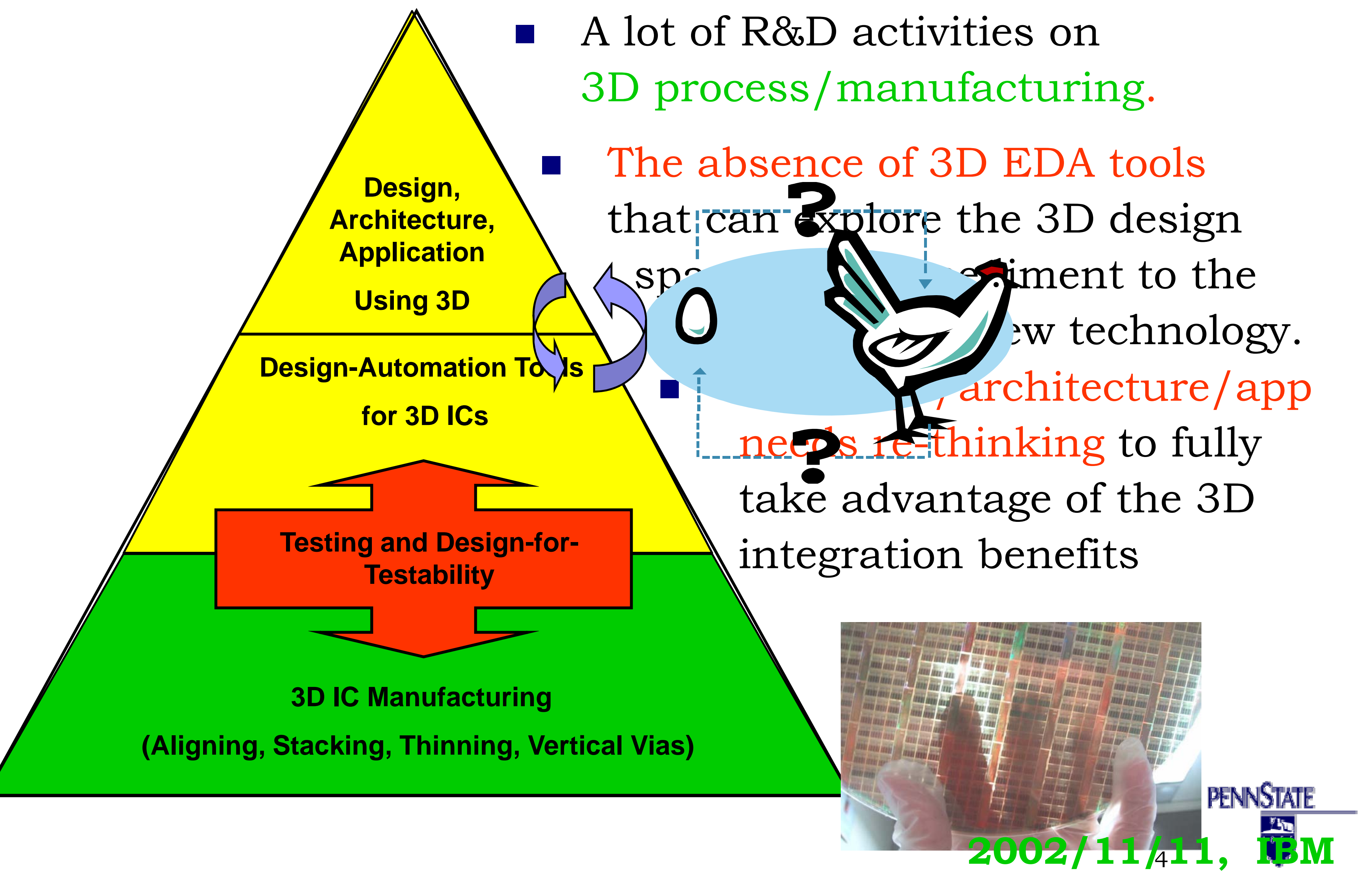
Outline

- 3D activities outside US
- Overview of design challenges for 3D ICs
- Research needs:
  - Identify novel architecture/design
  - Identify killer applications enabled by 3D
  - Cost analysis and cost-driven design flow
  - Testing issues
- Conclusions



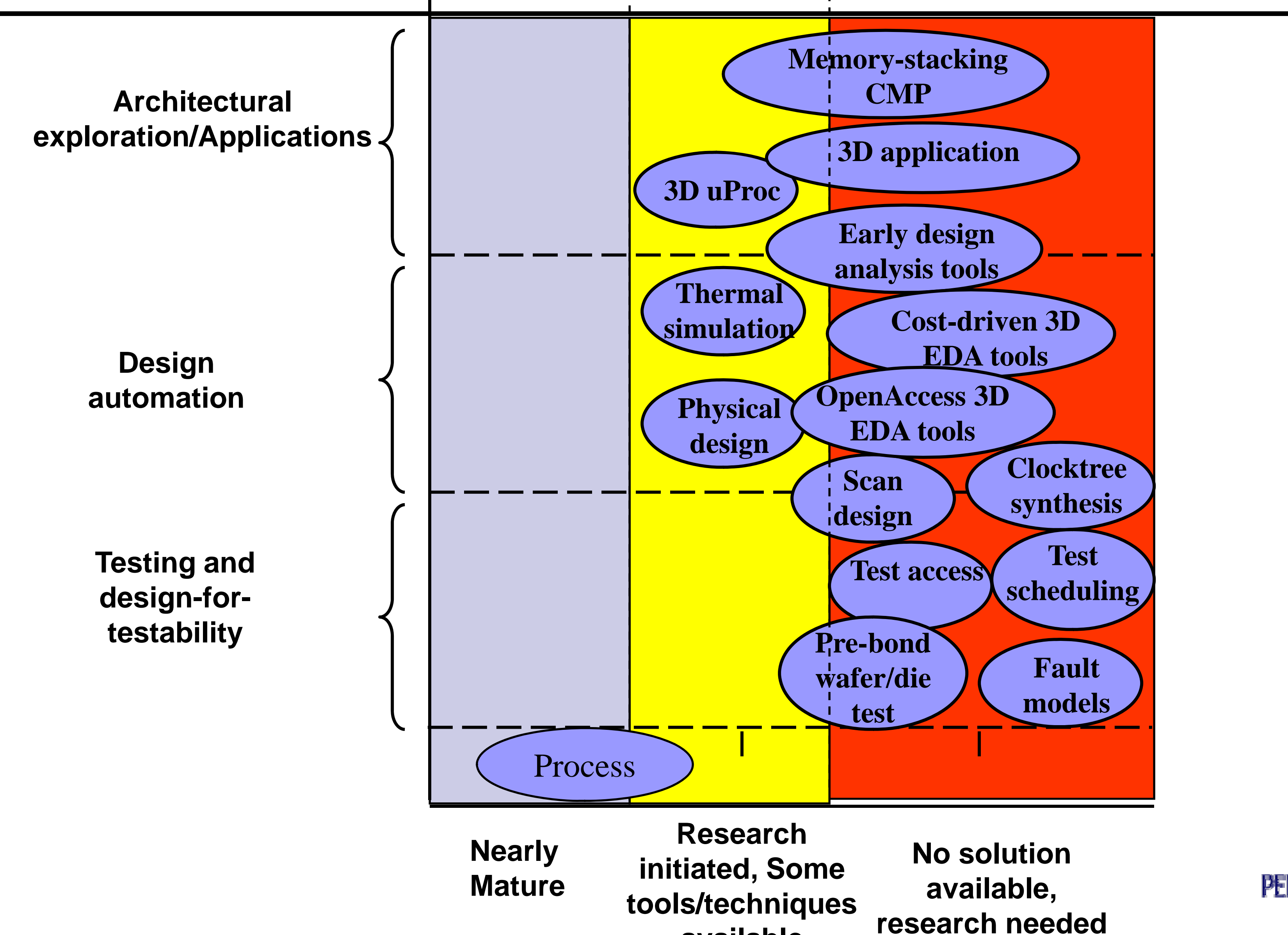
New Energy and Industrial Technology Development Organization
NEDO
Site Map
Japanese
FY2004
FY2005
FY2006
FY2007
FY2008
FY2009
FY2010
FY2011
FY2012
Semiconductor Technology
3D IC Consortium (Ad-STAC)
hosted by ITRI, supported by Government
Ad-STAC
Join funding,
Join development
IDB
SIPO assist to promote
Target
System Design
3D IC technology & Standard
Material
Equipment
EDA
Design
Fab
Package
Testing
Ad-STAC: Advanced Stacked-System Technology and Application
Source:ITRI, 2008,9
ITRI

Challenges for 3D IC Design Adoption



- A lot of R&D activities on 3D process/manufacturing.
- The absence of 3D EDA tools that can explore the 3D design sp… …iment to the …ew technology.
- …/architecture/app needs re-thinking to fully take advantage of the 3D integration benefits

Challenges for 3D IC Design Adoption



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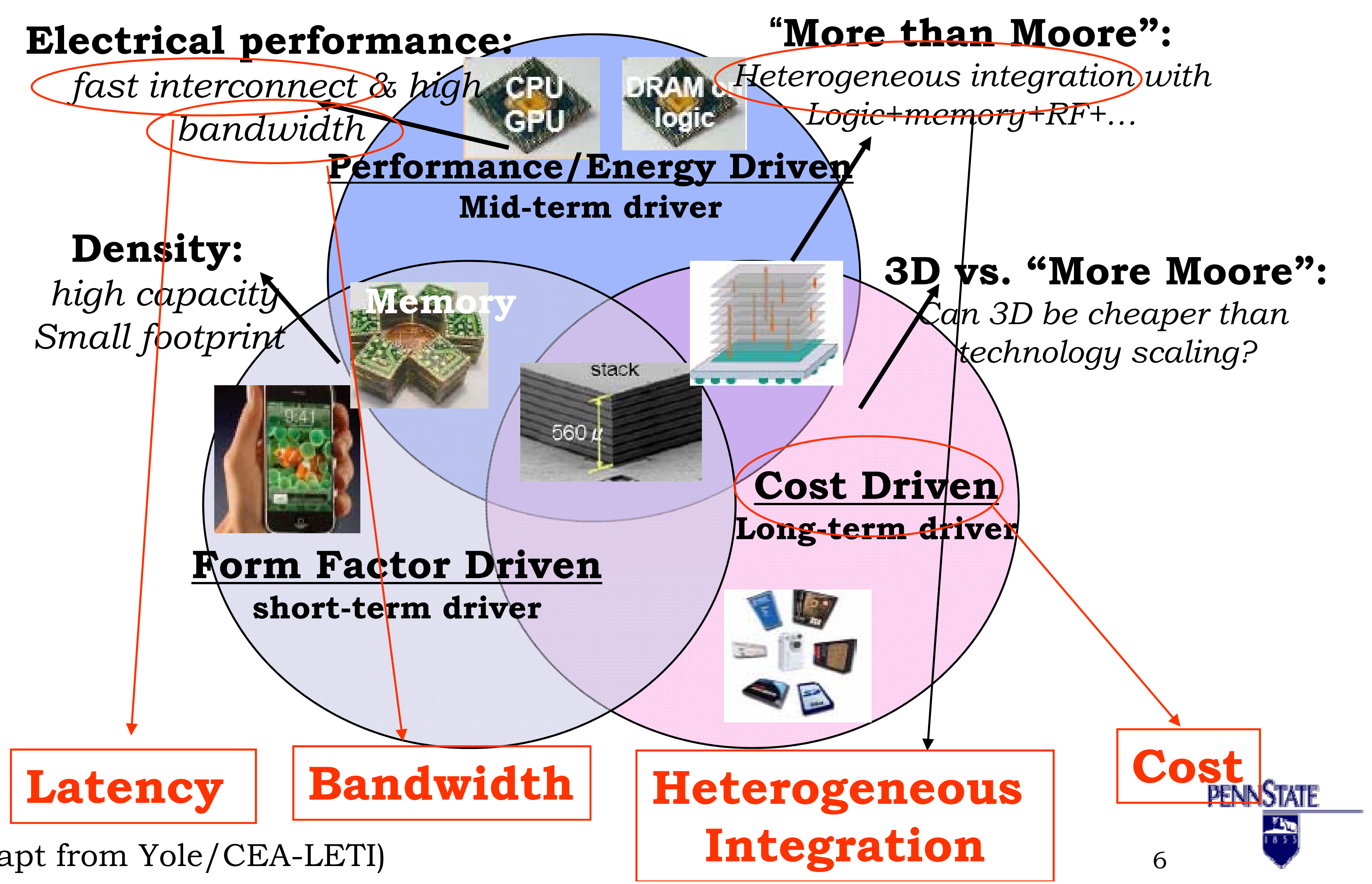
3D Benefits with Market Driver



(Adapt from Yole/CEA-LETI)

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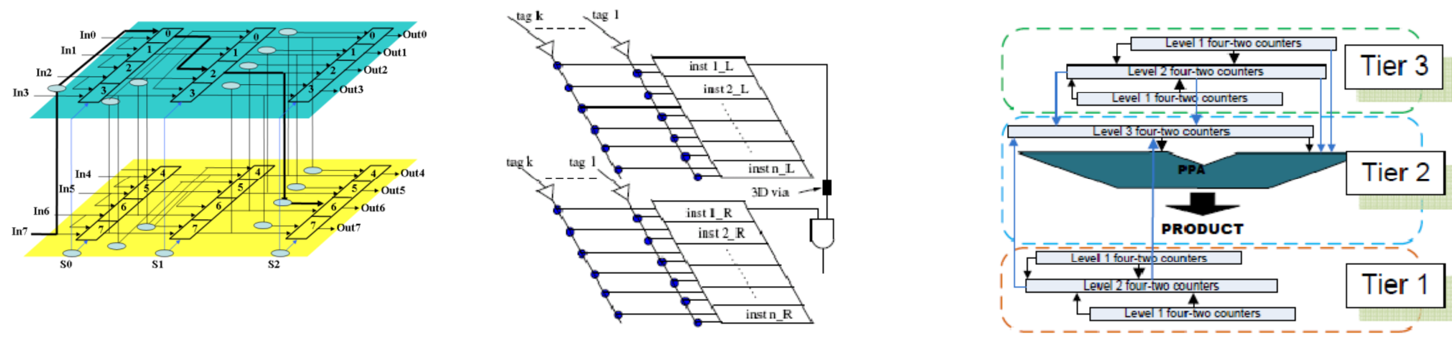
Why Should We Go for 3D?



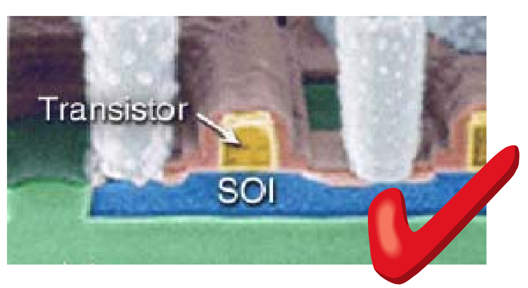
- Wire-length reduction? Delay/Power improvement?
  - E.g., a 3D ALU is 15% faster than a 2D ALU
  - Or, a 10-12% IPC improvement for a true 3D microprocessor

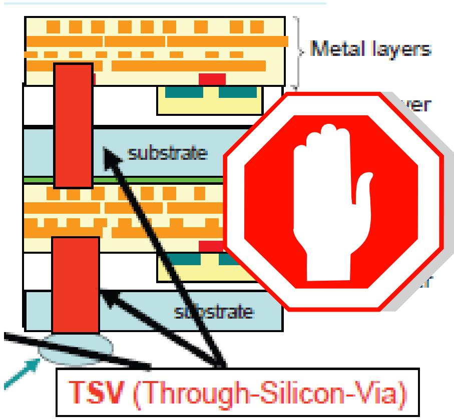
Are these benefits justify the investment in fab/CAD, and the increased design complexity?

Why Should We Go for 3D?

Such improvement could be done in 2D IC with other ways! Why take risk to go for 3D?

--- SOI vs. Bulk, strained silicon, X-routing, or scaling





Need to identify Novel Architecture / Killer Application that can only be done / enabled by 3D

Novel Architecture/Applications

- What are the novel architectural designs enabled by 3D integration?
  - Latency (fast interlayer interconnect)
  - Bandwidth (high number of connections bw layers)
  - Heterogeneous integration
  - Cost benefit

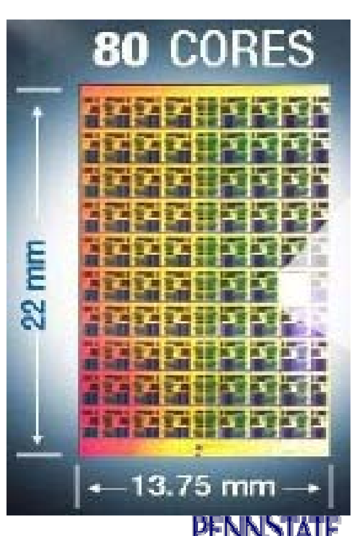
- What "Killer" applications could benefit from the unique features 3D can bring?
  - High-capacity memory
  - Multi/many-core?
  - Exascale computing?
  - From IP-reuse (SOC) to manufacture reuse (3DIC)?

What are the Novel Architectural Designs

What are the novel architectural designs enabled by 3D integration?

- Fine-grain 3D component design (many exisiting work)?
  - Leverage "latency" benefit
  - better performance, but increased design complexity
  - Not necessary exciting

- Memory stacking?
  - Leverage "high memory bandwidth" benefit
  - Help solve memory wall problem
  - Probably a near-term application for many-core
  - Should we re-design the memory interface/organization?



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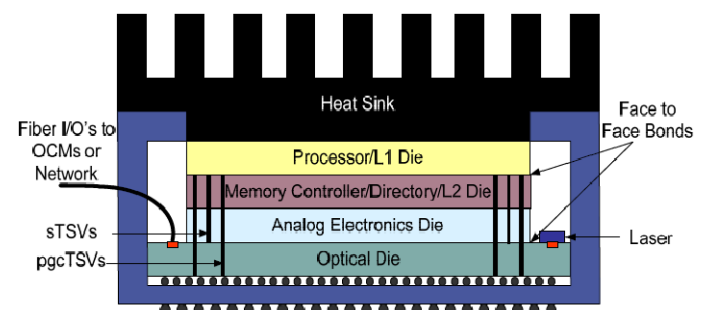
What are the Novel Architectural Designs

Heterogeneous Integration:

- Stacking NVM memory (e.g. MRAM/PCRAM) on logic
  - Instant-on/off feature? Radiation-harden design?
  - Extremely low leakage design?
- Optical device stacking
  - Hybrid electrical / optical interconnect?
  - Solving off-chip bandwidth problem?
- CMOS/non-CMOS integration?
- Different technology nodes stacking ?
  - (e.g. 45nm on 180nm)

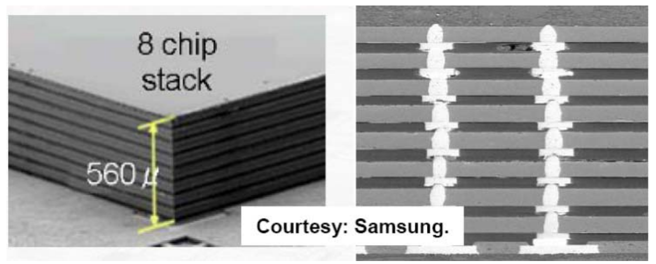


The most exciting feature to be exploited?

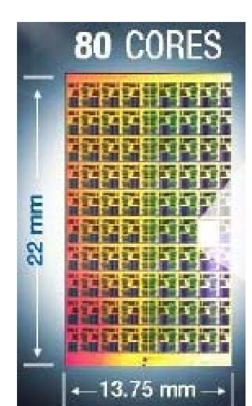
What are the Killer Applications

Identify the Killer Application using 3D

- High capacity memory! Yes
  - Samsung, MetaRAM etc.



- Multi/many-core?
  - Many research activities now
  - No way to go for many-core without 3D?
  - What are the research issues?
    - Memory interface/organization redesign?



What are the Killer Applications

Identify Killer Applications using 3D

- From Petascale to Exascale computing
  - What 3D can enable?
- From IP-reuse to manufacture reuse
  - SOC -> Enables IP reuse!
  - 3D IC -> Enables manufacture reuse?

Research Questions:

--- Are these killer applications? What else?

--- Can 3D be a "disruptive" technology to enable them?

--- What are the design issues?

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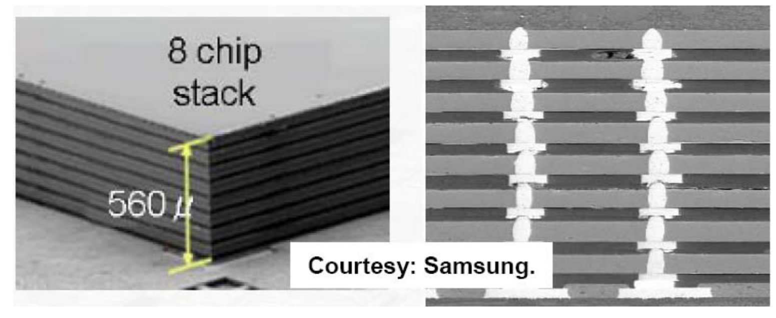
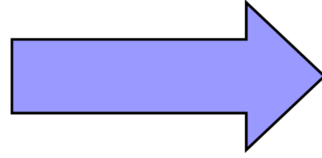
Cost Analysis and Cost-Driven Design Flow

- It all comes down to cost for the adoption of 3D IC in main stream tech! --
  - Does all the benefits come at a higher cost?
  - 2D or 3D? How many layers? W2W or D2D?
  - Any design options to offset the extra 3D bonding cost?
- It is necessary to integrating cost analysis into design flow
  - Explore cost-reduction options
  - Guide design exploration
- Needs close collaboration between foundry & design house





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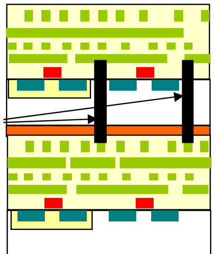
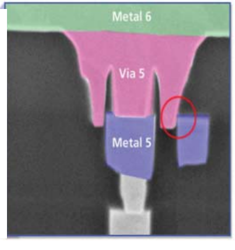
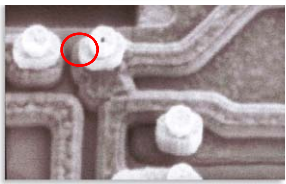
3D Testing







TSV shorts/opens
Imperfect via contacts
Edge effects
Test access, …

Testing is the "No. 1 Challenge" for 3D integration

(Ted Vucurevich, Cadence CTO, 2007)

Understanding of defects unique to 3D integration

Fault modeling and test generation for these defects

Needs Practical solutions for:

- **Pre-bond testing (KGD)**
- **Design-for-testability (DfT) infrastructure (Scan chains, test-access mechanisms, test scheduling, etc.)**

Optimization of scan chains, test-access mechanisms, test scheduling

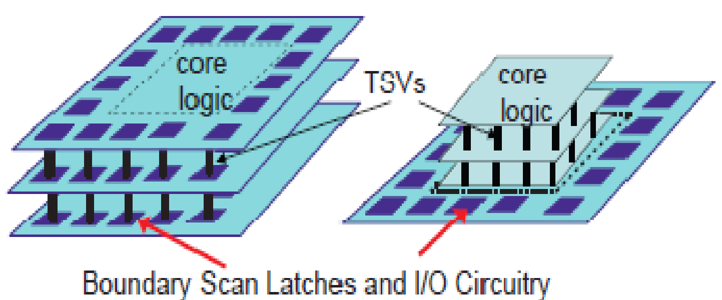
Test Challenges for 3D ICs

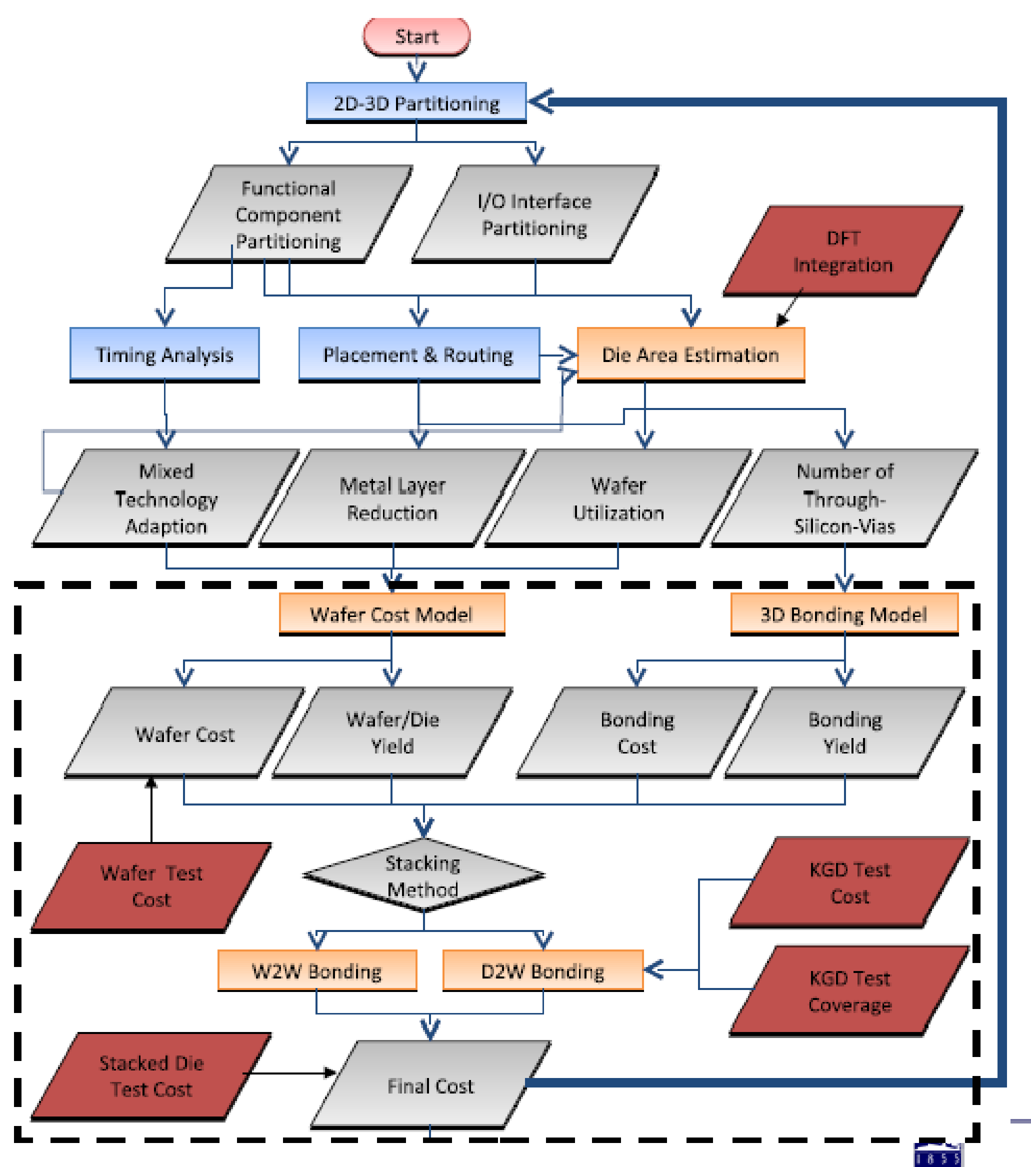
- Wafer probing
- Known-Good-Die Testing
- New Defect Types
- Thermal and Power Delivery in 3D Testing
- Test of TSVs
- Test access and Test-scheduling for core-based 3D IC
- Test Economics and its relationship to other cost

Test Economics

Needs to Understand Test Economics

- Close coupling between test-cost analysis and 3D physical design optimization
- Wafer cost, bonding Cost model, die area, test cost related to various stacking options





Conclusions

- 3D process/manufacture is getting mature
- Design tools and novel design architectures are the key to adopt 3D IC as main stream technology
- Important Research Needs:
  - What are the novel architectural design
  - What are the killer applications for 3D
  - Cost analysis and cost-driven design flow
  - 3D testing issues

"Space on the ground is running out…

The only way is up…

The question is not whether this reach for the sky will happen –

it's happening now –

but what it portends."

Hugh Pearman, May 2004
(The Sunday Times, UK)