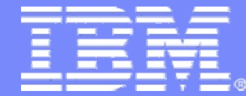


IBM Research

Co-Design of Future Architectures with 3D Integration

Michael Rosenfield
Director, VLSI Systems
IBM Research Division
Yorktown Heights, NY

6-30-09

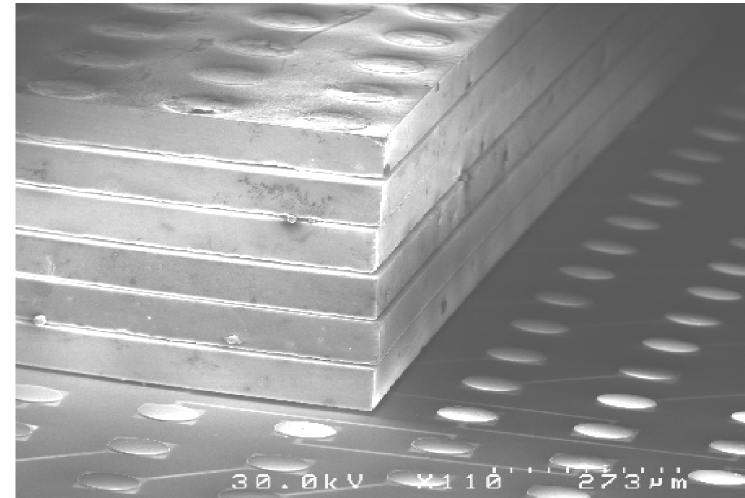
© 2009 IBM Corporation

Outline

- **Introduction and motivation**
- Technology
- Design enablement
- Modeling and analysis
- Summary: suggested future research areas

© 2009 IBM Corporation

3D Integration: Co-design of Future Architectures with New Technologies



As classical CMOS scaling comes to an end, leverage 3D for:

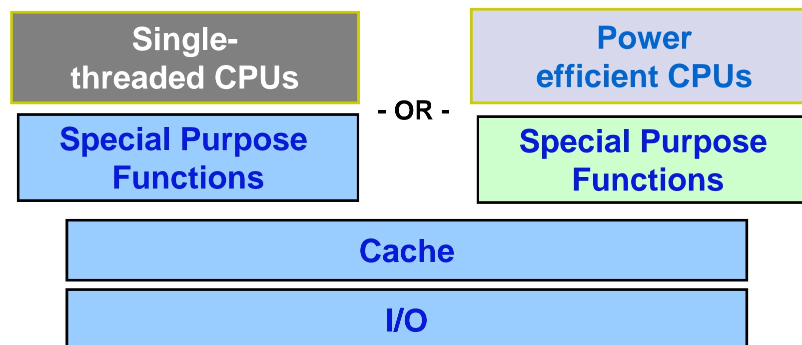
Power efficiency

Form factor

Modularity / shared components

Optimized system design

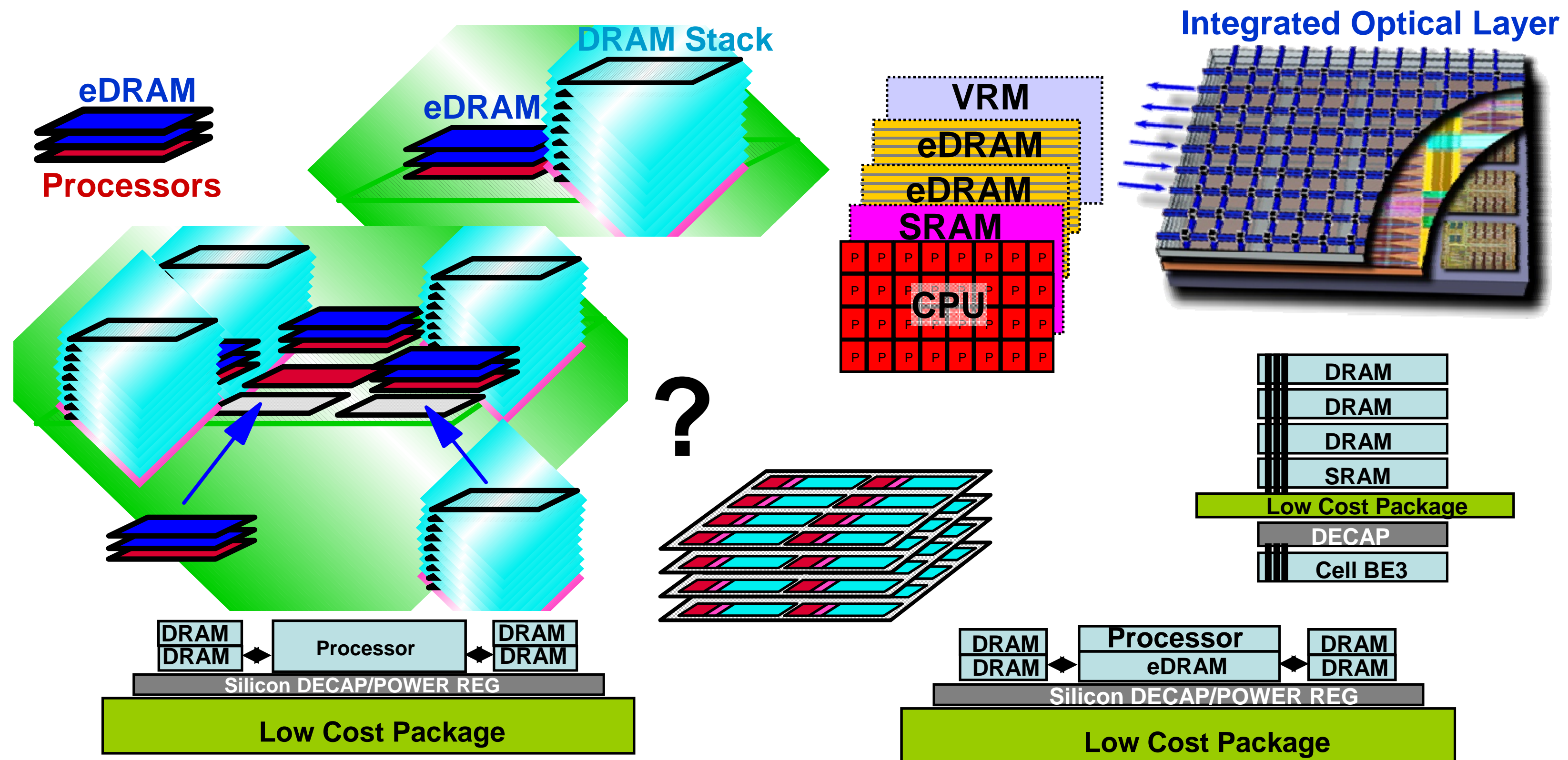
Improved yield



© 2009 IBM Corporation

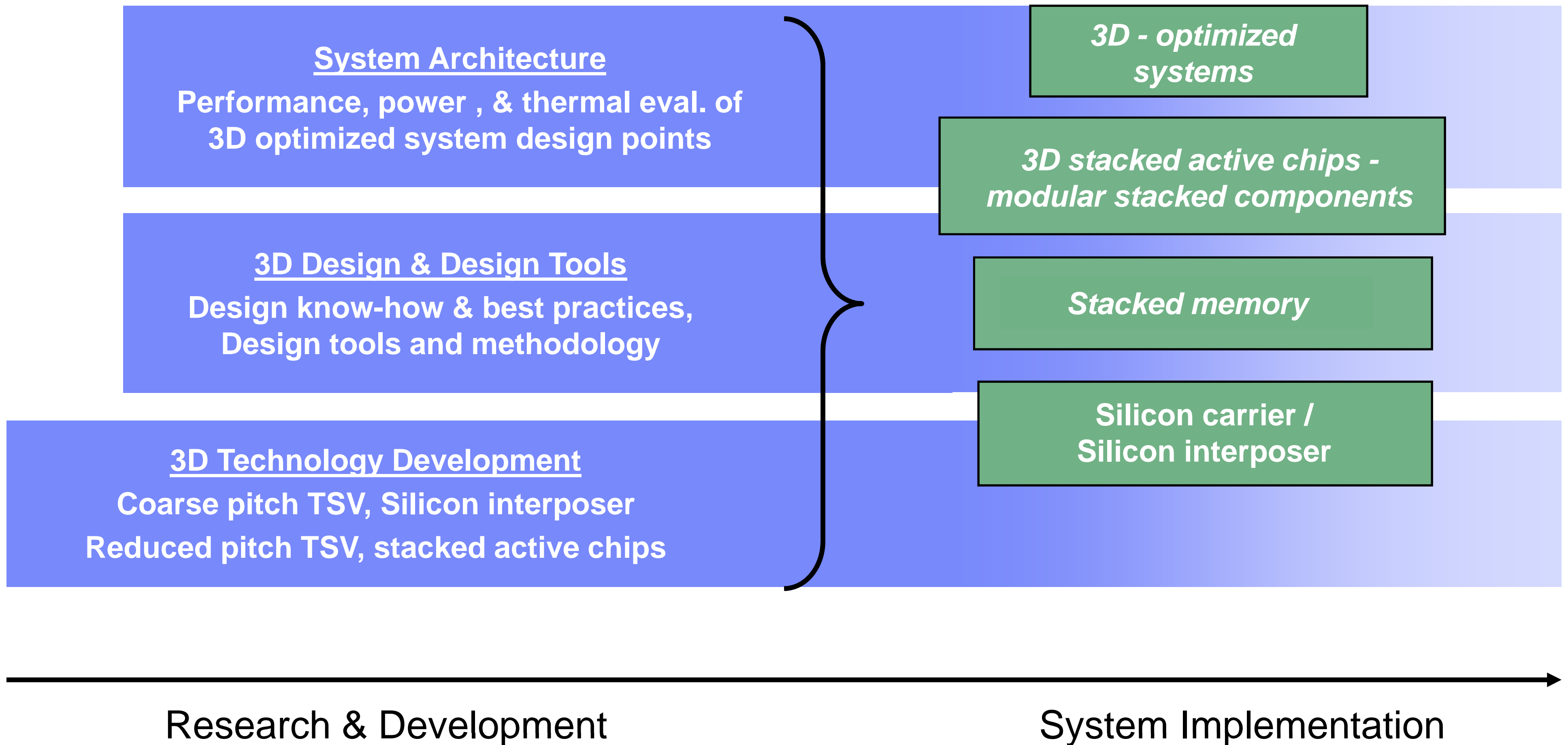
3D: A Family of Technologies and System Options

- **What value does 3D add to a "conventional" system?**
- **What <u>new systems</u> does 3D enable?**



 © 2009 IBM Corporation

3D Integration



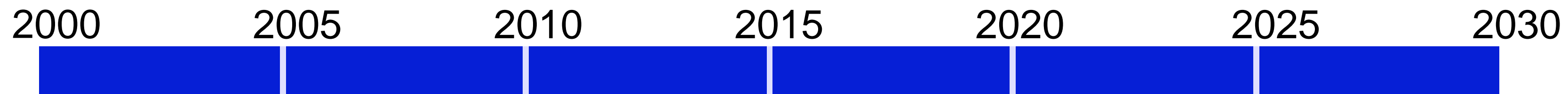
© 2009 IBM Corporation

Outline

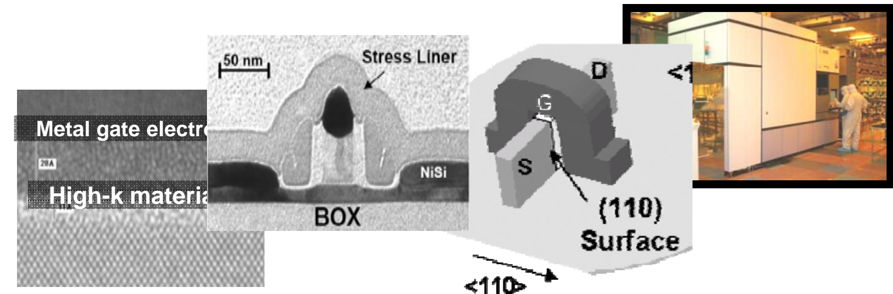
- Introduction and motivation
- **Technology**
- Design enablement
- Modeling and analysis
- Summary: suggested future research areas

© 2009 IBM Corporation

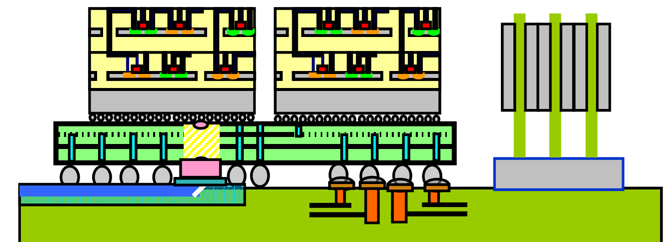
Semiconductor Innovation Roadmap



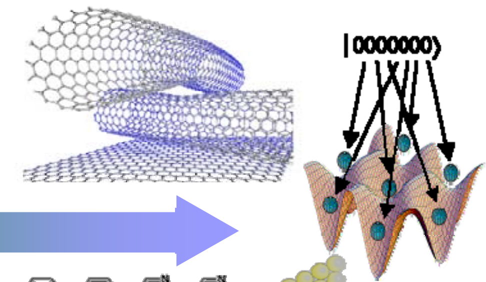
Extending Si CMOS



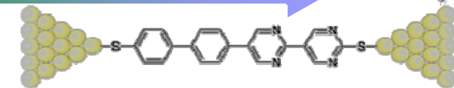
Subsystem Integration



Non-Si FET

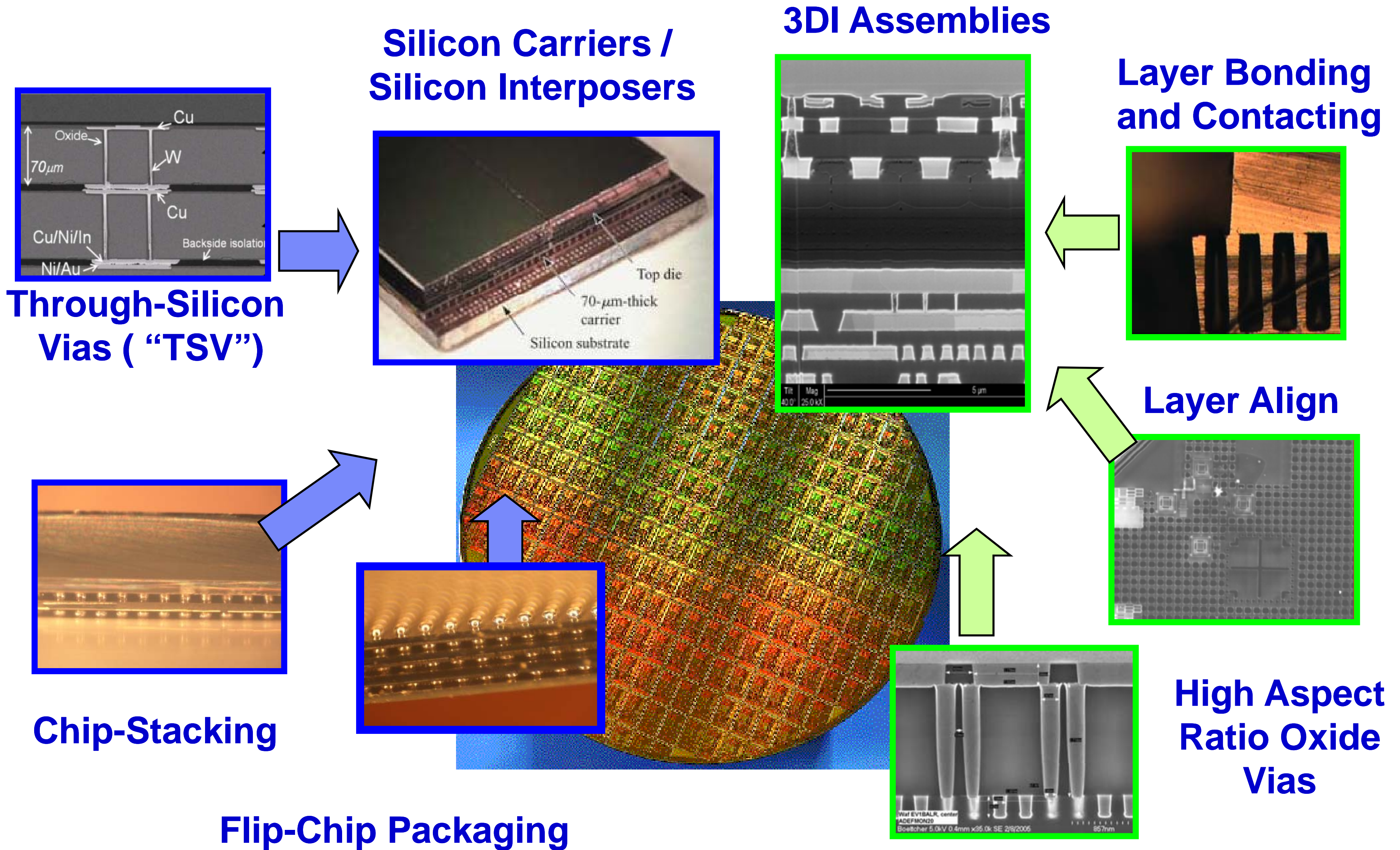


Beyond FET



© 2009 IBM Corporation

3D Integration: *Technologies*



© 2009 IBM Corporation

3D Technology Development

- **There are several variations in 3D technology parameters that can be considered**
  - TSV properties
  - Bonding method
  - Chip stack orientation

- **The various 3D technology parameters may have different effects on the base 2D technology parameters**
  - Ground rule implications
  - Thermal effects
  - Reliability
  - Test & known-good die

As the 3D technology continues to evolve, we need to do VLSI and systems architecture work in parallel

© 2009 IBM Corporation

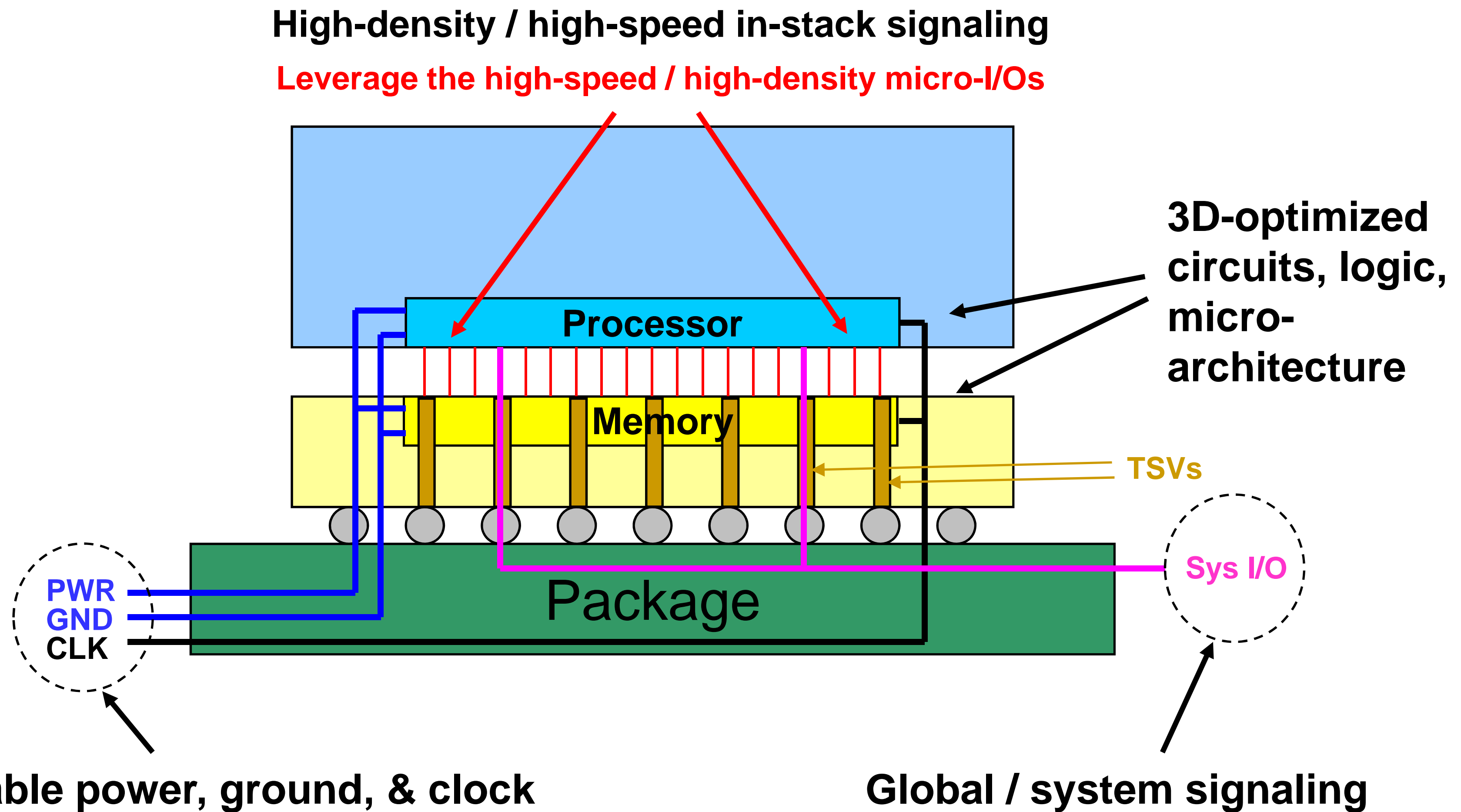
Outline

- Introduction and motivation
- Technology
- **Design enablement**
- Modeling and analysis
- Summary: suggested future research areas

© 2009 IBM Corporation

3D Fundamentally Affects VLSI Design

Chip infrastructure, IP blocks, design know-how, design tools and methodologies



© 2009 IBM Corporation

VLSI Design Implications over Time

- **3D designs will require 3D-compliant and optimized:**
  - Chip infrastructure elements:
    - Clock distribution, power and ground distribution
  - IP blocks:
    - SRAM, eDRAM, and non-traditional array technologies
    - Custom and random logic
    - Within-stack and on- and off-socket bussing and I/O
    - Analog
    - Special-purpose functions, materials
  - Design know-how, and supporting methods and tools:
    - Early and detailed planning and partitioning
    - Electrical and physical optimization and design
    - Automation-enhanced implementation
    - Checking and verification
    - Capture of power & thermal effects

© 2009 IBM Corporation

3D Requires Architecture / VLSI / Technology Co-Design

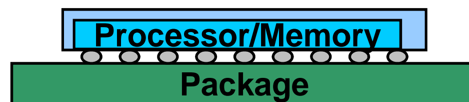
Technology and design interact in new ways:

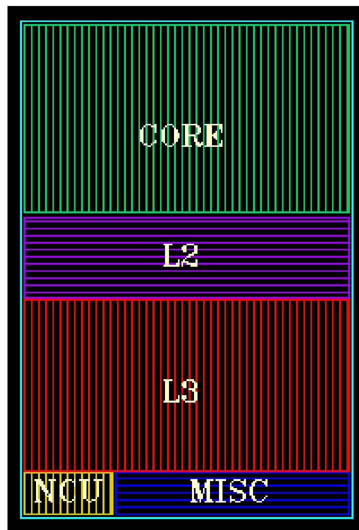
- **TSV materials and wafer thicknesses affect TSV electrical properties**
- **TSV electrical properties affect number of TSVs needed**
- **TSV size affects area overhead, wireability**
- **Sizes of IP blocks affect TSV locations, and vice-versa**
- **Partitioning functions over layers affects number of TSV connections required**

© 2009 IBM Corporation

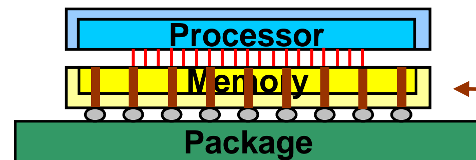
Simple Case: Convert to 3D with Minimal Changes

2D Microprocessor

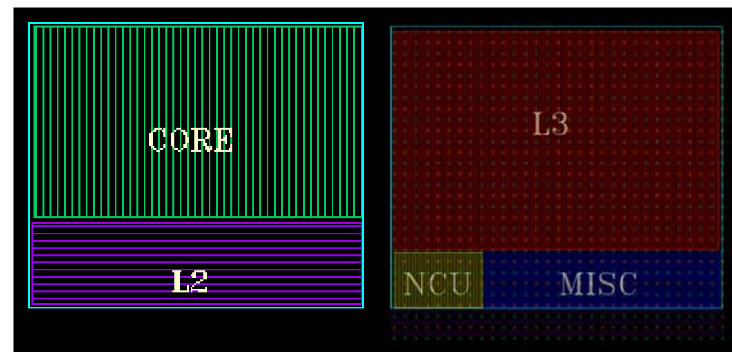




3D Microprocessor in Two Layers



TSV Level (Memory)



TSV Level

- **TSV layer requires a complete re-design**
- **More optimal variation:**
  - Re-floorplan each layer to optimize the new vertical connections

© 2009 IBM Corporation

3D Chip Design: New Considerations

- TSV & Stack Design Planning
- Early Power, IR Drop Analysis
- Early Clock Structure Design
- Stack Thermal Analysis

- Finalize TSV - Stack Networks
- Clock Design Across Stack
- TSV-Aware Logic, Circuit, Physical Design

- 3D Timing
- 3D-Aware Layout-to-Schematic & Schematic.-to-Logic
- Stack Continuity Analysis
- TSV Design Rule checking

- **Planning/High Level Design**
  - Additional architectural and planning needed for shared stack resources during HLD of individual layers
- **Design Development Phase**
  - Partitioning of shared stack resources allows individual layers to proceed independently.
  - Addtional constraints/contracts and crosscheck needed to ensure design closure at both the stack level and system level
- **Pre-tapeout verification**
  - 3D-aware stack-level verification

© 2009 IBM Corporation

3D Integration Impact on Design

- TSV and bond & assembly technology & reliability
- Test strategy for known-good-die
- Power delivery through chip stack
- Thermal impacts & Cooling

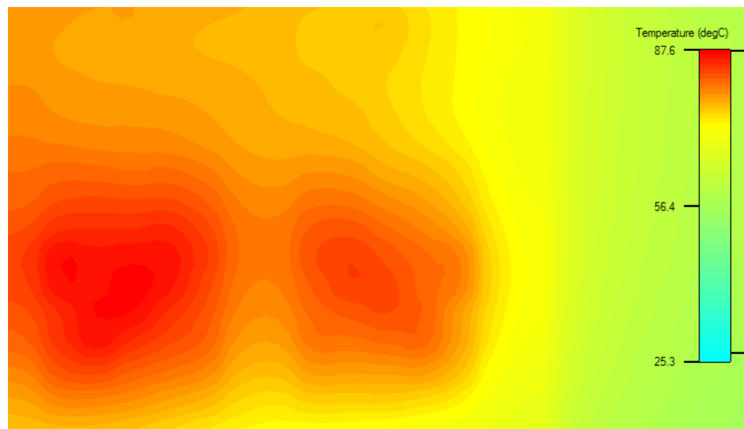
© 2009 IBM Corporation

3D Power / Thermal Analysis and Mitigation

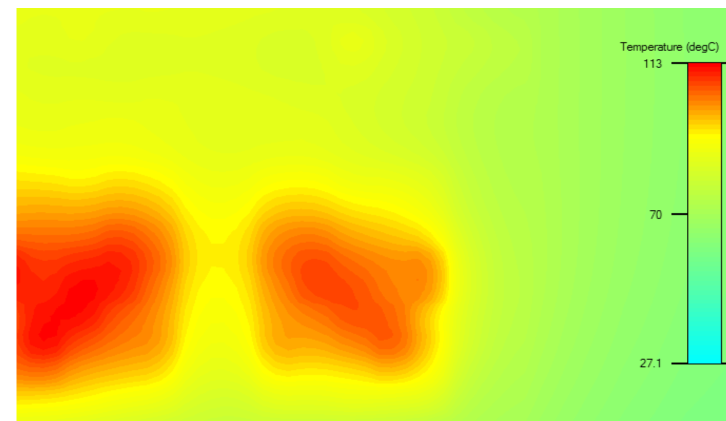
- **Chip Stacking Power Implications**
  - Decreased heat spreading / increased hot spot temperatures
  - Power analysis studies:
    - Compare power, temperature, and performance for early-late design stage analysis of proposed 3D architectures
    - During design, identify chip hot spot(s): temperature and regions

- **Thermal mitigation techniques:**
  - Hardware (autonomic) dynamic task/activity migration
  - Software-guided task scheduling
  - Per-core voltage regulation and power gating via 3D-VRM

Peak temperature 87.6°C
Good lateral heat spreading



Peak temperature 113°C
Poor lateral heat spreading



© 2009 IBM Corporation

Outline

- Introduction and motivation
- Technology
- Design enablement
- **Modeling and analysis**
- Summary: suggested future research areas

© 2009 IBM Corporation

3D Systems Architecture and Modeling

- **In the long term, 3D has the potential to realize systems that do not have attractive 2D alternatives**
  - Different ratios of processing capability to memory capacity to bandwidth
  - Much higher bandwidth, lower latency between components
  - Tight integration of dissimilar or incompatible technologies or functions
    - Different CMOS technology generations
    - Security, I/O, memory, processing layers
    - Optical components, Non-CMOS, etc.

- **Ultimately, we want to analyze systems that are well beyond present capabilities**
  - Workloads that don't exist today
  - 100's of cores, 1000's of threads, 10's of logical partitions, 100's of GBytes cache in many layers

© 2009 IBM Corporation

Systems Architecture and Modeling

- **3D VLSI exploitation will leverage technology attributes not exploited by current software**
  - Significant advances needed on ability to model and analyze tradeoffs
  - Larger and more complex workloads, more complex systems, new design dimensions, etc.
- **Environment needed for combining workload characterization, performance, power, temperature, physical planning, reliability**
  - Use in exploratory and concept-phase stages for designing future systems
  - Serve as front-end to the design process for 3D VLSI systems

© 2009 IBM Corporation

Outline

- Introduction and motivation
- Technology
- Design enablement
- Modeling and analysis
- **Summary: suggested future research areas**

© 2009 IBM Corporation

Summary – Future 3D Integration Research

- **Optimized system design**
  - Systems exploiting 3D will leverage hardware attributes not available today. What new systems does 3D integration enable?
    - An evaluation framework is needed
  - How do we restructure future systems from embedded through servers to exploit 3D integration technology?
- **Quantitative evaluation of performance, power, and other benefits of 3D integration**
  - We all know the potential high level, qualitative, benefits of 3D. It is now time to provide information on the quantitative value of 3D
- **VSLI design enablement**
  - 3D integration fundamentally affects many aspects of VLSI design: clock, power, and signal distribution, through-silicon-via aware design, I/O, test/reliability, design automation tools, etc.
    - How can the large, existing base of 2D design automation tools, methodologies, and designs be extended to effectively leverage 3D technologies?

© 2009 IBM Corporation