Future challenges from a thermal perspective for three dimensional chip stacks

June 2009

Gamal Refai-Ahmed, PhD
AMD Fellow
Product Development Group
AMD
&Chair of PKG Thrust

Bahgat Sammakia, PhD
Professor and Director
S3IP
Binghamton University

S3IP
The Small Scale Systems Integration and Packaging Center
BINGHAMTON UNIVERSITY

Product Features and Specifications Notice

The product(s), features, and specifications presented in this document are under development and/or in their definition stage. This document is preliminary and tentative in nature, and may contain technical inaccuracies, omissions and errors. Information contained herein may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. AMD and BU assume no obligation to update or otherwise correct or revise this information. However, AMD and BU reserve the right to revise this information and to make changes from time to time without obligation to notify any person of such changes.

AMD AND BU ASSUME NO LIABILITY FOR ANY INACCURACIES, ERRORS OR OMISSIONS THAT MAY APPEAR IN THIS PRESENTATION.

Outline

- Definition of the challenges
- Identified Thermal issues
- Final Remarks

Processor may be on top.
In stack fluidics interposer for thermal management not shown

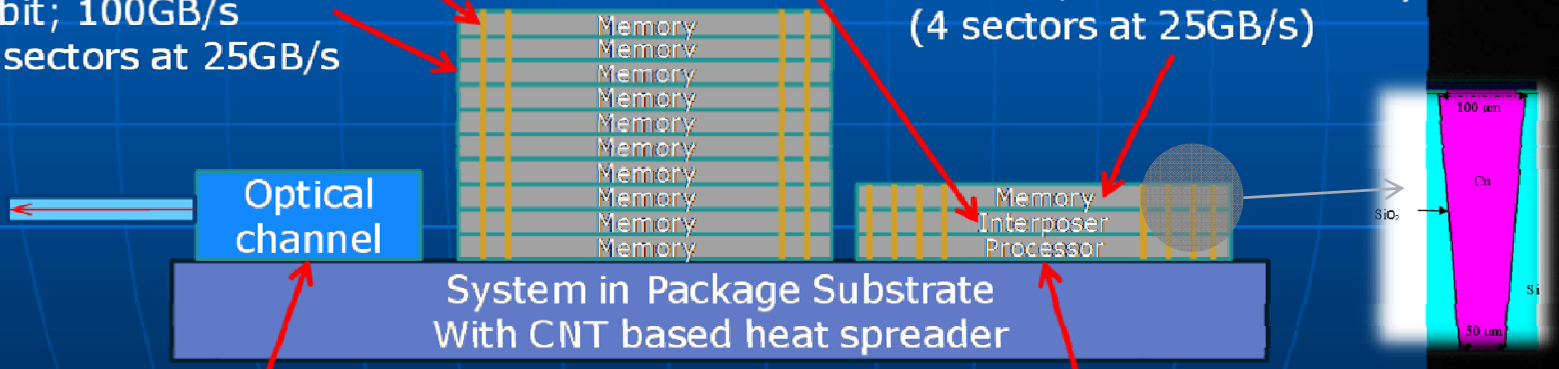
Tera-scale Computing by 2015

TSV die to die connection

Silicon Interposer with:
-Integrated thermal management
-Integrated Passive networks

Memory cube
1Tbit; 100GB/s
(4 sectors at 25GB/s

100Gbit; 100GB/s memory
(4 sectors at 25GB/s)



1TB/s optical transceiver for:
- Off package communication
- On package routing

Processor with 100 cores
Core transistor speed 10GHz
25um thick wafer (~.5V power)

From ITRS 2009, In Progress

The Small Scale Systems Integration and Packaging Center
BINGHAMTON UNIVERSITY

AMD
The future is fusion

Challenges

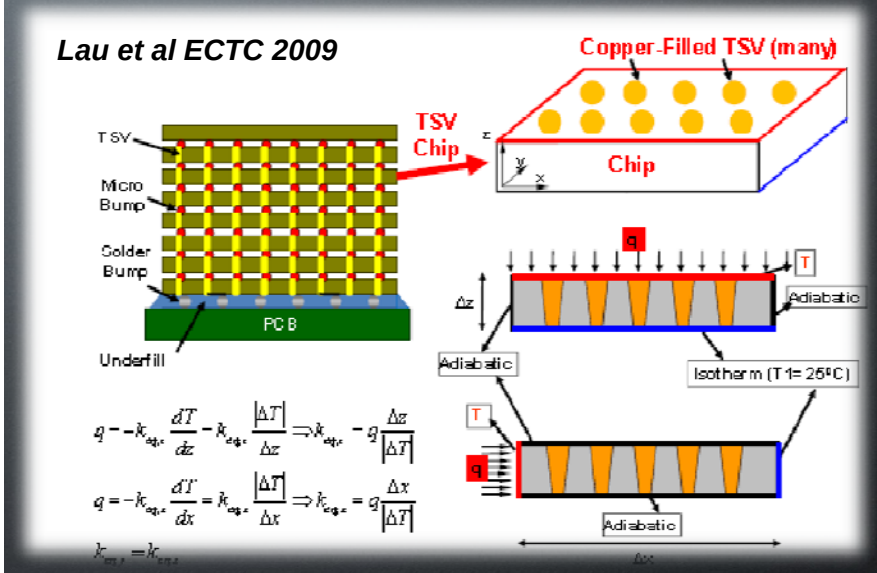
- **Technology Modeling**
  - Utilizing TSV to improve Thermal spreading in-plane and through-plane of the die-stack
    - How much thinner can the die and the TSV become without any side impact on the manufacturability of wafer and provoking Joule heat effect
  - Understanding the Joule heating
    - Impact of lifetime reliability from the current density, as well as the thermo-mechanical stresses when the TSV gets thinner
  - Removing the heat dissipation
    - Flow Instabilities Vs Power Map in the real life application
- **Architectural Exploration Analysis Tools**
  - Impact on the performances as a function of the thermal management and Si architecture
    - Re-arrangement hot spot to have the lowest thermal resistance

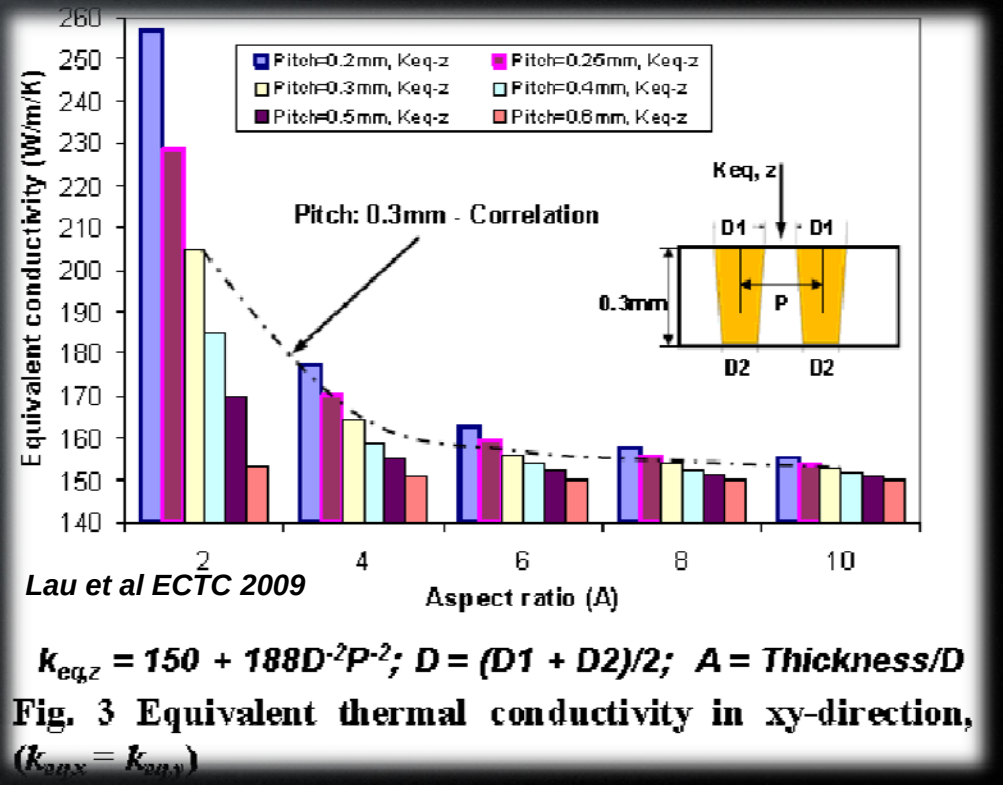
Outline

- Definition of the challenges
- Identified Thermal issues
- Final Remarks

Challenge:

- Utilizing TSV to improve Thermal spreading in and through the die-stack





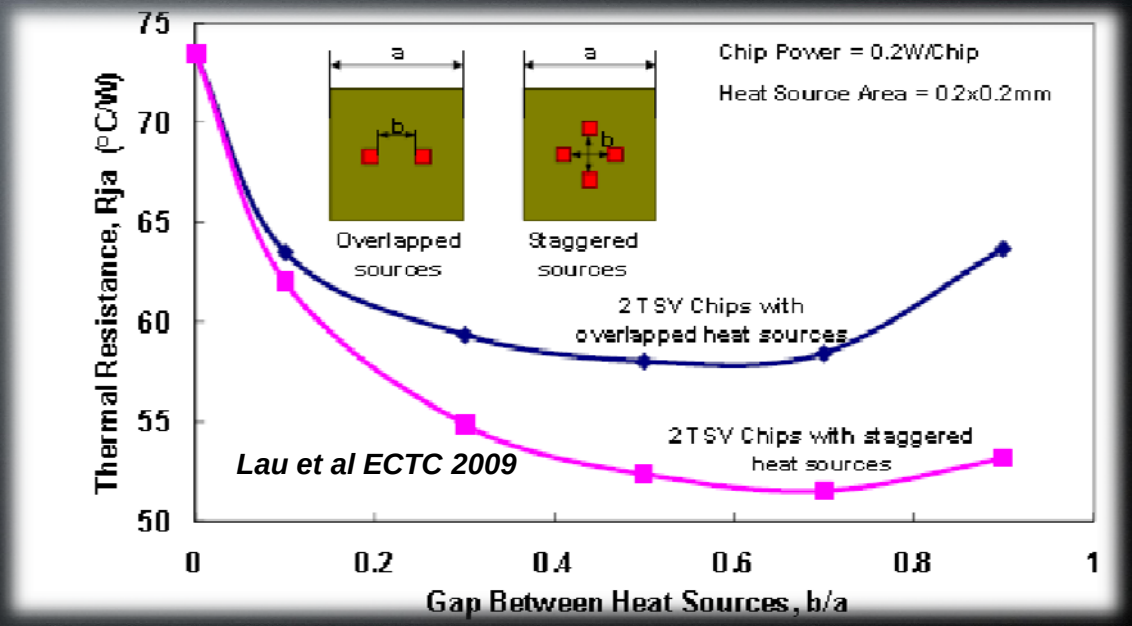
$k_{eq,z} = 150 + 188D^{-2}P^{-2}$; $D = (D1 + D2)/2$; $A = Thickness/D$

Fig. 3 Equivalent thermal conductivity in xy-direction, ($k_{eqx} = k_{eqy}$)

- How thinner can be the die and the TSV without any side impact on the manufacturability of wafer and provoking Joule heat effect

Challenge:

- Re-arrangement hot spot to have the lowest thermal resistance



- What is the impact on the performances

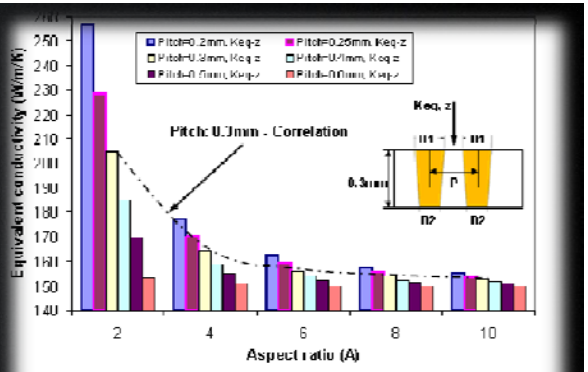
Challenges

- **Technology Modeling**
  - ✓Utilizing TSV to improve Thermal spreading in-plane and through-plane of the die-stack
    - ✓ How much thinner can the die and the TSV become without any side impact on the manufacturability of wafer and provoking Joule heat effect
  - ❖Understanding the Joule heating
    - ❖Impact of lifetime reliability from the current density, as well as the thermo-mechanical stresses when the TSV gets thinner
  - ❖Removing the heat dissipation
    - ❖Flow Instabilities Vs Power Map in the real life application
- **Architectural Exploration Analysis Tools**
  - ❖ Impact on the performances as a function of the thermal management and Si architecture
    - ❖Re-arrangement hot spot to have the lowest thermal resistance

Joule Heating

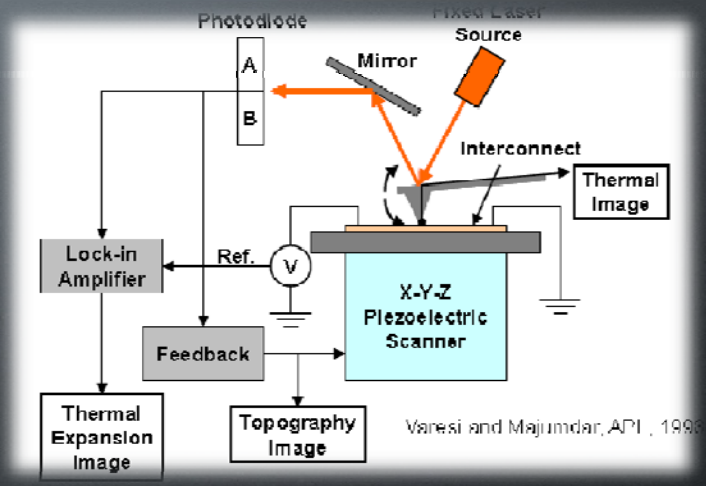
Challenge:

➢Understanding the Current density in a real application when the TSV getting thinner and thinner

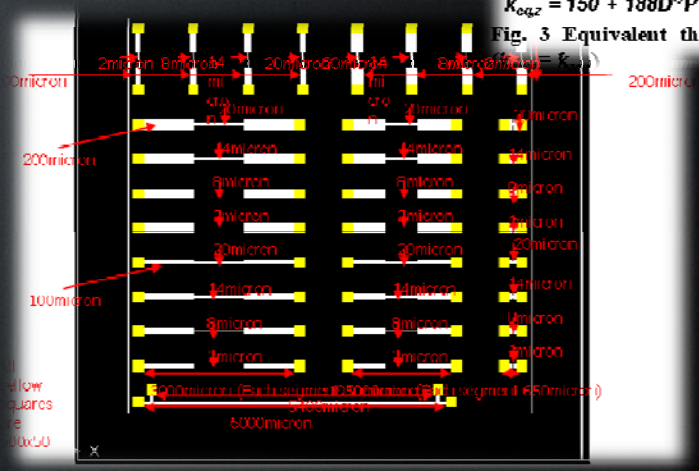


$k_{eq,z} = 150 + 188D^{-2}P^{-2}$; $D = (D1 + D2)/2$; $A = Thickness/D$

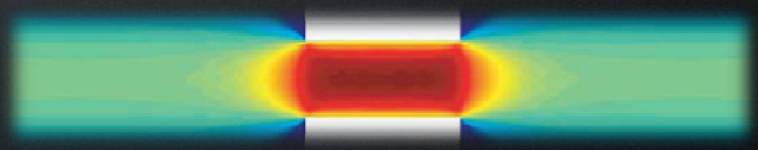
Fig. 3 Equivalent thermal conductivity in xy-direction.



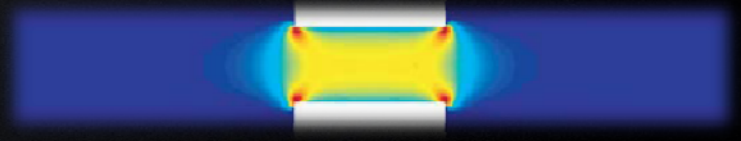
Scanning Joule Expansion Microscopy
Yogendra Task 1292.006



Sample used in Yogendra Task 1829.001



Current Image

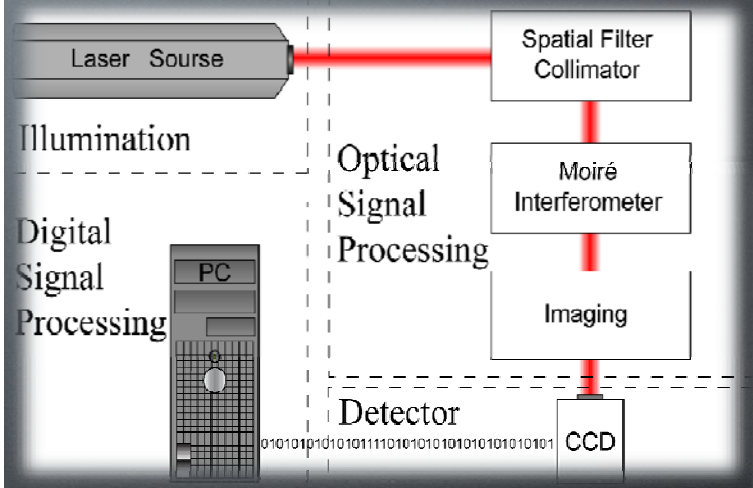


Thermal Image

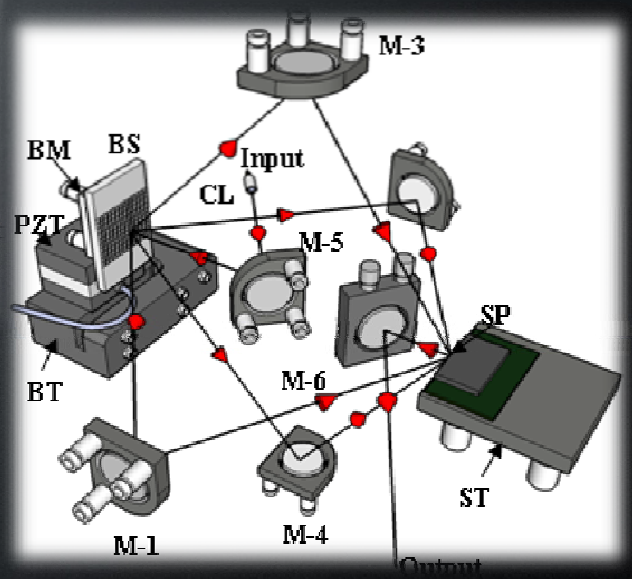
The future is fusion

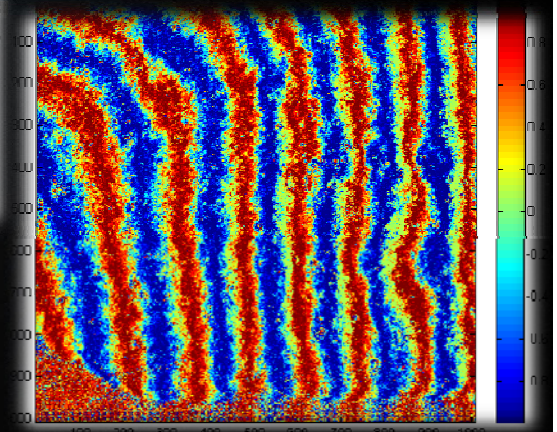
Joule Heating

>Understanding the Impact of Current density without any destruction



Moiré Interferometer System



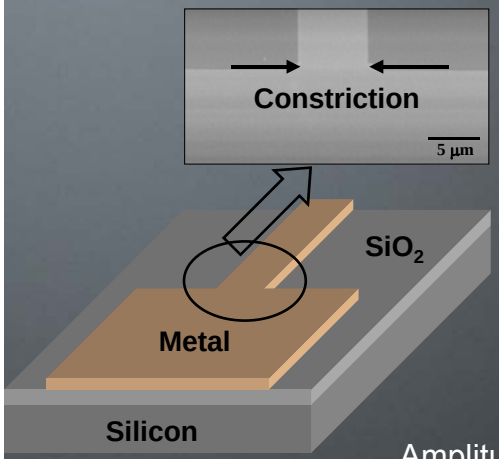


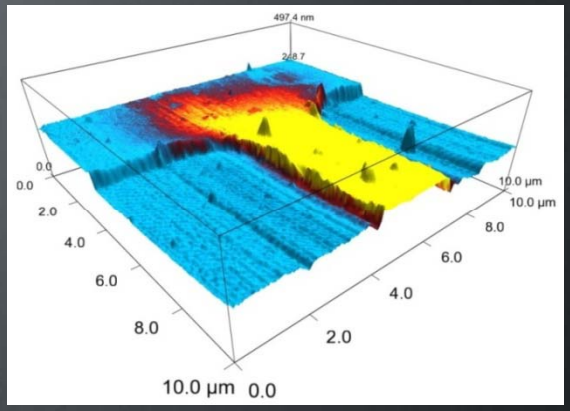
Basaran's Research Team in SUNY Buffalo, 2008

Sample of approx 18 gauge wire with 20A

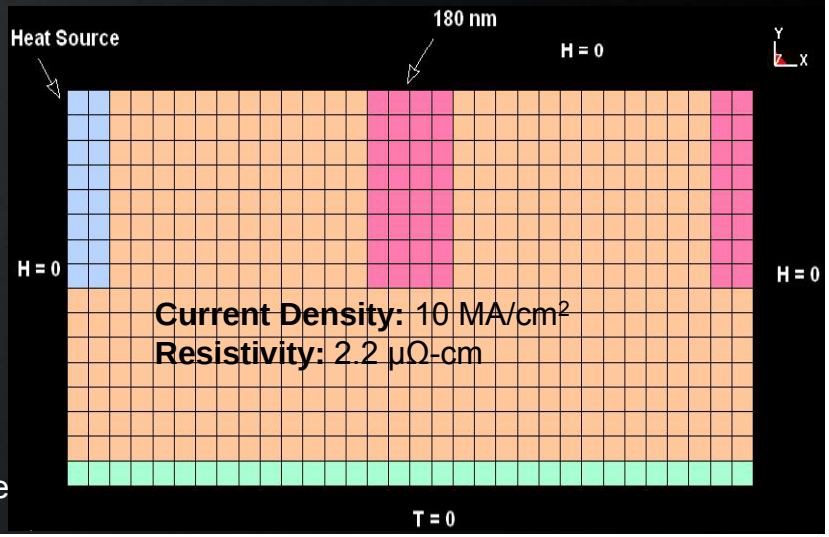
The future is fusion

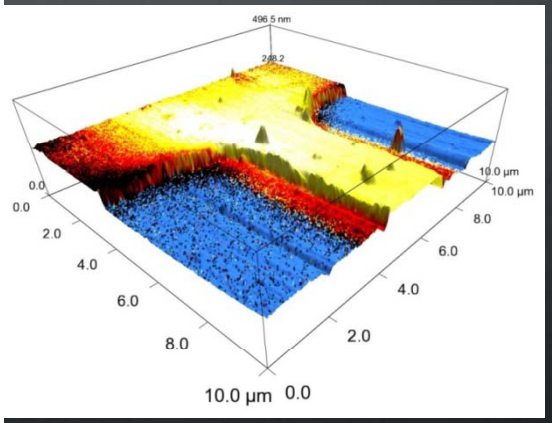
Joule Heating Impact: Reliability & Thermal Management

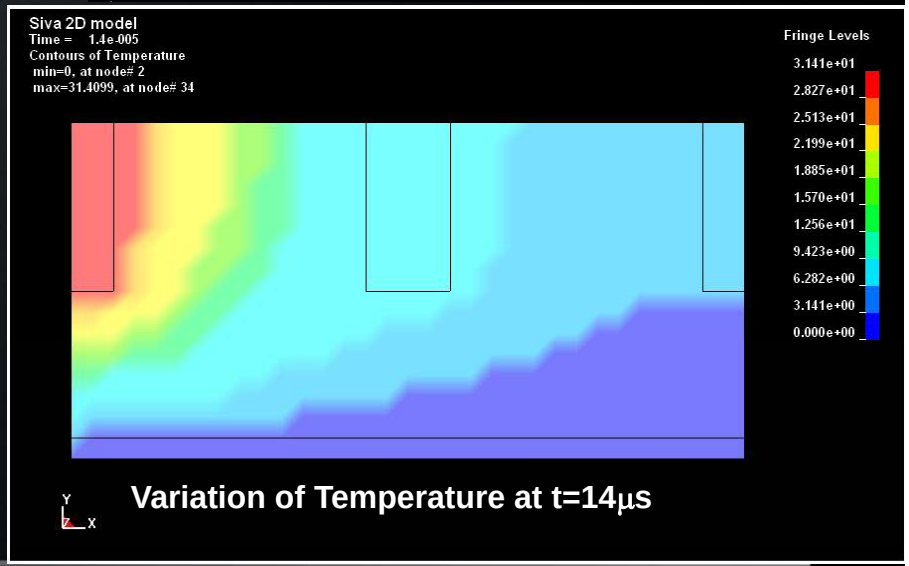




Amplitude (Top) and Phase (Bottom) SJEM Image







Variation of Temperature at t=14µs

Yogendra K. Joshi, Task 1881.005
Barabadi et al IMECE 2009

The Small Scale Systems Integration and Packaging Center BINGHAMTON UNIVERSITY

AMD The future is fusion

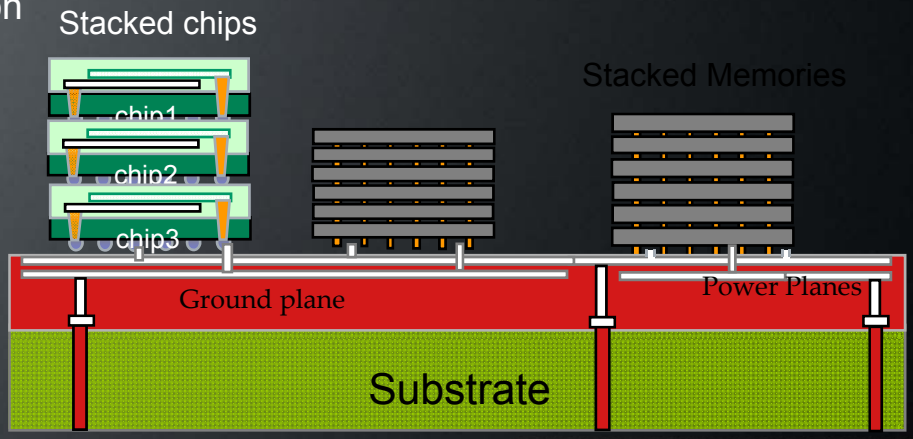
Challenges

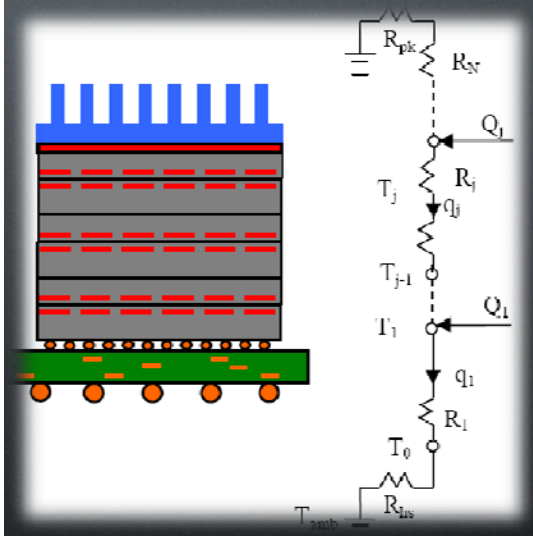
- **Technology Modeling**
  - ✓Utilizing TSV to improve Thermal spreading in-plane and through-plane of the die-stack
    - ✓ How much thinner can the die and the TSV become without any side impact on the manufacturability of wafer and provoking Joule heat effect
  - ✓Understanding the Joule heating
    - ✓Impact of lifetime reliability from the current density, as well as the thermo-mechanical stresses when the TSV gets thinner
  - ❖Removing the heat dissipation
    - ❖Flow Instabilities Vs Power Map in the real life application
- **Architectural Exploration Analysis Tools**
  - ❖ Impact on the performances as a function of the thermal management and Si architecture
    - ❖Re-arrangement hot spot to have the lowest thermal resistance

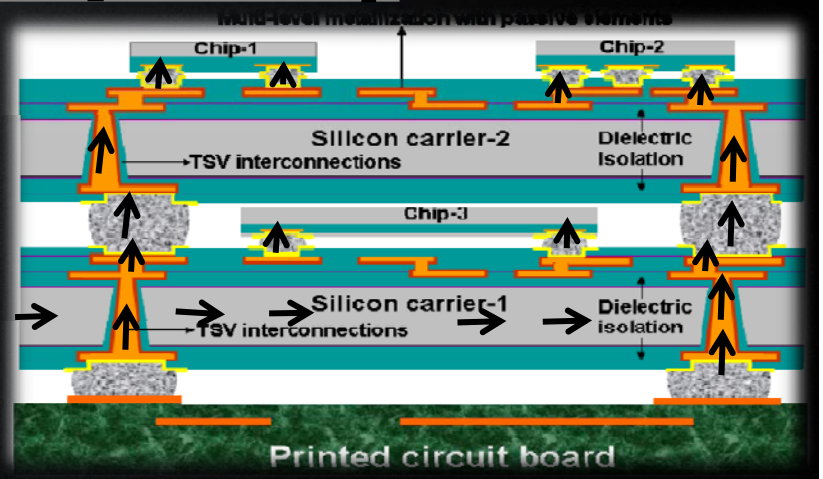
Extracting the heat outside the Die-stack

Challenge

- Removing the heat dissipation





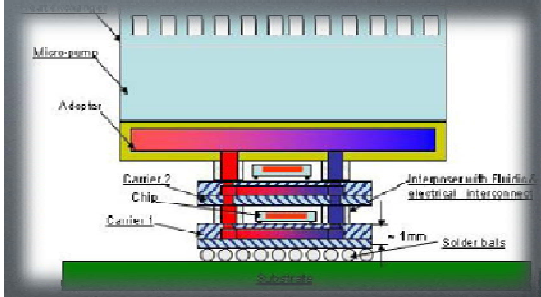


Tan et al 2008 10th EPTC & Swaminathan et al, Georgia Tech 3D workshop, 2009

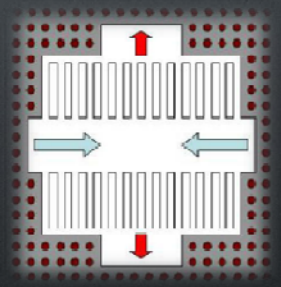
Extracting the heat outside the Die-stack

Challenge

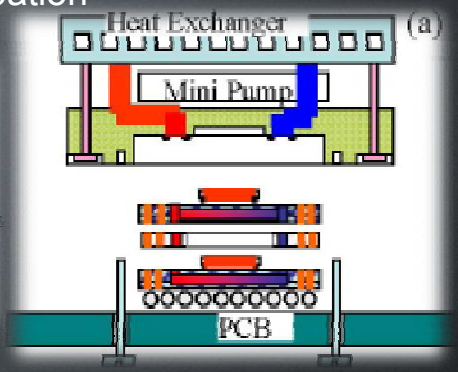
➢Removing the heat dissipation



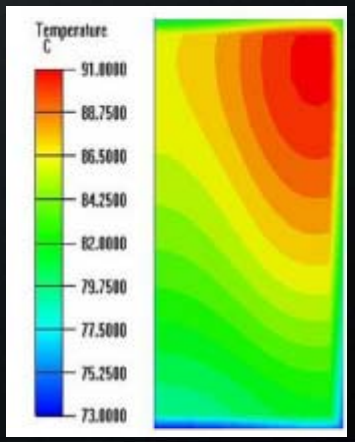
9C temperature variation across the die for 100 W/cm2

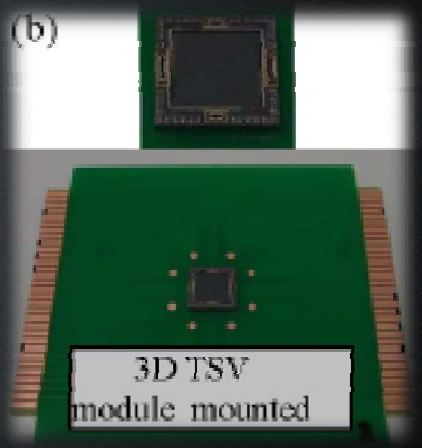


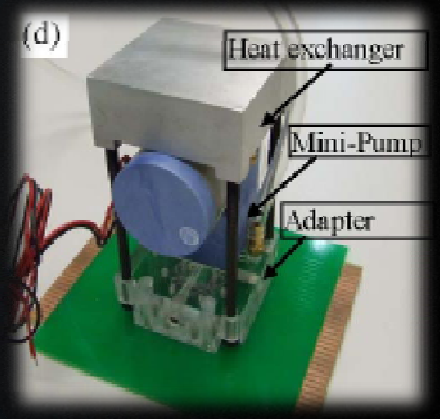
Tan et al 2008 10th EPTC



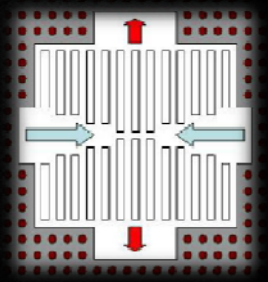
390 ml/min, 17C temperature variation across the die for 100 W/cm2





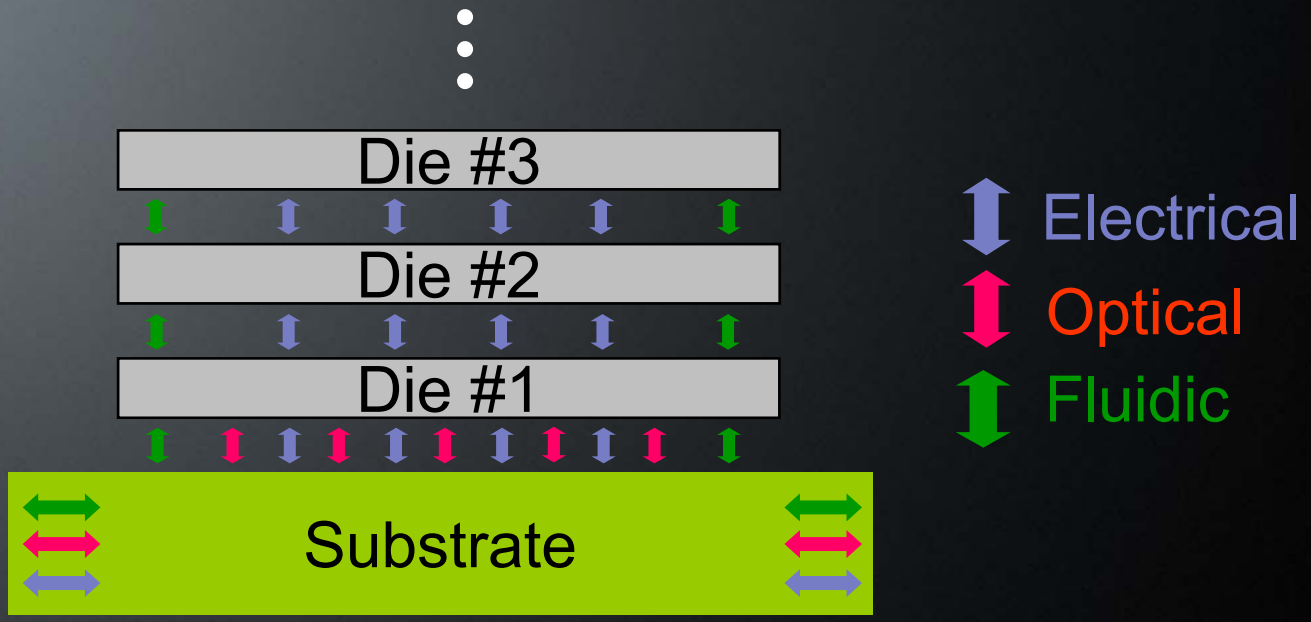


8C temperature variation across the die for 100 W/cm2



The future is fusion

Proposed Approach to IC Interconnection & System Integration



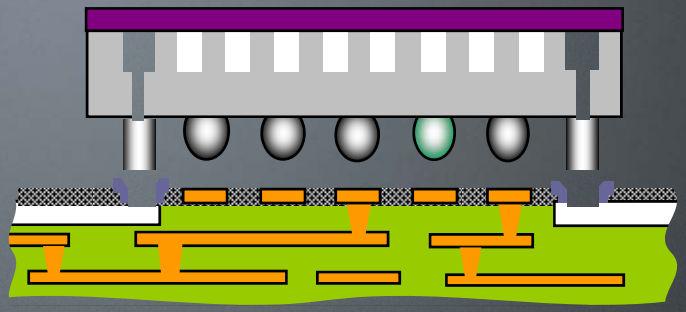
Strategy:

To extend and utilize wafer-scale batch fabrication, key to success of Si technology, to Si ancillary technologies

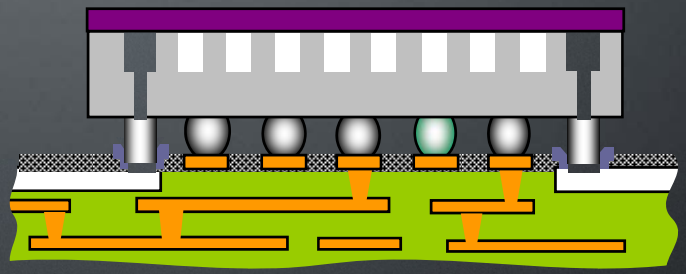
- Electrical I/O: power delivery and signaling
- Optical I/O: massive off-chip bandwidth
- Fluidic I/O: heat removal

Bakir, Georgia Tech, IFC 2009

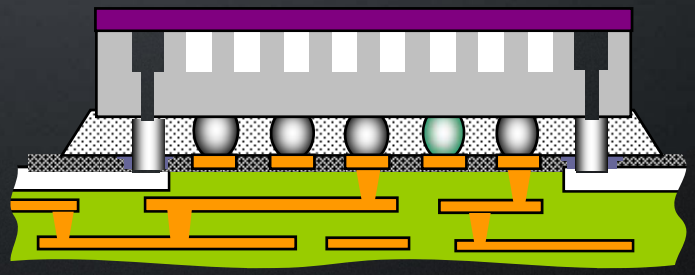
Novel Integration of IC Liquid Cooling Technology



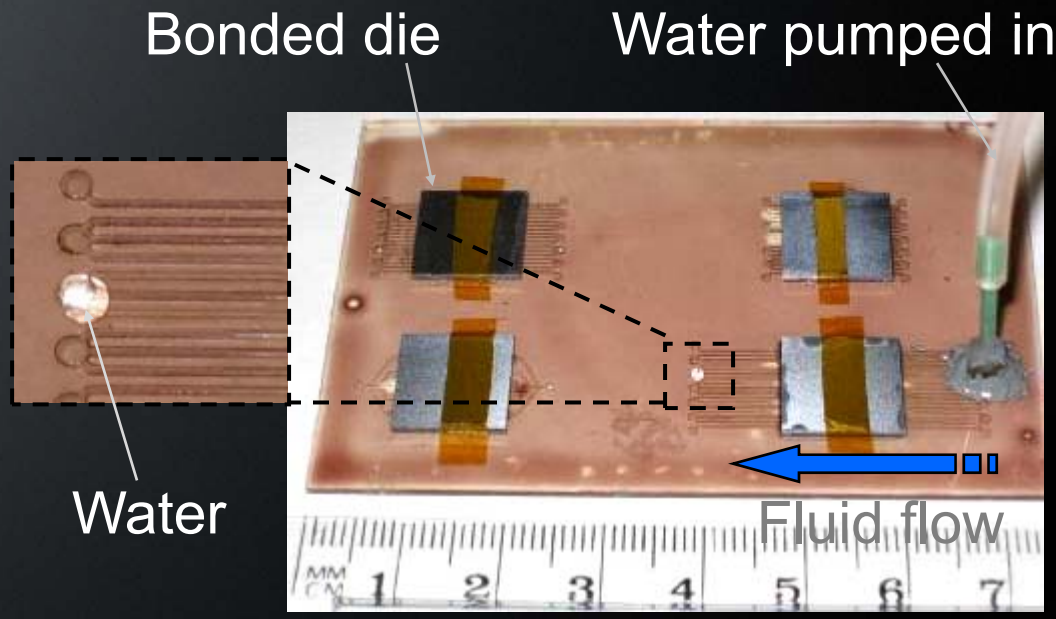
(a) Align



(b) Assemble



(c) Encapsulate

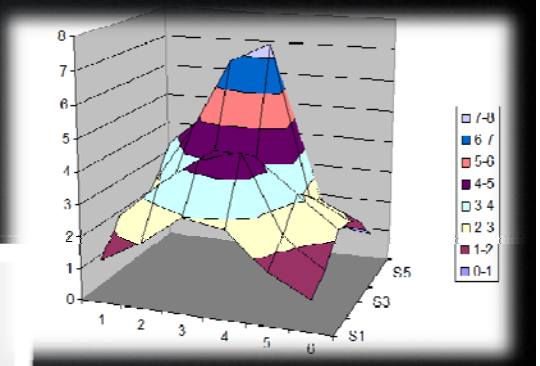


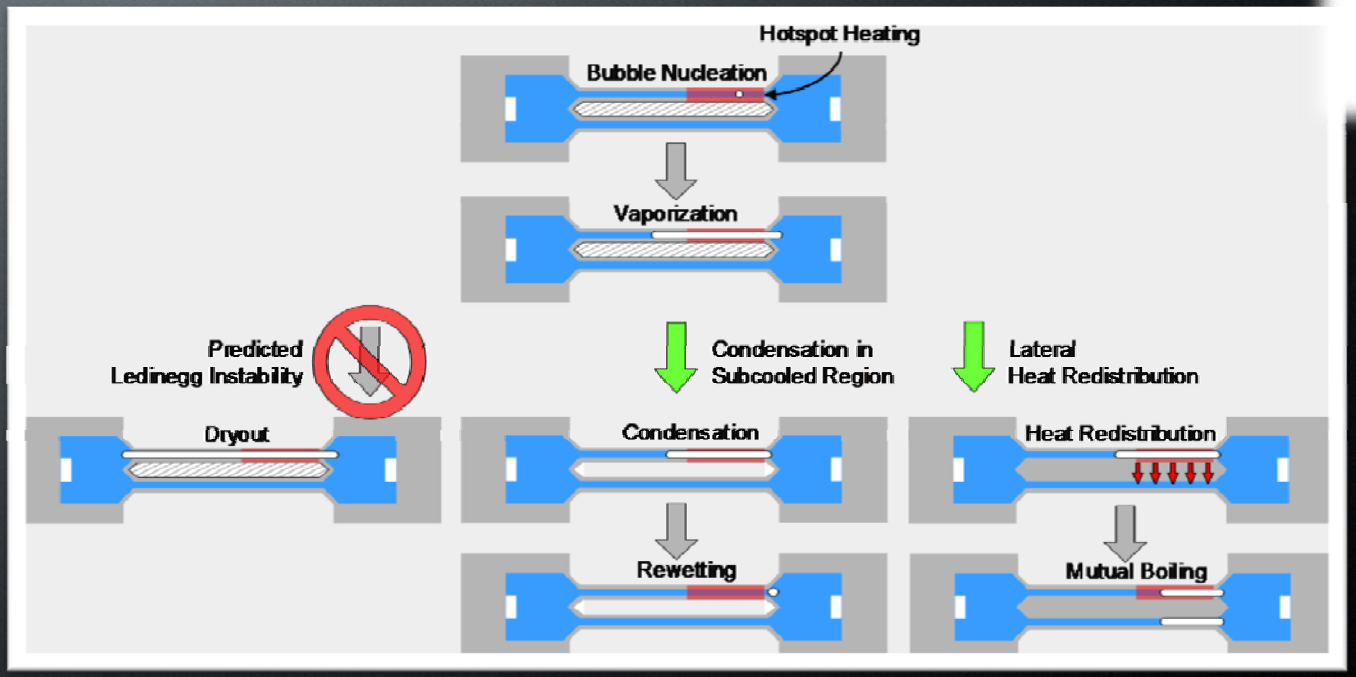
Bakir, Georgia Tech, IFC 2009

Extracting the heat outside the Die-stacking

Challenge

- Flow Instabilities Vs Power Map in the real life application





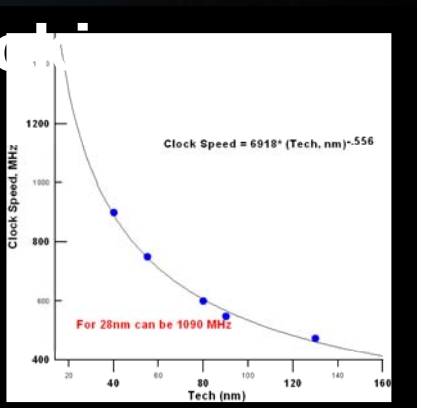
Goodson's Task 1445.001
Miller et al 2009 Ipack

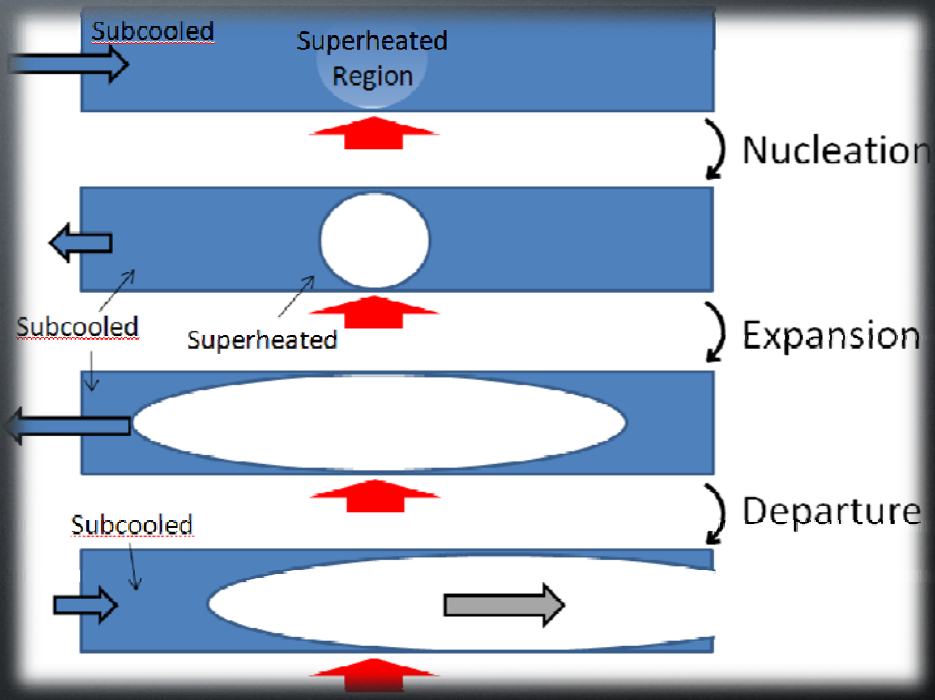
The future is fusion

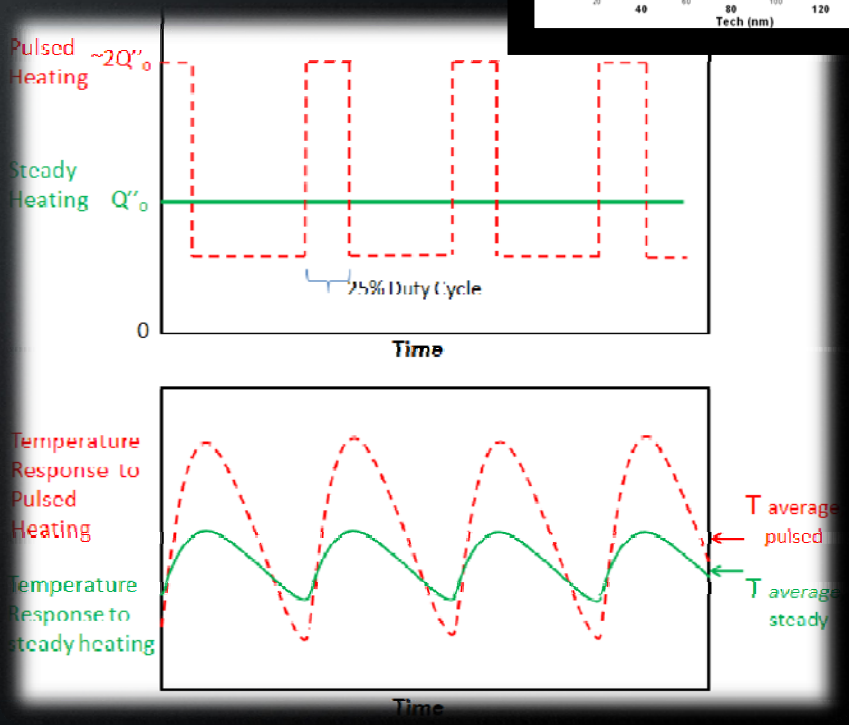
Extracting the heat outside the Die-stac

Challenge

- **Pulsed Heating**







Goodson's Task 1445.001

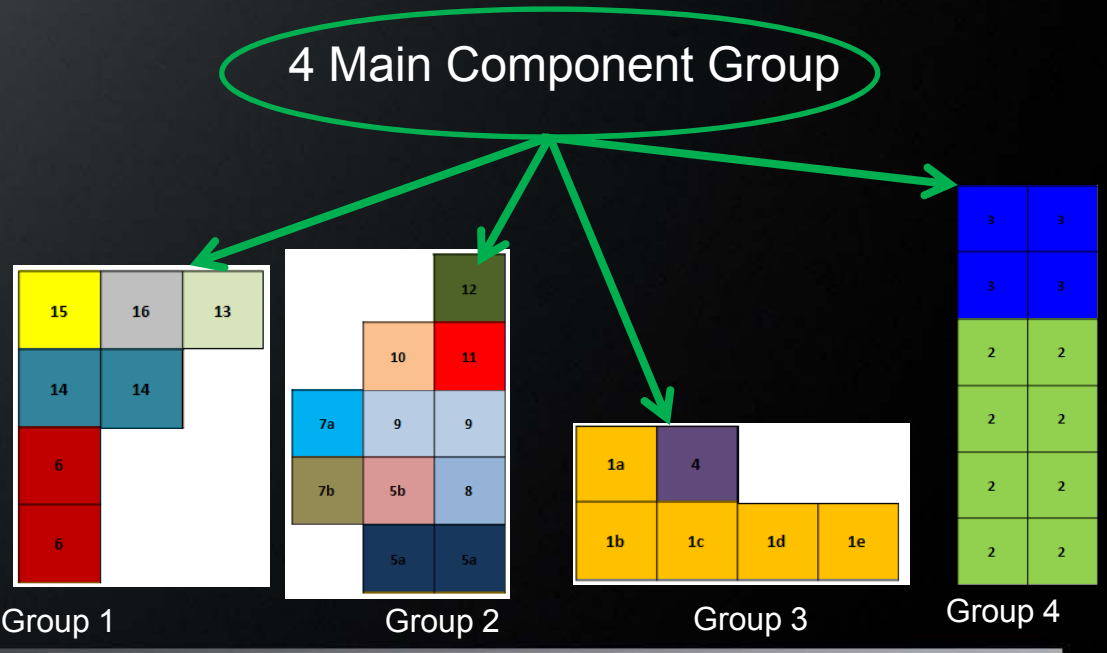
Schematic of applied heating signals and

Challenges

- ✓**Technology Modeling**
  - ✓Utilizing TSV to improve Thermal spreading in-plane and through-plane of the die-stack
    - ✓ How much thinner can the die and the TSV become without any side impact on the manufacturability of wafer and provoking Joule heat effect
  - ✓Understanding the Joule heating
    - ✓Impact of lifetime reliability from the current density, as well as the thermo-mechanical stresses when the TSV gets thinner
  - ✓Removing the heat dissipation
    - ✓Flow Instabilities Vs Power Map in the real life application
- ❑**Architectural Exploration Analysis Tools**
  - ❖ Impact on the performances as a function of the thermal management and Si architecture
    - ❖Re-arrangement hot spot to have the lowest thermal resistance

Penalty on Performance*

Group	Blocks	Penalty (%)
1	15 and 16	4
	15 and 14	4
	6 and 14	3
	7a and 7b	8
2	5a and 5b	11
	5b and 8	5
	9, 10 and 11	6
3	No serious performance loss	<2
4	2 and 3	18



Ghose et al SRC 1292.053

Karajgikar et al Ipack 2009

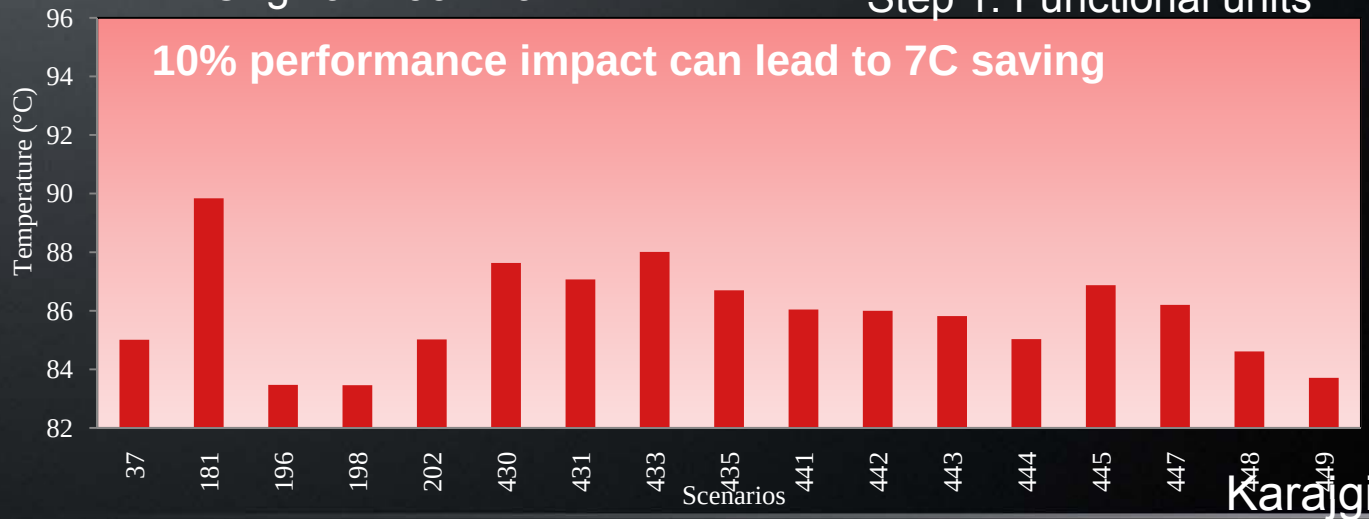
AMD The future is fusion

Challenge:

- What is the impact on the performance

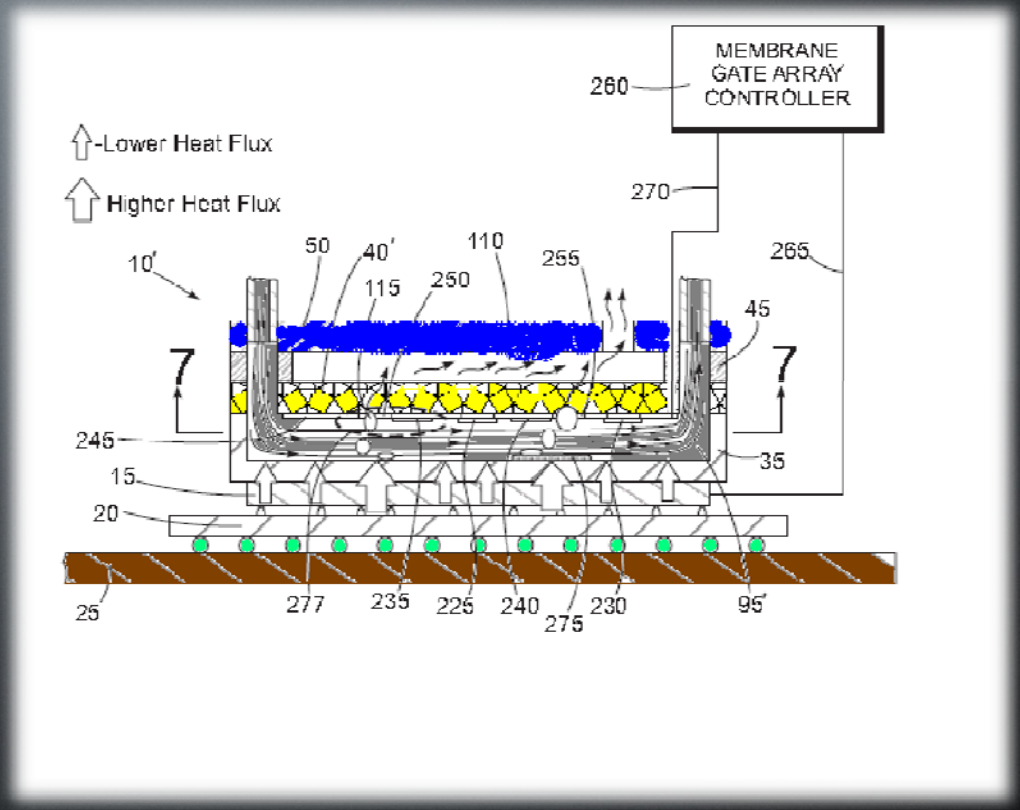
Original Floor Plan

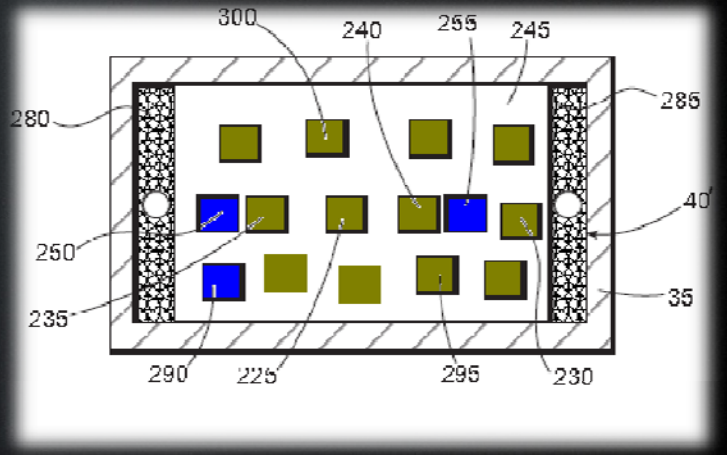
Step 1: Functional units

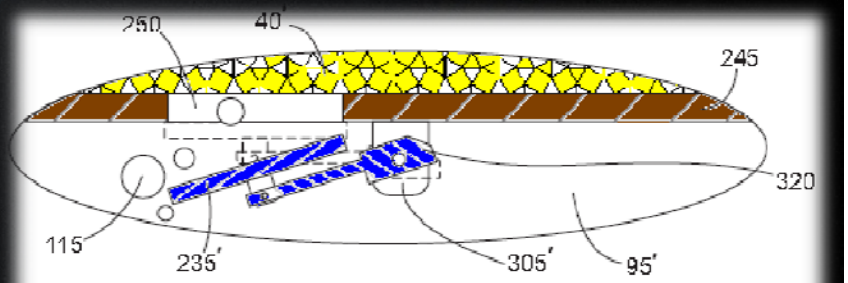


Karajgikar et al Ipack 2009

Dynamic Control for Hot Spot Removal

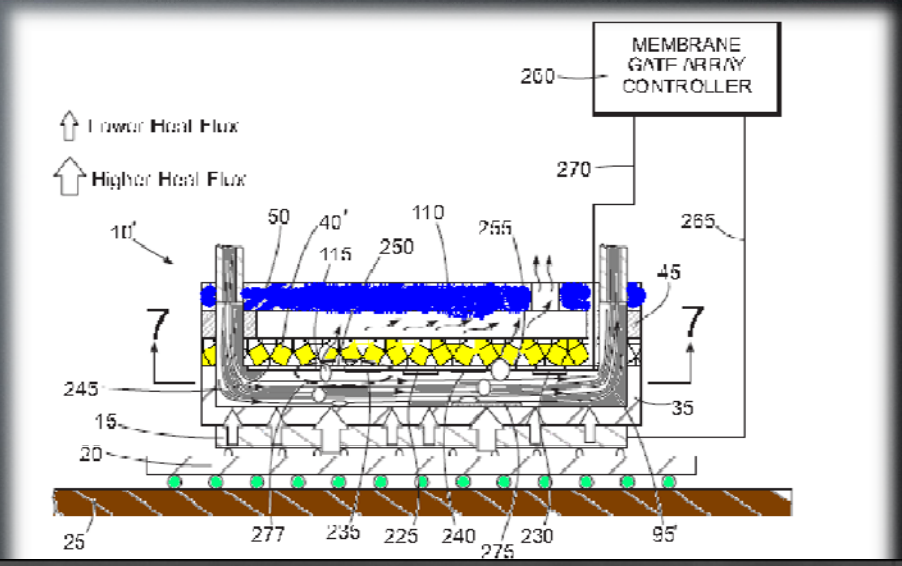


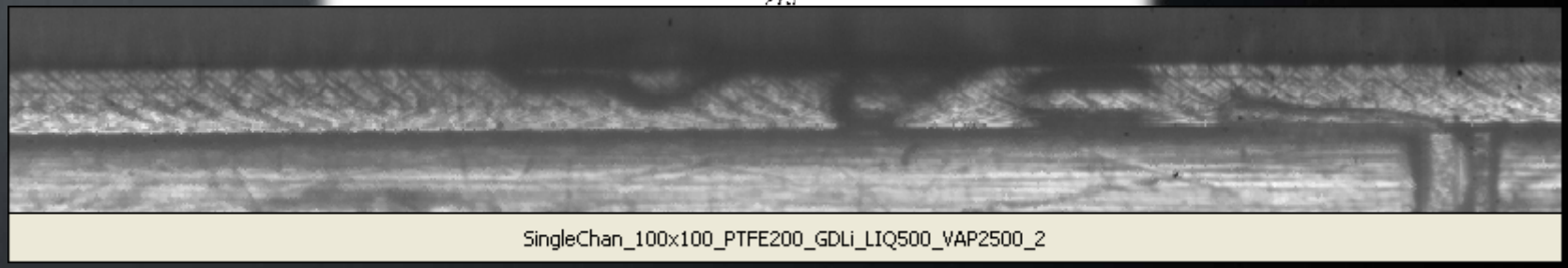




Refai-Ahmed and Goodson's Team in Stanford Univ, SRC 1455.001, US Patent Application 2009

Dynamic Control for Hot Spot Removal





SingleChan_100x100_PTFE200_GDLi_LIQ500_VAP2500_2

Refai-Ahmed and Goodson's Team in Stanford Univ, SRC 1455.001, US Patent Application 2009

Outline

- Definition of the challenges
- Identified Thermal issues
- Final Remarks

Final Remarks:

- 3D can extend Moore's Law beyond the interconnect limitations in 2D present technology, but requires advances in reduced cost, increased power dissipation and heterogeneous integration not being pursued in the IFC – has impact < 5 years, requires collaboration with design.
- 3D can provide enabling improvements for SIP, heterogeneous integration, form factor and package cost. Major research needs, include low T bonding and 3D reliability. Has major impact < 5 years
- There is a need to expand the funding level on the technology modeling and exploring architecture exploration analysis tool
- There is a need to establish synergy between Design and Packing Thrust areas to deliver mature 3D-die stack on time

Disclaimer and Attribution

DISCLAIMER

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions and typographical errors.

The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. AMD and BU assume no obligation to update or otherwise correct or revise this information. However, AMD and BU reserve the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD and BU to notify any person of such revisions or changes.

AMD and BU MAKE NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE CONTENTS HEREOF AND ASSUMES NO RESPONSIBILITY FOR ANY INACCURACIES, ERRORS OR OMISSIONS THAT MAY APPEAR IN THIS INFORMATION.

AMD and BU SPECIFICALLY DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL AMD and BU BE LIABLE TO ANY PERSON FOR ANY DIRECT, INDIRECT, SPECIAL OR OTHER CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF ANY INFORMATION CONTAINED HEREIN, EVEN IF AMD AND BU ARE EXPRESSLY ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TRADEMARK ATTRIBUTION

© 2009 Advanced Micro Devices, Inc. All rights reserved. AMD, the AMD Arrow logo, ATI, the ATI logo, and combinations thereof are trademarks of Advanced Micro Devices, Inc. Microsoft, Windows, and Windows Vista are registered trademarks of Microsoft Corporation in the United States and/or other jurisdictions. Other names used in this presentation are for identification purposes only and may be trademarks of their respective owners.

©2009 Advanced Micro Devices, Inc. All rights reserved.

What We Face in Life can the Electrons Face it?