# Taller vs. Smaller:

## 3D Development & Moore's Law

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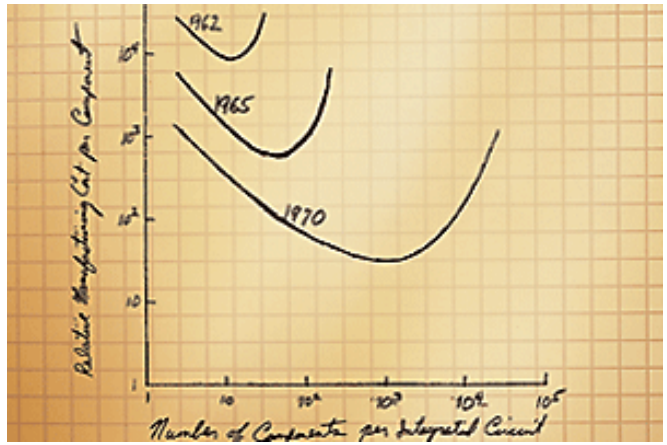
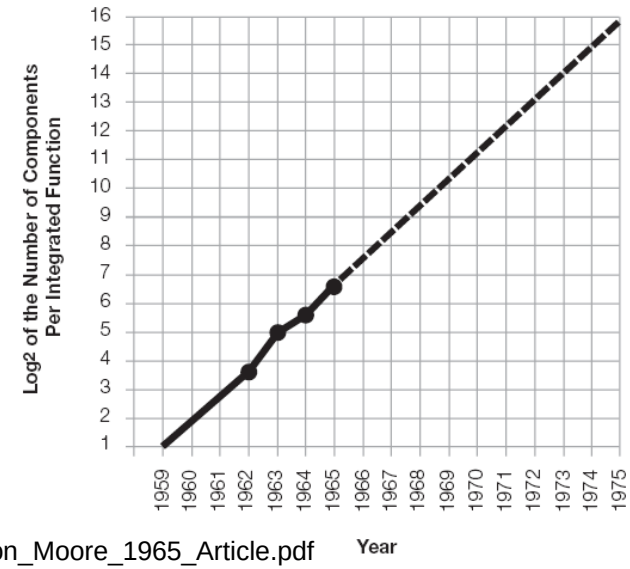
**GRC ETAB Summer Study**
**La Quinta, CA**
**June 30, 2009**

# Moore's Law

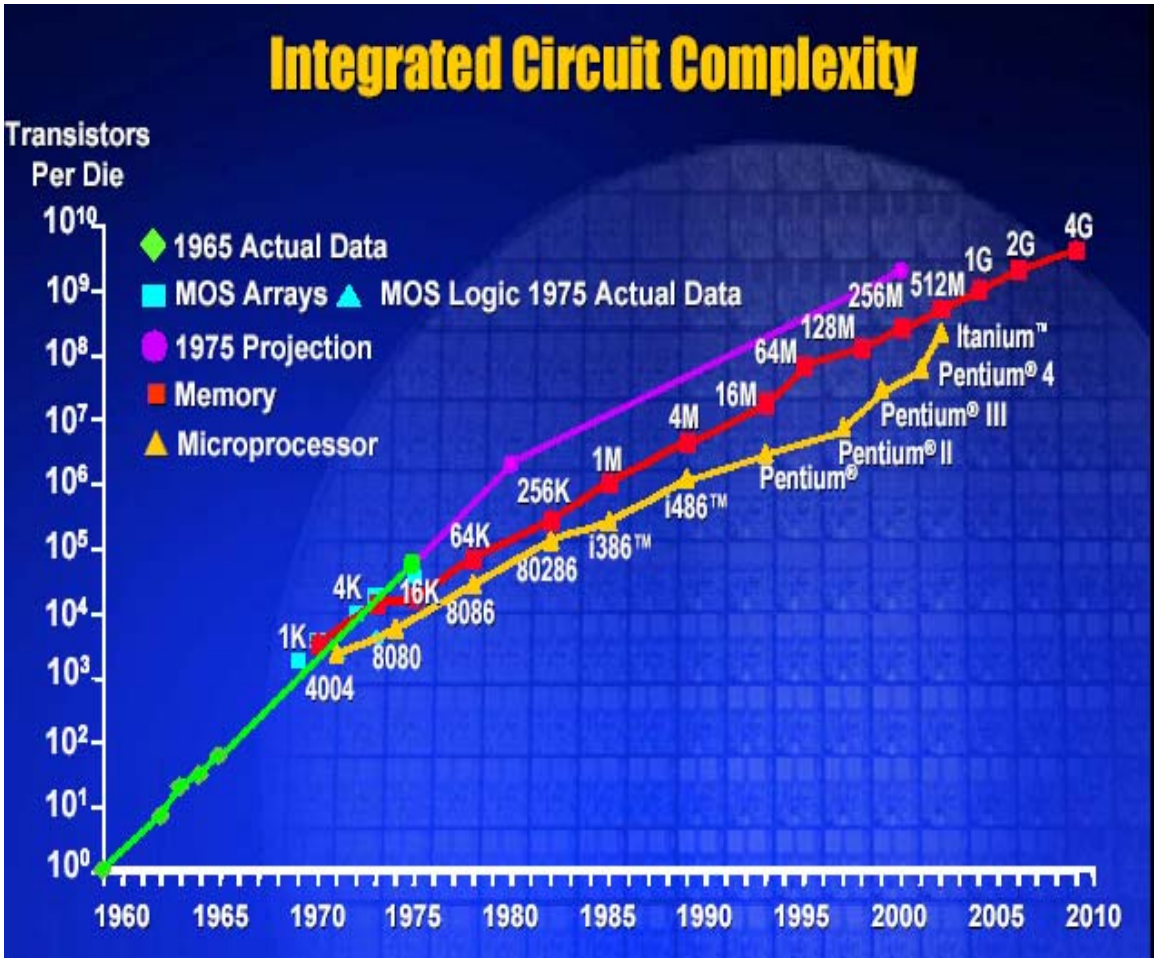
- Famous 1965 article
- Observation on COST
  - Cost per component decreases with integration
- Number of transistors doubles every 2 years




**Cramming More Components onto Integrated Circuits**
G. Moore, Electronics Vol. 38, pp. 114-117 (1965)
http://download.intel.com/museum/Moores_Law/Articles-Press_Releases/Gordon_Moore_1965_Article.pdf

# Moore's Law

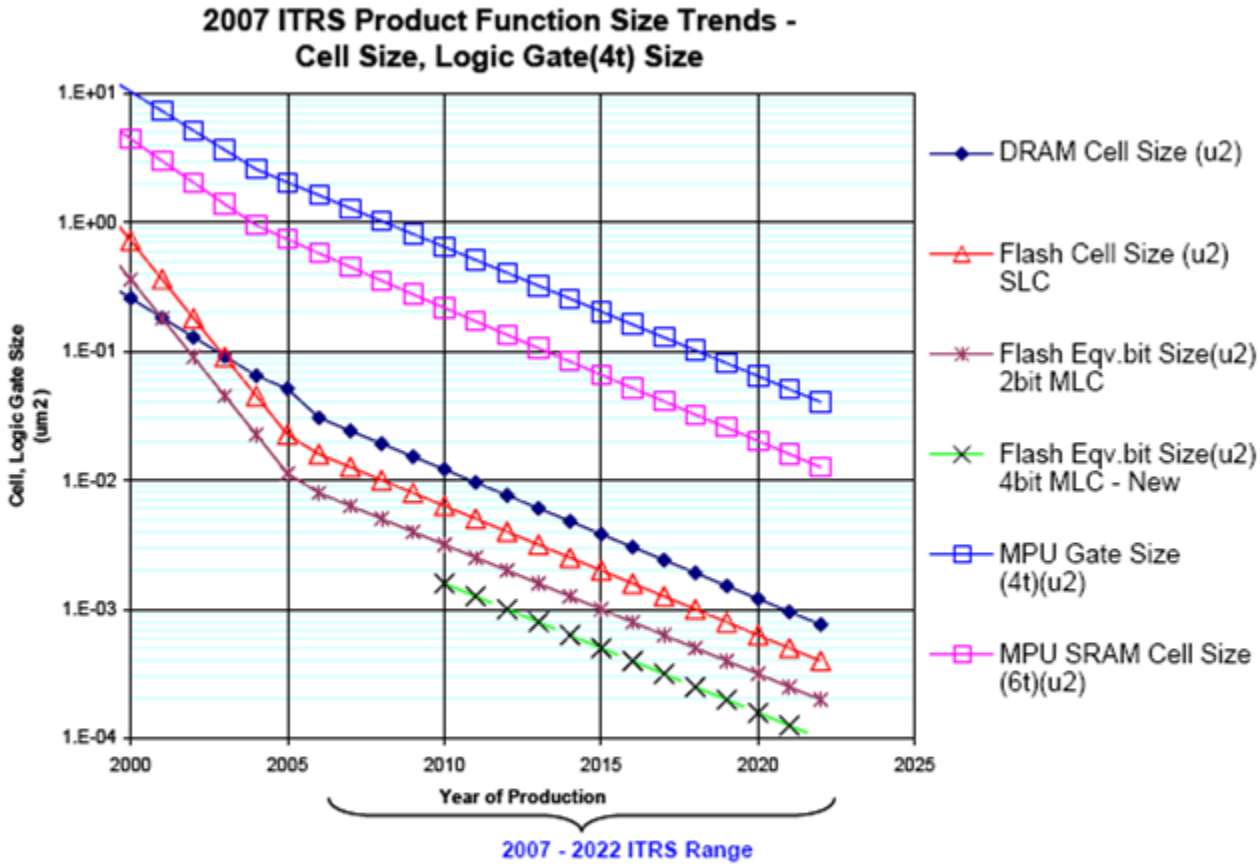



Source: Intel
ftp://download.intel.com/research/silicon/Gordon_Moore_ISSCC_021003.pdf

# Moore's Law

- Achieved by shrinking
  - Smaller feature sizes (linear dimension)
  - Smaller Cell sizes (aerial dimension)
  - "Smaller" Chip sizes (for same function)
    - Improves yield for a fixed wafer size
- Other aspects also shrink
  - Voltage
  - Oxide layers
- All now planned in the ITRS Meetings
  - www.itrs.net

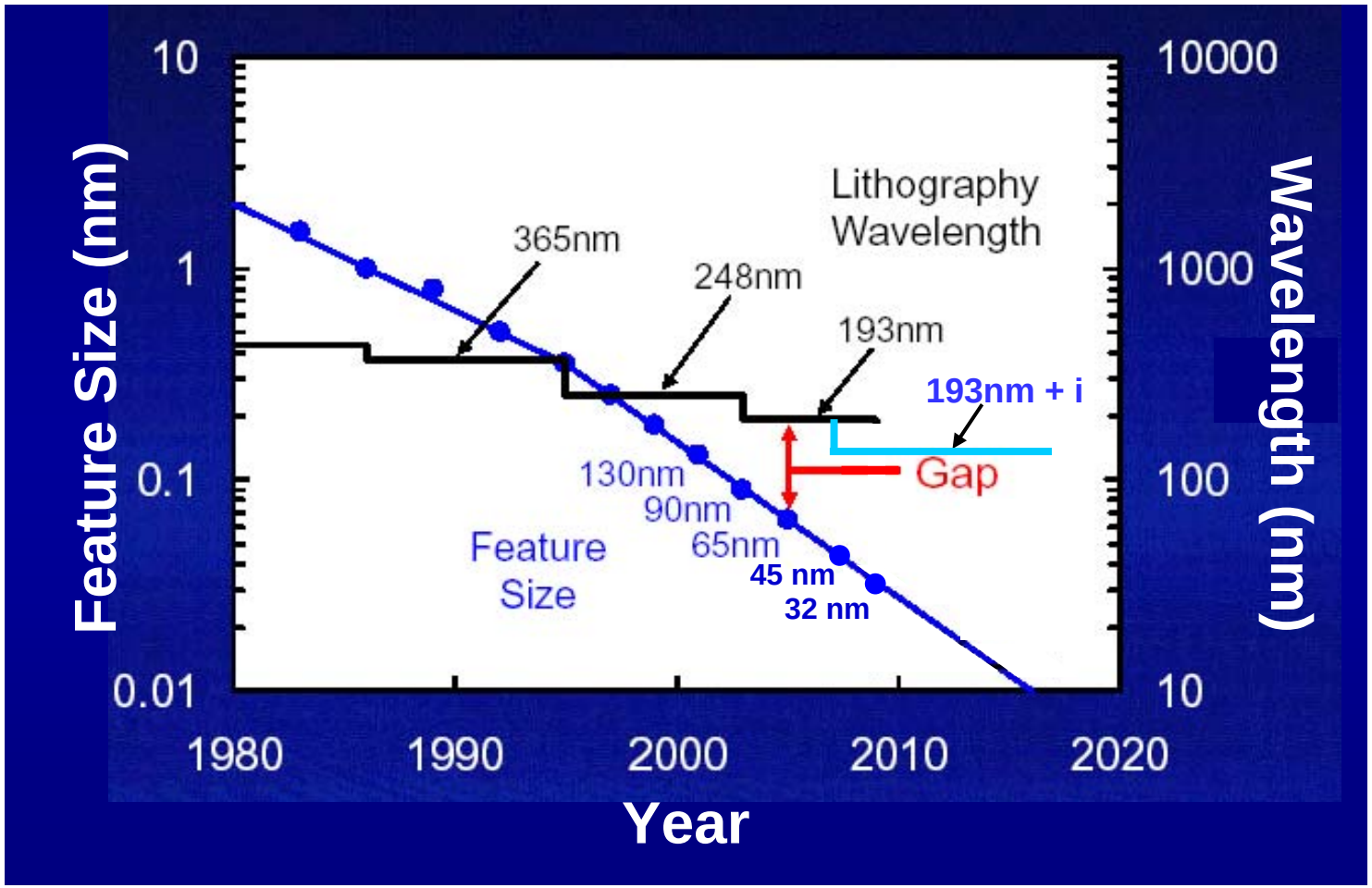
# Moore's Law: ITRS




**ITRS 2008 Update**
**http://www.itrs.net**

*Figure ORTC3 ITRS Product Technology Trends:*
*Product Functions/Chip and Industry Average "Moore's Law" Trends--Updated*

# Moore's Law: Subwavelength




**Adapted from:**
**M. Bohr, http://www.intel.com/technology/silicon/65nm_technology.htm**

# Litho Scaling Gap

- Gap created opportunity
  - Shrinking Paradigm changed
- Emergence of RET
  - Resolution Enhancement Technology
  - Modeling sub-wavelength behavior/distortions
  - Adapting IC Designs/Layouts to compensate
    - OPC
    - Phase Shifting Mask
    - Off-Axis Illumination
    - Immersion (High NA)
    - Double Patterning
    - SMO (source/Mask Optimization)

# RET adds complexity

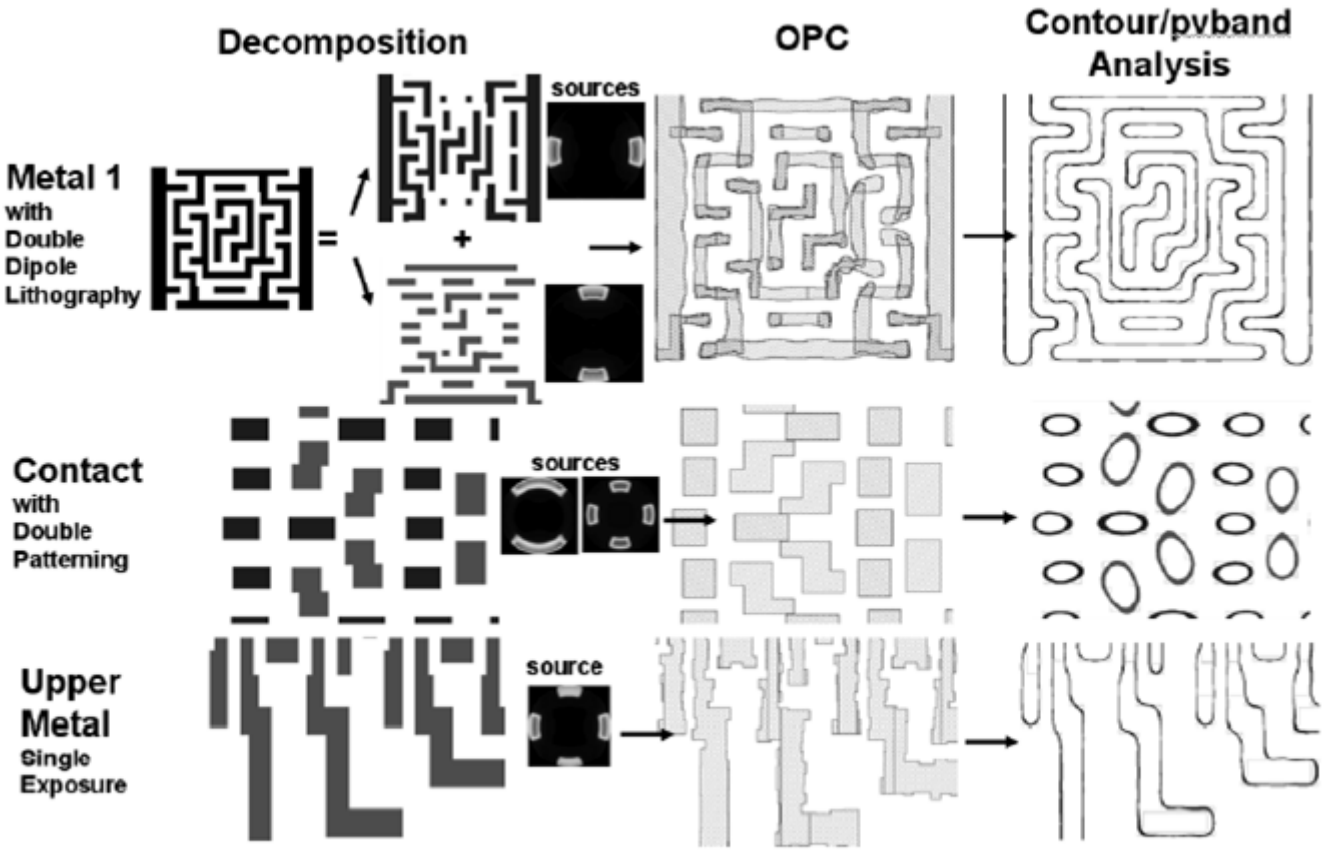
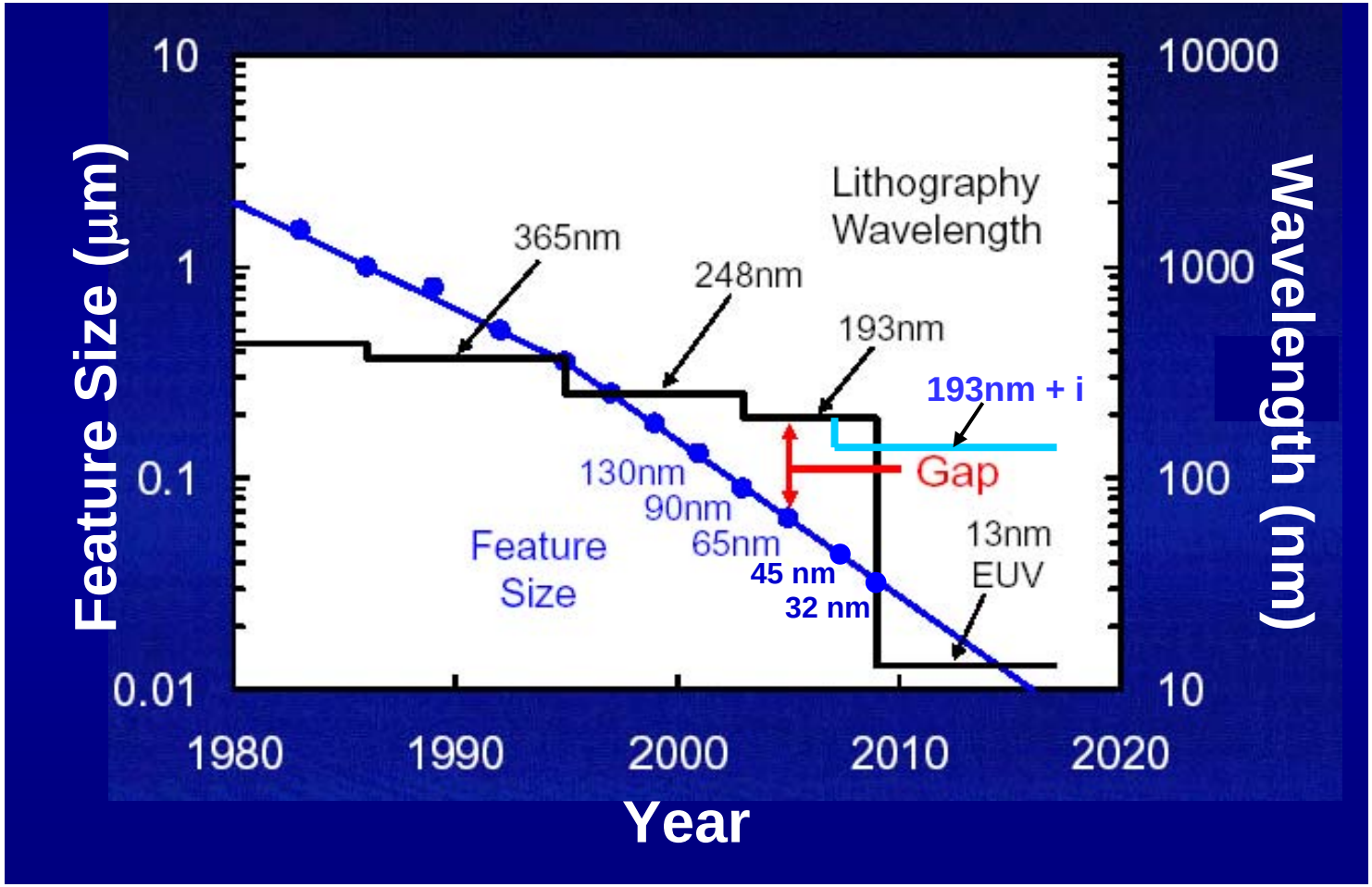



Figure 3. The experimental flow for decomposing, applying OPC, generating post-OPC contours, and analysis is shown. For our experiments, we studied the Metal 1, Contact, and Upper Metal processes.

**Inverse vs. traditional OPC for the 22nm node**
James Word et al.,Mentor Graphics, Proc. SPIE 7274, 72743A (2009)

# Moore's Law

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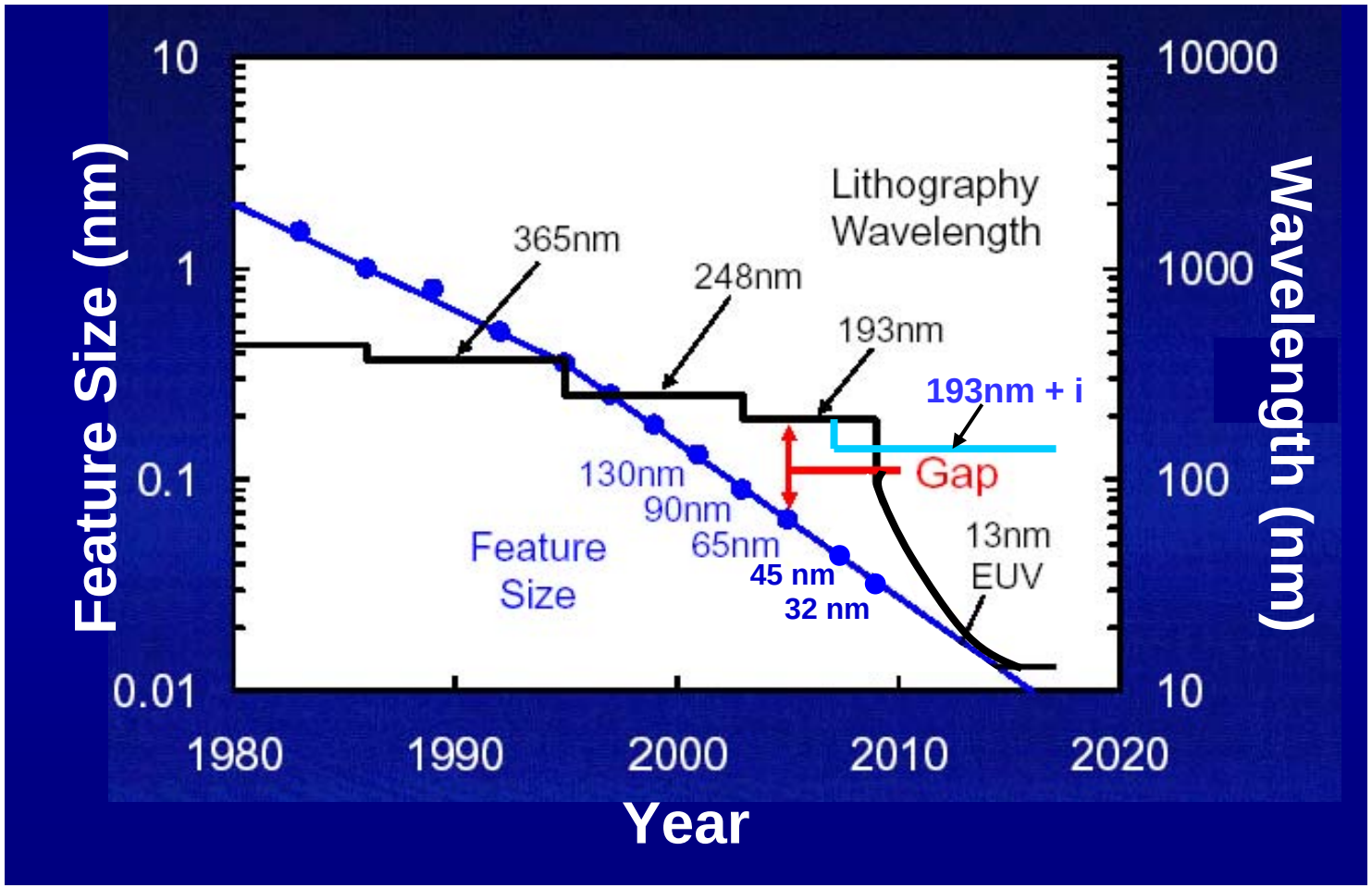
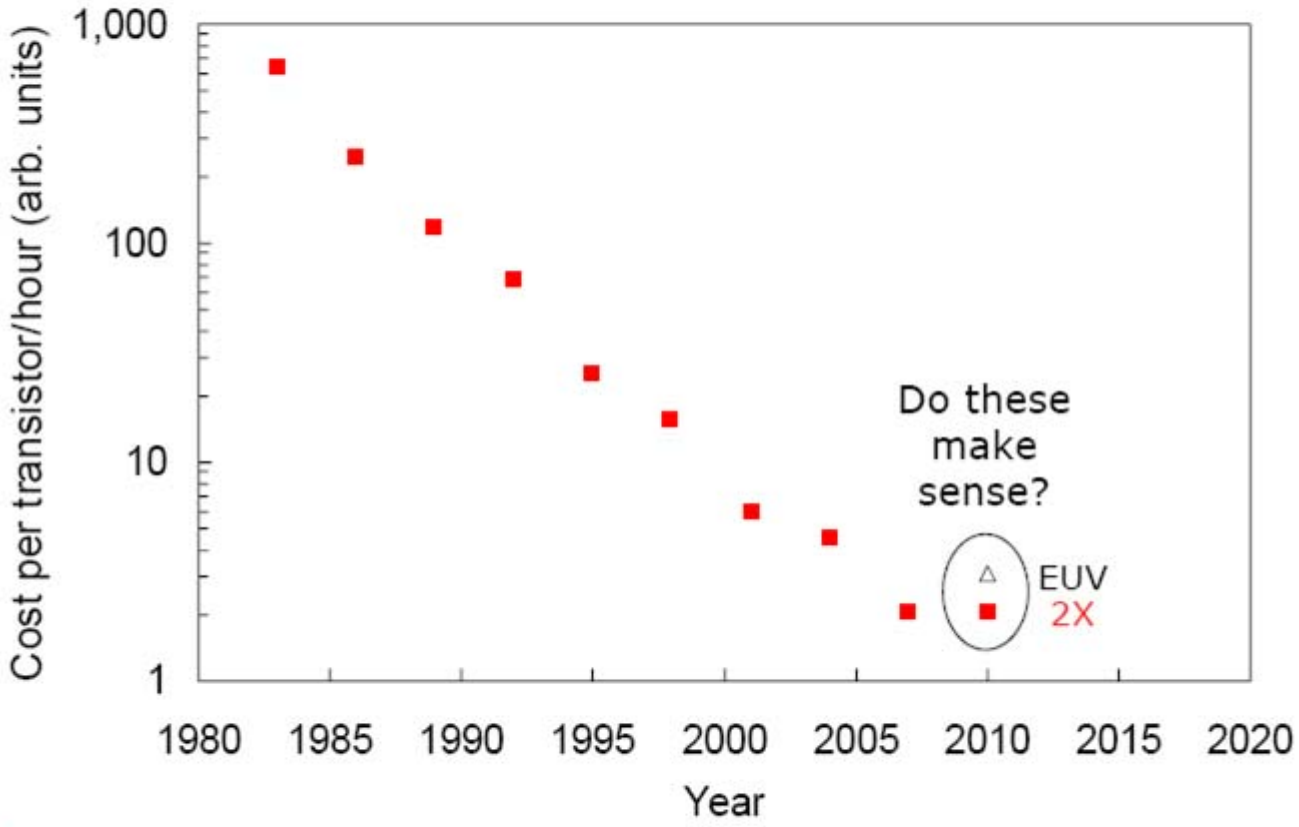



**Adapted from:**
**M. Bohr, http://www.intel.com/technology/silicon/65nm_technology.htm**

# Critical layer capital cost per transistor




18 29 March 2007 Cost and the Future of Lithography

**Source: H. Levinson, SEMI Silicon Valley Lunch Forum, 3-29-2007**
**http://content.semi.org/cms/groups/public/documents/events/p041431.pdf**

# Lessons Learned

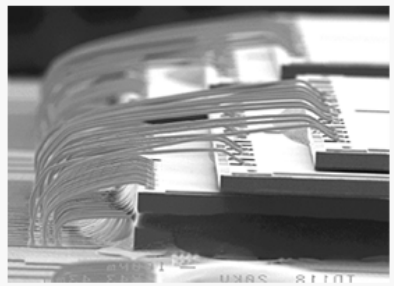
- **Litho scaling running out of steam**
  - **Complexity and Cost problems**
  - ***not*** **technology barriers**
- **The Gap has been filled with Modeling Tools**
  - **RET/DFM Market now ~$500M/ year**
- **Expect more ITRS revisions**
  - **New consumer devices don't need shrinking**
  - **All exponentials eventually end**
- **The End of the Roadmap (as we know it) is near!**

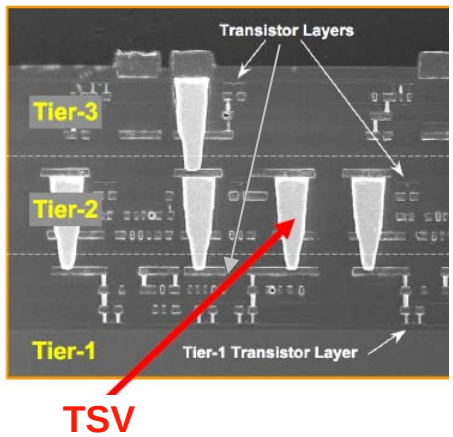
# What's Next

- **Nowhere to go but  UP.**

# Stacking: What can be achieved

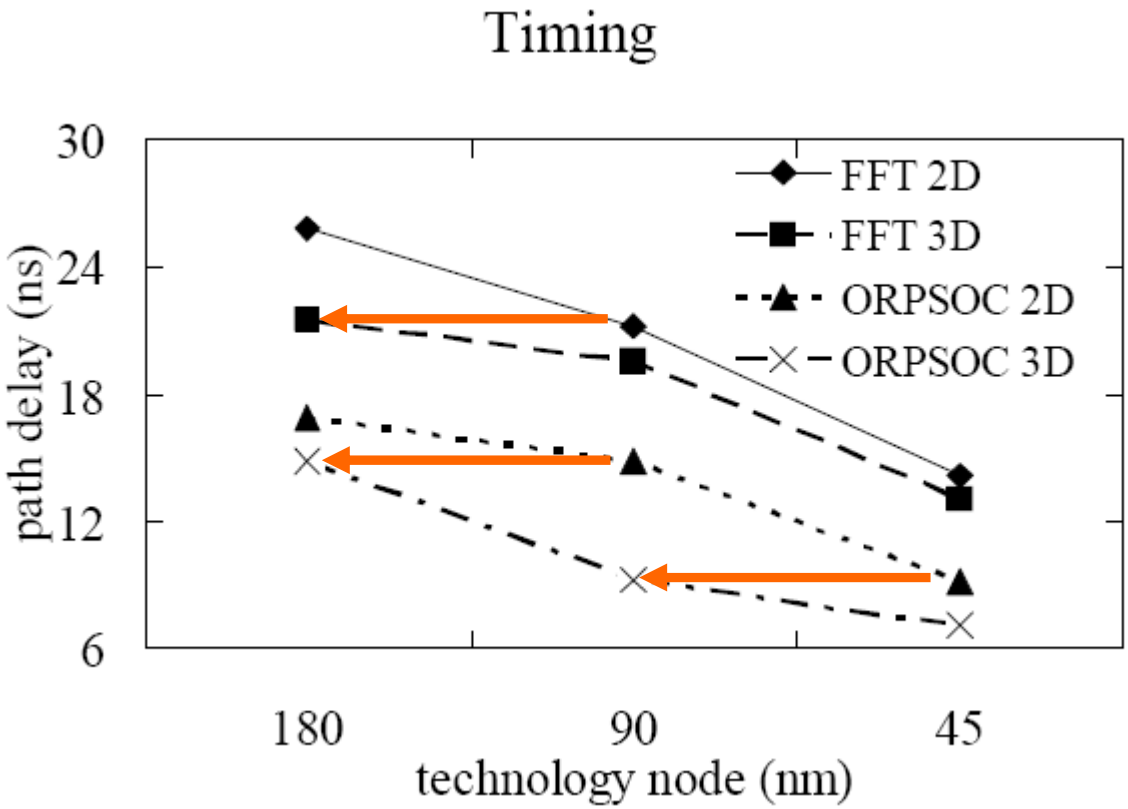
- Stacking creates more functions per $cm^2$
  - High value for cell phones, handheld devices
  - Mix-and-match of established (working) ICs
    - Memory on top of logic
- Up until now, a packaging problem
  - Like a 3-D printed circuit board
  - Wire bonding
  - Flip chips
- Thru Silicon Vias (TSVs) emerged in MEMS
  - Already a long way up the learning curve
  - Shorter wires = faster interconnects
    - Signal never “leaves” the IC
  - Integrated connections = smaller footprint





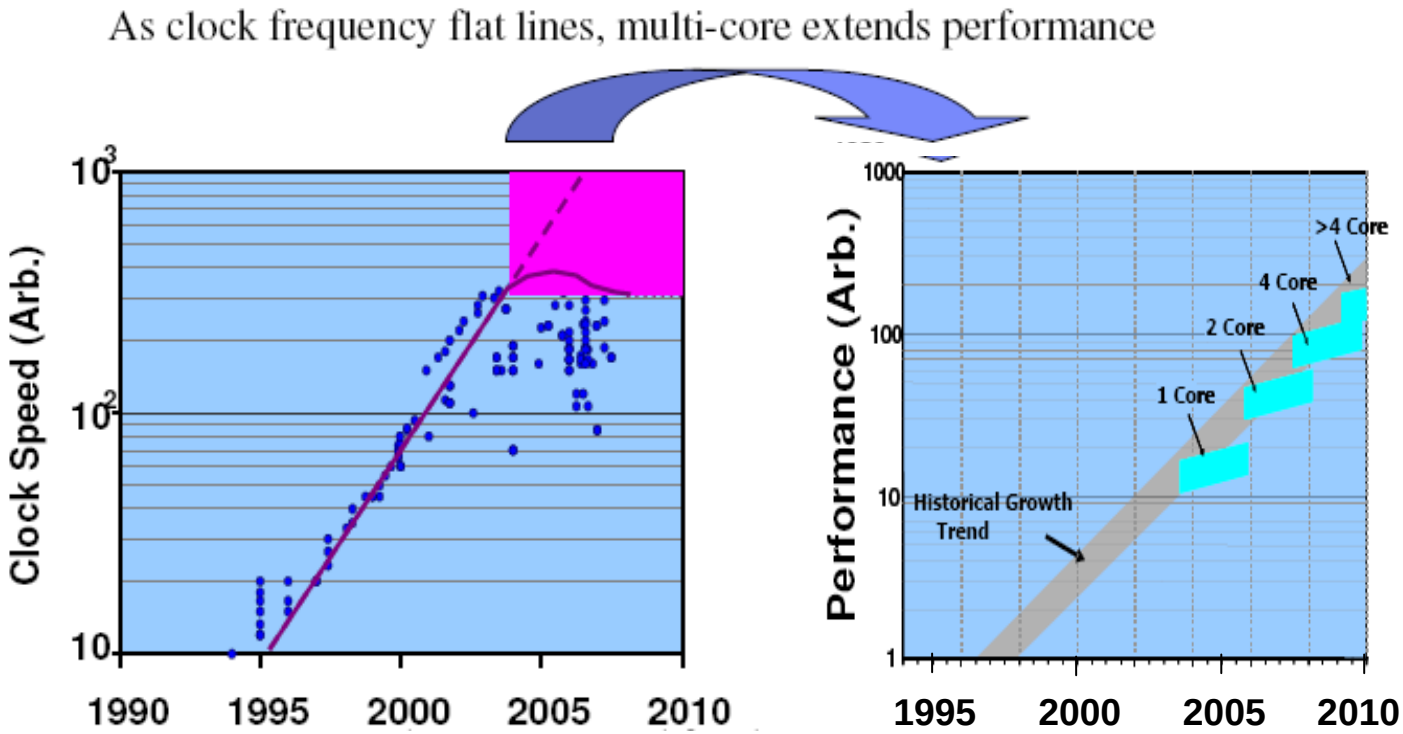
# Stacking improves performance

- **"Stacking buys you 2 nodes"**



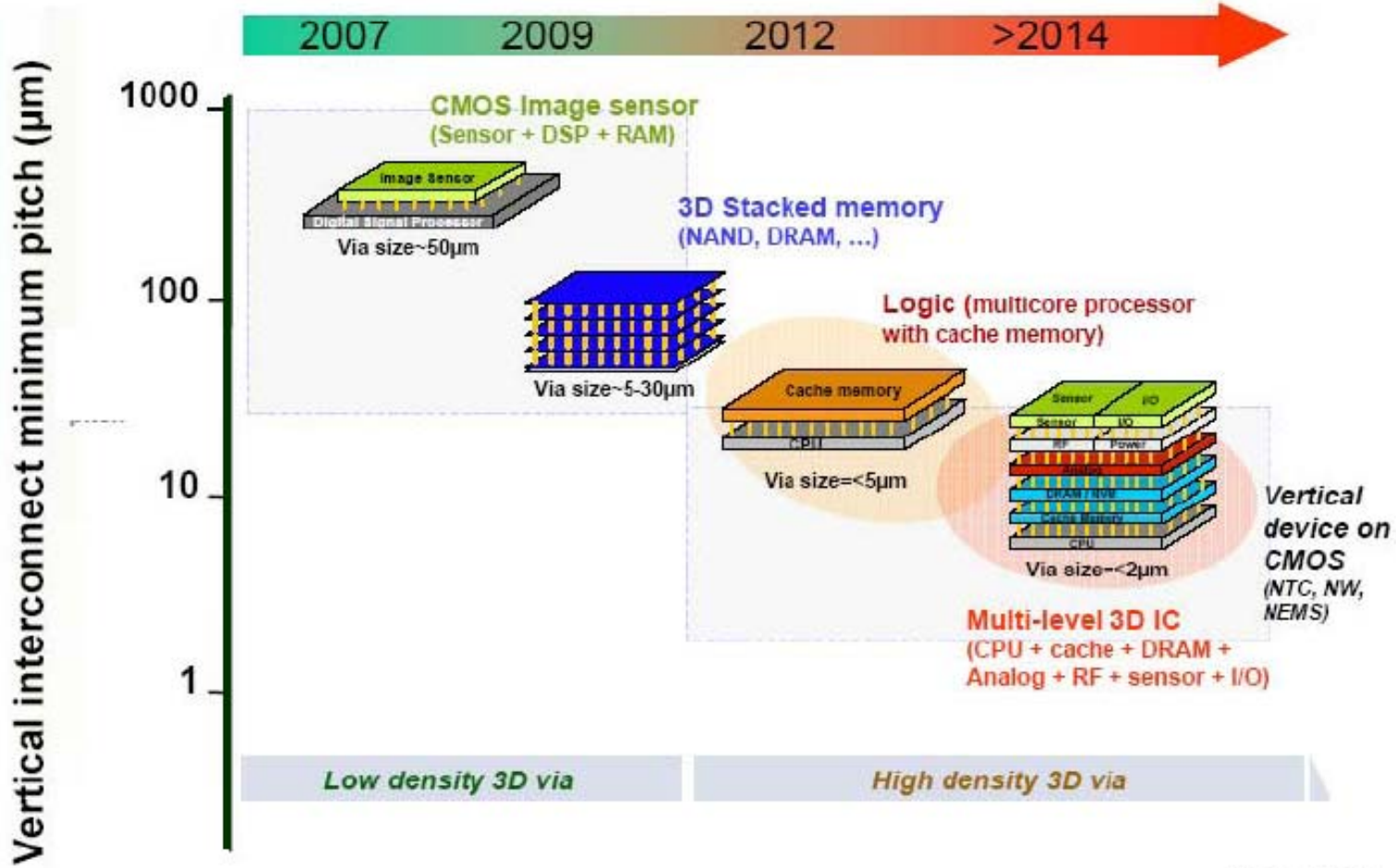

**Source: P. Franzon et al, NCSU,**
**"Design and CAD for 3D Integrated Circuits", Proceedings DAC 2008, pp. 668 – 673.**

# There is a Gap




**Adapted from:**
**M. Shapiro, IBM, RTI 3D Architectures for Semiconductor Integration Seminar, Nov. 2008**

# There is a Roadmap




Source: CEA Leti

# 3D TSV Appeal

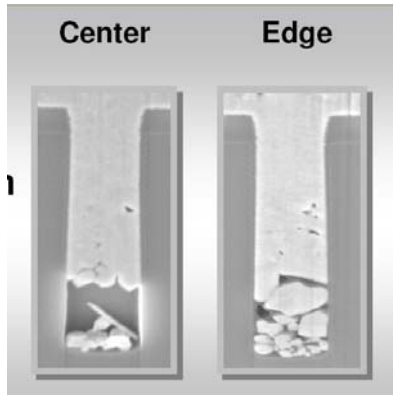
- **Higher overall density**
  - **Moore's Law continues**
- **Lower cost**
  - ***If* it yields**
- **Mix and match**
  - **Segregation of tasks**
    - **Logic below, memory above**
    - **Attach MEMS / Optoelectronics / AMS / RF / etc.**

# 3D TSV Appeal

- **Higher overall density**
  - **How much can you cram together?**
- **Lower cost**
  - **Electrical Properties / failure modes of real TSV**
- **Mix and match**
  - **Can you do it?**
  - **Can you design it?**

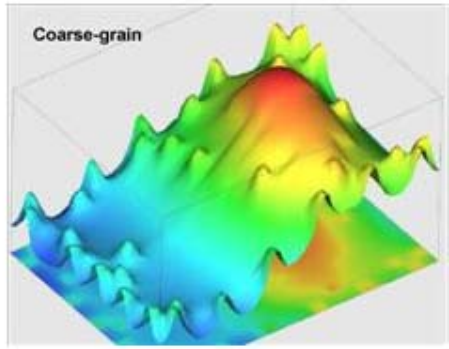
# TSV Problems

- Electrical properties of the TSV itself
  - e.g. 50 μm deep, 10 μm across, Cu in insulator in Si
  - How closely spaced?
    - Can design rules do it?
  - What are L,R,C as dimensions vary?
    ... over time?
    - Can look-up tables do the job?
    - Like RET modeling problem – Rule vs. model vs. hybrid
  - What are the failure modes?
- Need: Reliable, adaptable compact models
- Need: Metrology basis set for calibration
- Need: Test techniques for fabricated vias



# Transistors in 3D Context

- **Leakage Current not gone**
  - **Generates heat**
  - **Upper layers far from the package heat sink**
- **Does it Matter?**
  - **Effect on transistors**
    - **Temperature**
    - **Stress**
- **Need: Workable models**



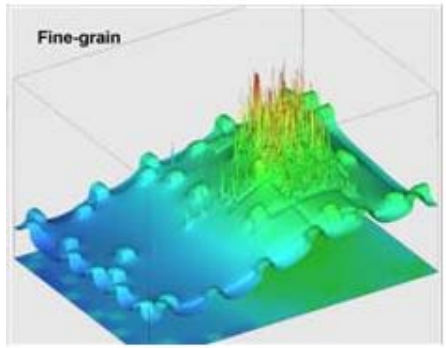
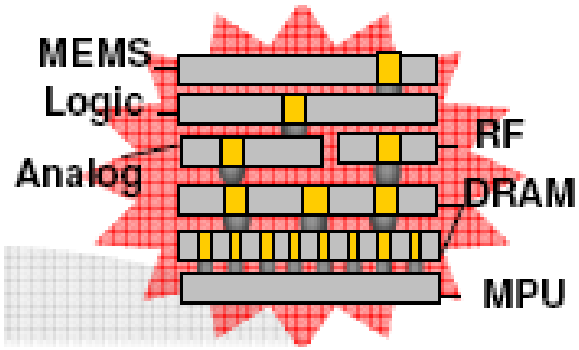




**Illustration from the Gradient Design Automation www.gradient-da.com**

# Design problems

- **Greatest appeal: Modularity**
  - **Stack old memory with new logic**
  - **Stack RF on Digital**
  - **Stack anything on everything**
    - **Allow components to be made with optimal processes**

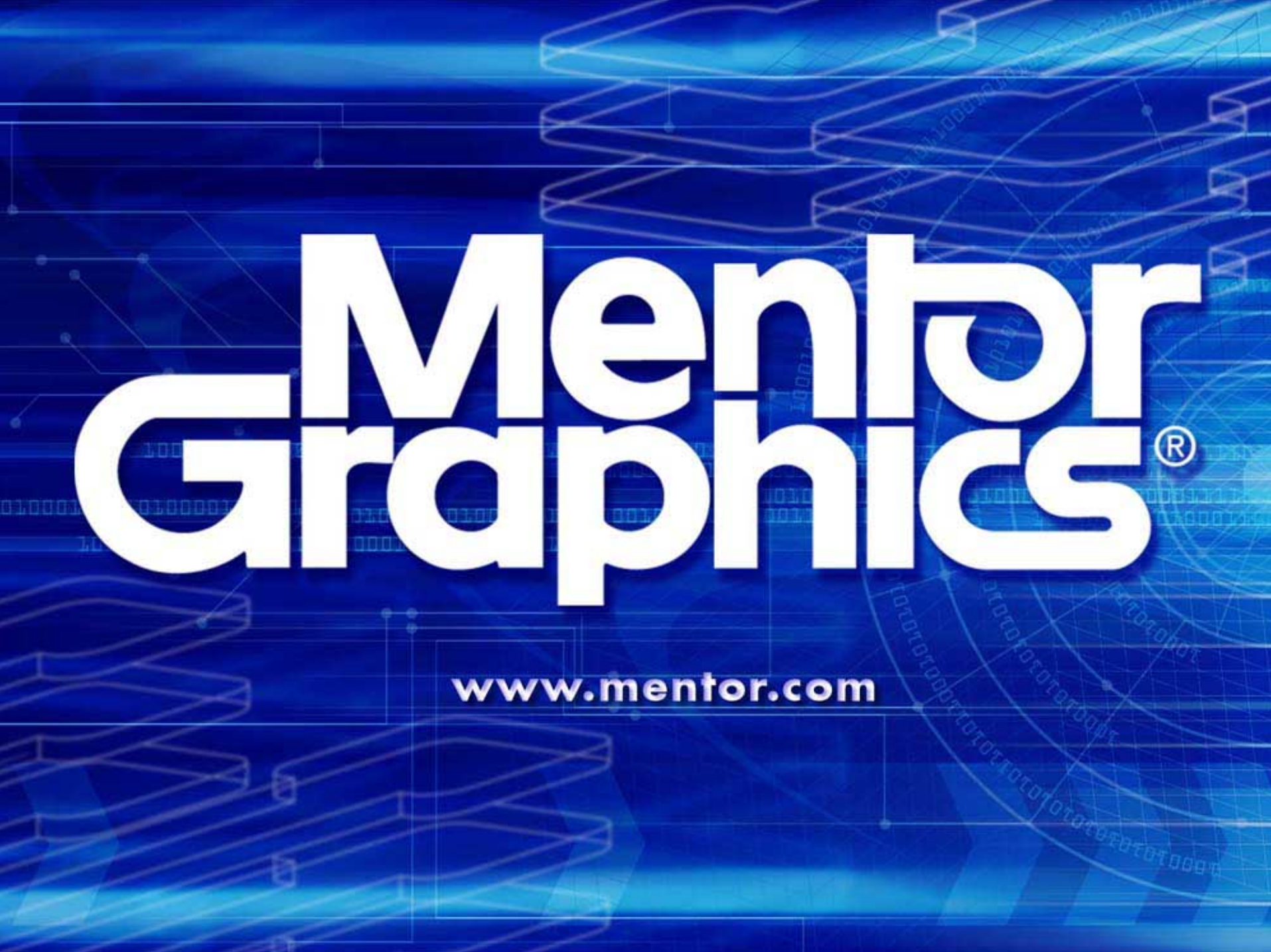



- **Need: What makes sense?**
  - **Where are the greatest benefits?**
  - **Which architectures are most complementary?**

# Final Slide

- Market needs are the real issue
  - What can stacking do better / cheaper / faster?
  - Can it really provide 2 nodes of value?
- Modeling tools that fill the gap are needed
    - And provide good University projects
  - Electrical properties and dependencies of vias
  - Behavior of stacked transistors
    - Power Management
    - Temperature modeling
    - Stress modeling
  - Mixed device architecture optimization

# Thank you for your attention.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