Session III
Design Challenges for 3D Integration

SRC GRC ETAB Summer Study

8:00 – 12:30

June 30, 2009

Agenda

8:00 **Introduction** - **John Darringer**, IBM
8:15 An IFM Perspective of a 3D Design Eco-System
- **Riko Radocic**, Qualcomm
8:45 Co-Design of Future Architectures with 3D Technologies
- **Mike Rosenfield**, IBM
9:15 Future Challenges From A Thermo-Mechanical Perspective For 3D
- **Gamal Refai-Ahmed**, AMD, B. Sammakia, SUNY Binghamton
9:45 **Break**
10:00 Taller vs. Smaller: 3D Development and Moore's Law
- **Frank Schellemberg**, Mentor
10:30 Coping with the Vertical Interconnect Bottleneck
- **Jason Cong**, UCLA
11:30 Architecture and Application Perspectives for 3D Integration
- **Yuan Xie**, Penn State
12:00 **Panel** – What are the top areas for 3D research?
– Moderator - **John Darringer**
12:30 **Lunch**

3D Trends

- 3D Technology in use worldwide
  - Important part of semiconductor roadmap
- Today: Simple designs with today's tools
- Tomorrow: Common set of challenges
  - Lack of physical models (mech, thermal, electrical)
  - Lack of tools to accurately evaluate design options
  - Lack of tools to support 3D chip integration and test
  - Lack of standards
- Evidence that Universities can help
- Consensus for action (semi and system houses)
  - 3D as driver of tasks in multiple science areas

Topics for 3D Research

1. 3D Architectural Exploration Analysis
   - Explore more configurations for low power and cost
2. 3D Design
   - Multi-layer units (cache, ALU, …)
3. 3D Technology Modeling
   - Compact models for TSVs and SPICE for therm/mech
4. 3D Chip Integration Tools
   - Physical synthesis that optimizes TSVs
5. 3D Chip Testing
   - Strategy to balance test complexity with performance