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Output from 2009 SRC GRC ETAB Summer Study

A Report to the SRC Board of Directors
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Sessions

- Research Portfolio Five Years from Now
- Research Opportunities for Systems/Software Research
- Design Challenges for 3D Integration
- Wrap-up and Compilation of Recommendations for the Board



Session I: Research Portfolio Five Years from Now - Key Messages from the ETAB



- While the focus is often on areas of divergence, there is much consensus on SRC-GRC research
 - Not recommending major changes
- Need to define specific areas of research appropriate to GRC with critical mass and adequate member interest
- Look to SRC-GRC management to then propose any structural changes – define the buckets in advance of directed funding
- Major follow-up work by GRC staff and members required to propose and rationalize a coherent portfolio response to the Summer Study output



Session I: Research Portfolio Five Years from Now – Area to Explore Expanding



- System research, particularly system-level design, is a building interest for many companies – major relevance in ICSS, CADT and IPS
 - Need an integrating strategy based on requirements of some selection of model future systems relevant to the members
 - Should be a driver vertically (system to devices) and horizontally (across technologies)
 - Crisply define roadmap, inputs/outputs, tasks and SA ownership (including significant cross-thrust work)
 - Reflect ITRS and learning from past projections in proposals
 - Need to remember that we must have materials, processes and structures - building blocks (bottom up) - to address system needs (top down)

The co-design arrows go up as well as down

Need tools that address all levels of abstraction



Session I: Research Portfolio Five Years from Now – Additional Guidance



- Pursue relevant opportunities for additional funding like TxACE and Multicore Solicitation
 - ESH center work with other government agencies?
 - Other TRCs beyond NINE and TERC?
 - Topics to attract new members
- Cost aspects should be evaluated, e.g. 3D
 - Assessment of viability comprehended in proposal review/ITRS
- Re-establish tracking of opportunities for transfer from one entity to another (e.g. FCRP to GRC, GRC to SMT)
 - Migration between entities is part of corporate goals – will make information accessible to ETAB
 - Highlight funding issues and pros/cons of overlap with respect to e.g. differing entity membership
- Members always need to evaluate whether we have the right people in advisory bodies to carry us forward



Session II: Research Opportunities for Software/Systems Research - Discussion



- 4 Application spaces of future multicore systems were presented:
 - Cyber-Physical Systems (embedded + networking) – Ty Znati, NSF
 - Hybrid (GP + networking): Shahrokh Daijavad, IBM
 - Industrial (automotive): Raj Rajkumar, CMU
 - Massive data computing: Pradeep Dubey, Intel
- Trends going beyond SoC: Jan Rabaey, UC Berkeley
 - Complexity, reliability, and energy providing problems that require solutions going beyond the silicon level and top-down design.
 - Broad collaboration needed
- ETAB generally agrees that system design research needs to be more strategically guided into the GRC. However,
 - **Biggest Issue: 'Systems and/or Applications' Research too broad.**
 - Appropriate research topics in right time frame appear to be definable - more work needed to make specific recommendations
 - Zero-sum funding issue not resolved



Session II: Research Opportunities for Software/Systems Research



- Recommendations

- GRC Staff map New Multicore portfolio (25 CADTS/ICSS projects) and topics proposed by presenters (back-up) against
 - Resiliency and concurrency
 - Other system research topics/applications
- Form *ad hoc* advisory group between ICSS, CADTS and IPS to
 - Complete system/applications research topics, and their evaluation
 - Does 'embedded systems' help restrain the topic of systems research or not?
- Follow up on CPS joint NSF/GRC solicitation
- Embedded Systems (Real-time Computing) may **comprehend most of GRC's system research needs**



Session III: Design Challenges for 3D Integration - Key Messages from Presenters



- 3D Technology in use worldwide
 - Important part of semiconductor roadmap
- **Today: Simple designs with today's tools**
- Tomorrow: Common set of challenges
 - Lack of physical models (mech, thermal, electrical)
 - Lack of tools to accurately evaluate design options
 - Lack of tools to support 3D chip integration and test
 - Lack of standards
- Evidence that Universities can help
- Consensus for action (semi and system houses)
 - 3D as driver of tasks in multiple science areas



Session III: Design Challenges for 3D Integration - Topics for 3D Research



1. 3D Architectural Exploration Analysis
 - Explore more configurations for low power and cost
2. 3D Design
 - Multi-layer units (cache, ALU, ...)
3. 3D Technology Modeling
 - Compact models for TSVs and SPICE for therm/mech
4. 3D Chip Integration Tools
 - Physical synthesis that optimizes TSVs
5. 3D Chip Testing
 - Strategy to balance test complexity with performance

- Board inputs will be comprehended along with the key messages and disseminated to the ETAB
- Member Company ETAB representatives will discuss directions within their individual companies and provide SRC-GRC with comments and potential research areas to consider based on these messages
- SRC-GRC Management will propose portfolio responses



Session I: Research Portfolio Five Years from Now - Areas to Increase / Decrease



- More high-level system design (AMD); tools that provide an integrating strategy, repartitioning workloads to assign tasks in a multi-core / multi-controller environment (FSL), focus on tool work in CADTS (Mentor)
- Actionable roadmap on carbon thin film electronics within GRC (AMAT); basic materials, basic integration – continue focus on research in these areas. Technology down-selection, e.g. CNT and other technologies that have run their course. Re-invest in new technologies, e.g. III-V [keep in MPD]. (Novellus); new materials research to enable future multi-system – more effective roadmap from NRI to GRC (TEL)



Session I: Research Portfolio Five Years from Now - Areas to Increase / Decrease



- 1-Low Power High Performance Technology research, 2-3D IC, 3-Embedded memory (GF)
- Continued scaling, non-classical CMOS Center per plan; interest in design complexity challenges – would give up in e.g. some areas of NMS and CNT (Intel)
- New buckets: 1-Multicore / 3D, 2-Embedded systems with analog mixed signal, 3-Back end of line scaling, memory, devices. Roughly equal distribution (IBM)
- **Happy** with critical mass in analog mixed signal; new areas would be alternate application areas: bio-electronics, energy electronics. Would give up in Non-classical CMOS, CNT and graphene - already being done in FCRP and NRI - to reallocate funds. (TI)



Session II Results: Research Topics

Unprioritized, Not Evaluated



System tools that provide an integrated strategy

- System Verification and Synthesis including hardware, OS software and application software
- Workloads (part of both top-down and bottoms-up SoC design. Workload requirements drive design and multicore architectural decisions and validate designs)
 - Workload theory/partitioning for interfacing of silicon cores and microcontrollers to the application
 - Note: Workloads will not drive innovation for an application space
- System design, exploration and optimization tools
- On-chip tools such as debuggers, compilers (for complexity from asynchronous clocks, for example).

Architectural Research

- I/O and decisions relating to memory and networking.
 - Networking speed is increasing at a faster pace than GP speed.
- **Feeding the Beast “memory hierarchy design”** (Research: capacity- BW tradeoff)
 - Stacked – packed – embedded
 - Volatile – non-volatile – remote
- Manycore Scalability Research
 - Fine-grain sharing of control and data
 - Unstructured parallelism support
 - Client-server computing



Session II Results: Research Topics

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Architectural Research (cont'd)

- Acceleration
 - Unifying software framework to deal with accelerators in a holistic way across networking and massive data domains.
 - Domain/Application-specific
 - What lies beyond, crypto, video, texture, scatter/gather, XML? Programmability, debug, and reliability support
- Resilient architectures
 - for zero-defect operation
 - Robust, fault tolerant operation without user intervention, including ability to autonomously detect, compensate, avoid, or correct anomalous conditions.

Design Complexity

- Top Down design: Model-based design: more math, more algorithms, more theory needed in face of complexity
- Comprehending emergent behavior from cyber-physical systems, for example.
- What are the interfaces of most concern across GRC membership: between workloads, application codes, hardware, software?
- Optimizing power/energy management, QoS, architectures, and timing tradeoffs in the face of operating environment, (ultra low) power, and safety constraints
- More fundamental research for both HW and SW
- Cross-disciplinary linkages between semiconductor systems research and relevant application domains

Other

- Industry/university needs to collaborate on developing system performance metric trends
- Background research for Standards of interest to several GRC member companies
- Interaction with the analog world (Analog design)