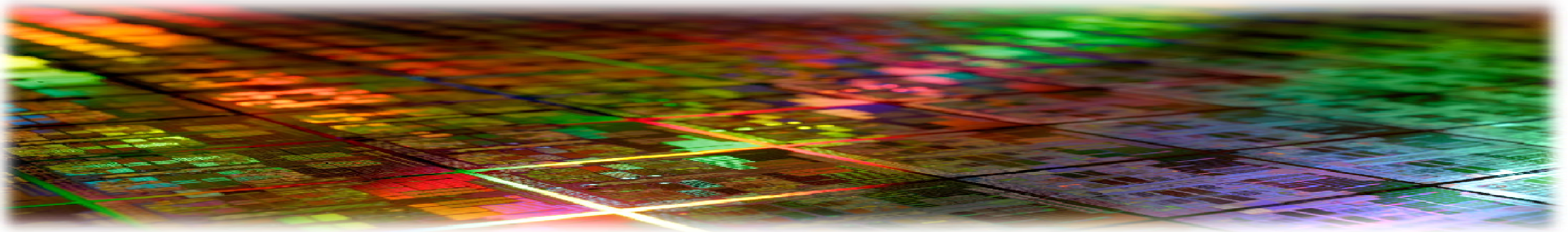

Extreme Patterning Solutions

Luigi Capodieci, Ph.D.

R&D Fellow, DFM Director

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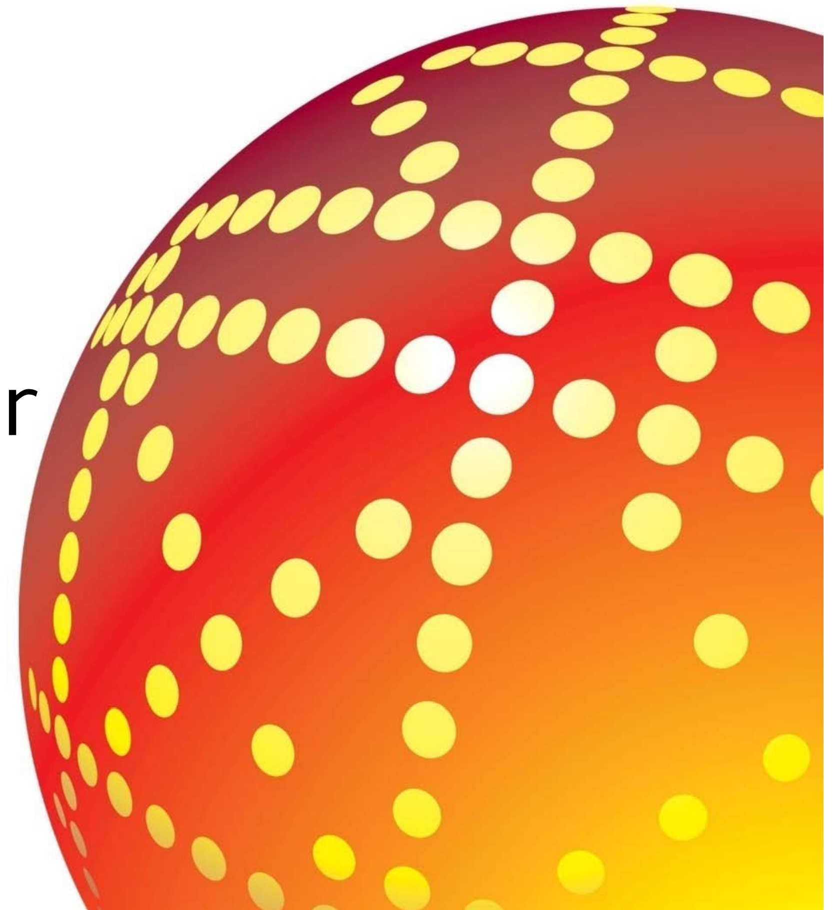

Outline

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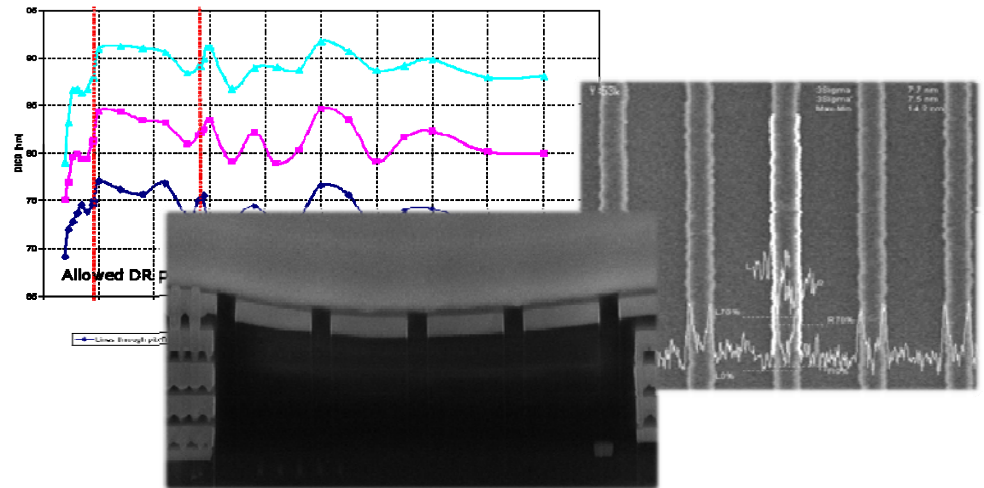
- Patterning in *perspective*:
  - **Variability** in Lithographic Processes
  - Manufacturing **Costs and Trends**
- Patterning and Physical Design
  - The case for DFM (Design for Manufacturing)
- Advanced Patterning at 22nm and below
  - Systematic approaches to ***managed variability***
  - Source Mask/Design Optimization and "*pixelated*" OPC
- Extreme Patterning Solutions at 20nm and below:
  - Dual Mask (and Multi-Mask) Patterning Schemes
  - Novel Process Integration Schemes
  - EUV: good progress, but timing risk
- Analysis and Conclusion: "State" of Patterning

Variability: key to patterning

- At the limits of the "geometric scaling roadmap": **variability** as a percentage of feature size increases:
  - –atoms don't scale
  - –kt/q doesn't scale
  - –photons don't scale
- Main factors:
  - –Intrinsic process variability
  - –Environmental effects
  - –Physical limits



- Variability affects Yield, Performance, and Power
- Variability can be classified as "random" and "systematic"
  - –Physical limits cause "random" variations (e.g. dopant fluctuations)

Variability: length scale

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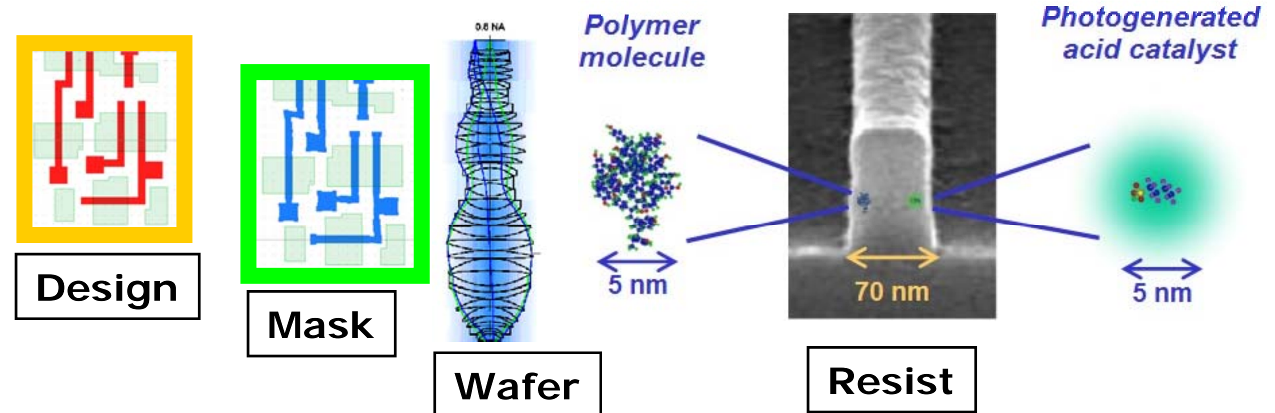
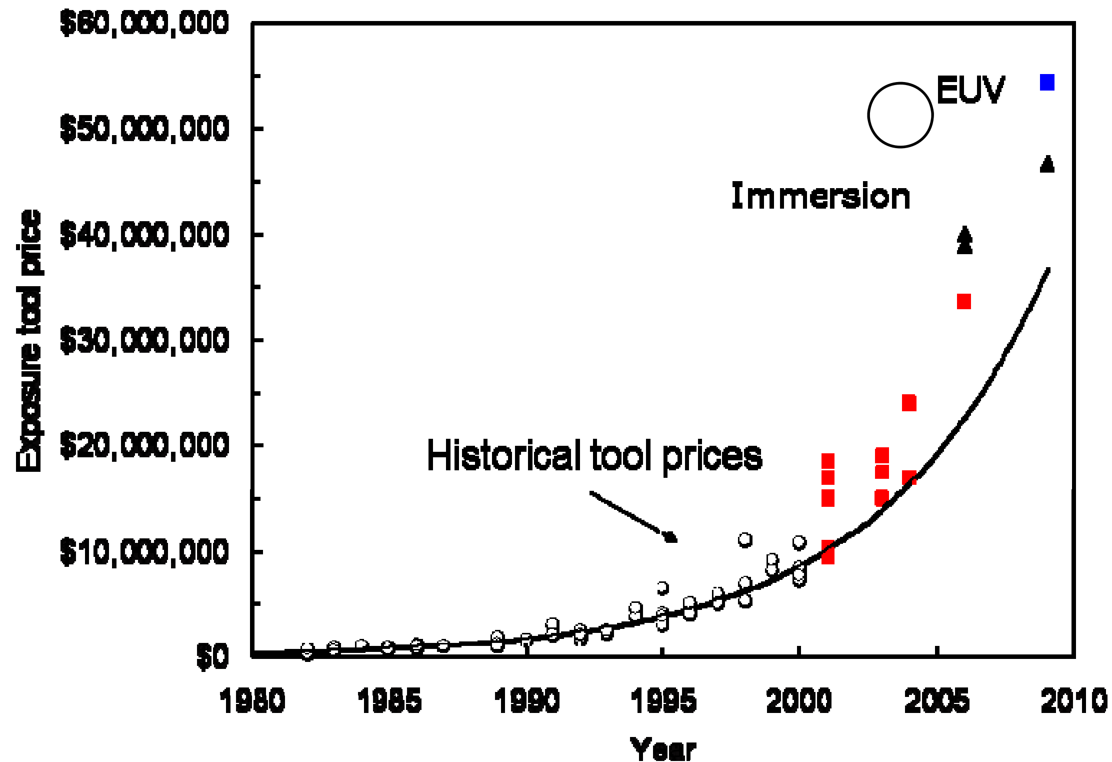
- Variability occurs at different length scales
  - Across a single transistor (or wire)
  - Transistor to transistor
  - Across Die
  - Across Wafer
  - Wafer to Wafer
  - Lot to Lot



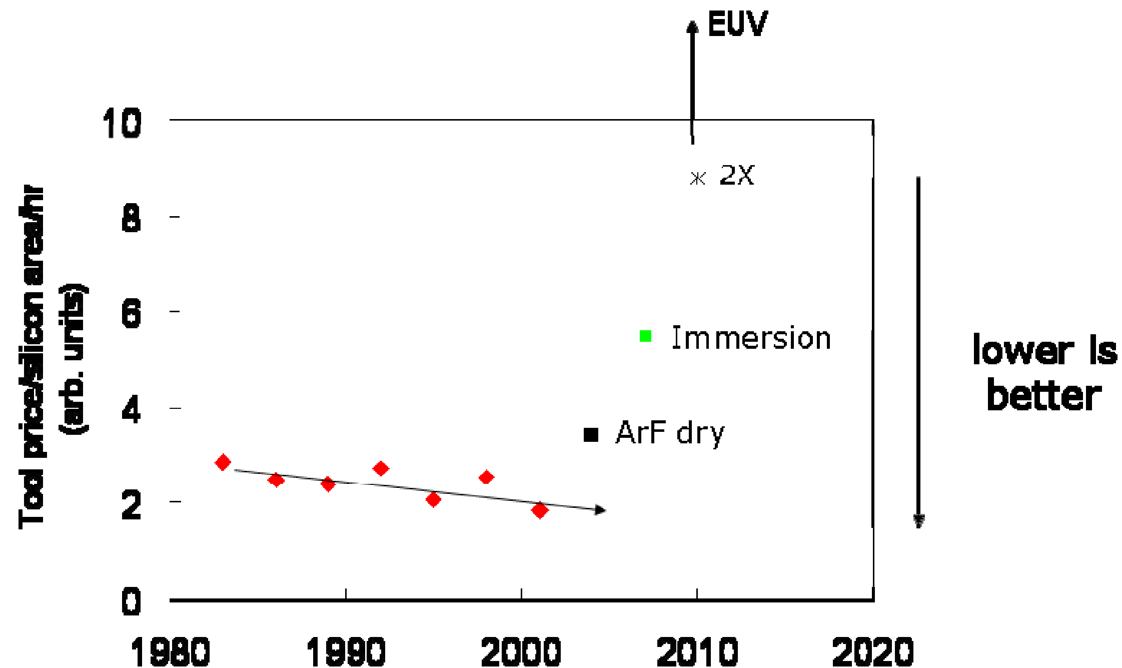
- Often systematic effects are considered random only because it is difficult (or impossible) to characterize them

Lithography Process Costs



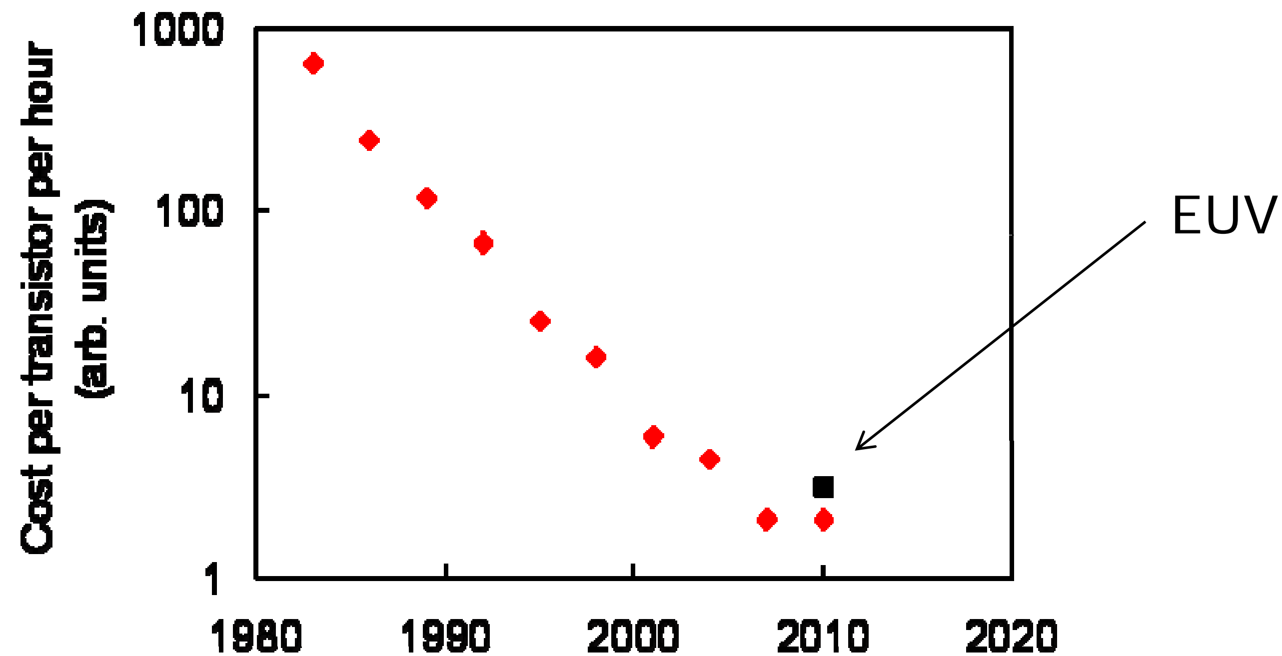
- Costs of Single tool increasing by ~3x every 5 years
- Scanner for 45nm node costs $40m

Lithography Costs Per Unit Area

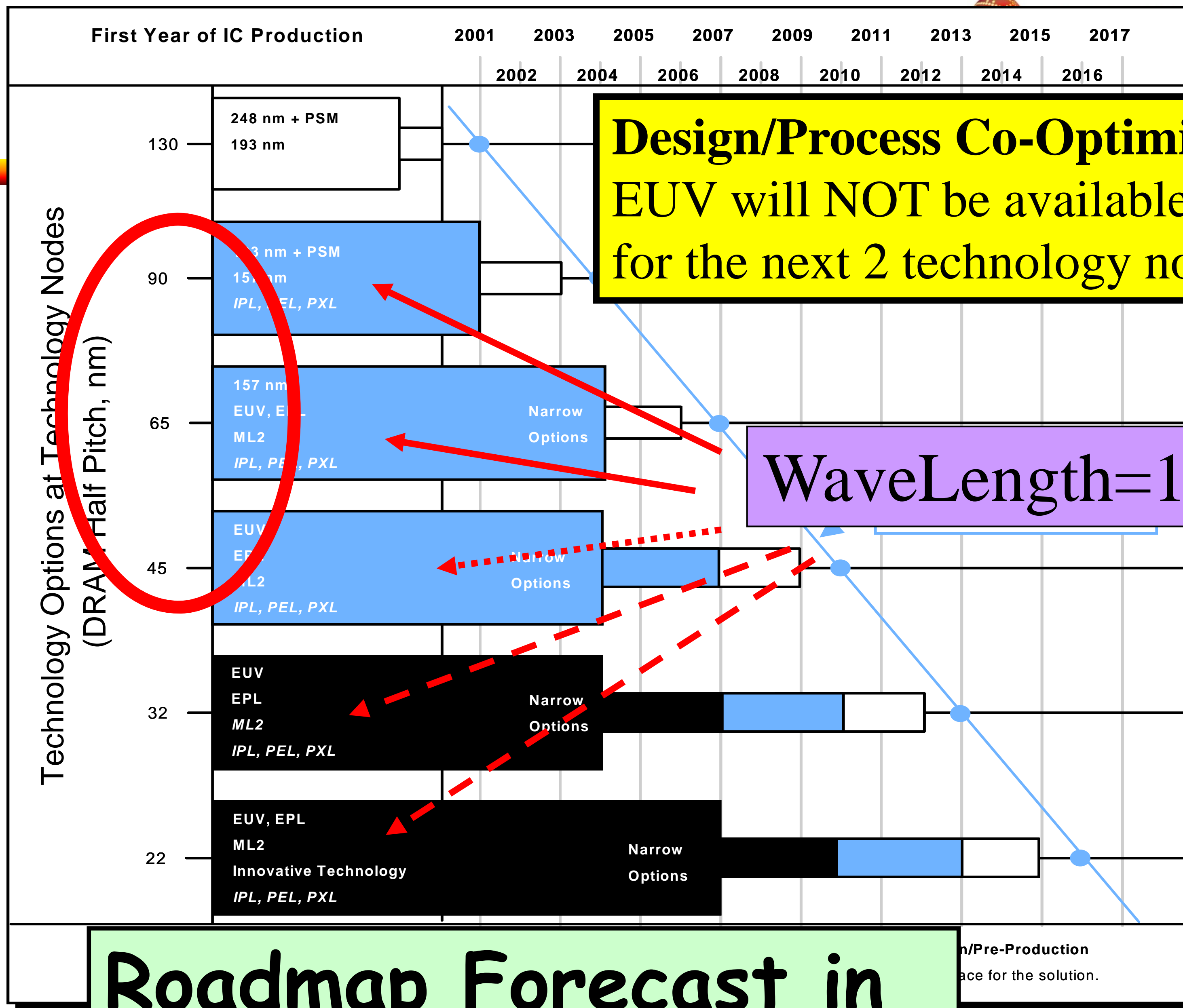


- Wafer Size increases
- Scanner Throughput (wafers per hour) increases
- Net: cost per unit area declined down to 65nm node
  - **Increasing for 45 and 32nm nodes**
- Supports relatively constant cost per chip

Lithography costs – Per Transistor

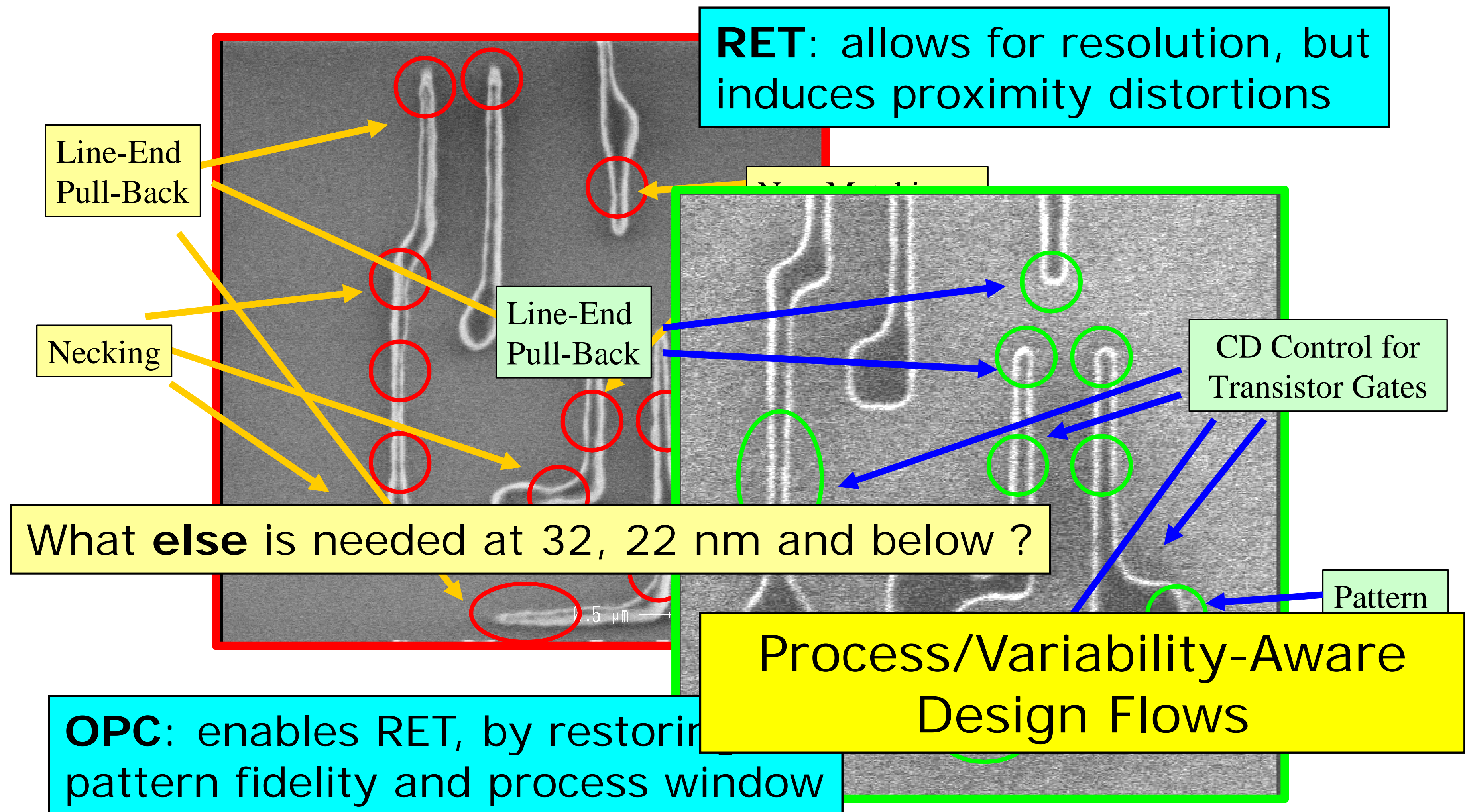


- Rapidly decreasing cost per transistor fuels semiconductor device and product innovation



Roadmap Forecast in 2001

Patterning and Physical Design at 45nm



Layout dependent Yield

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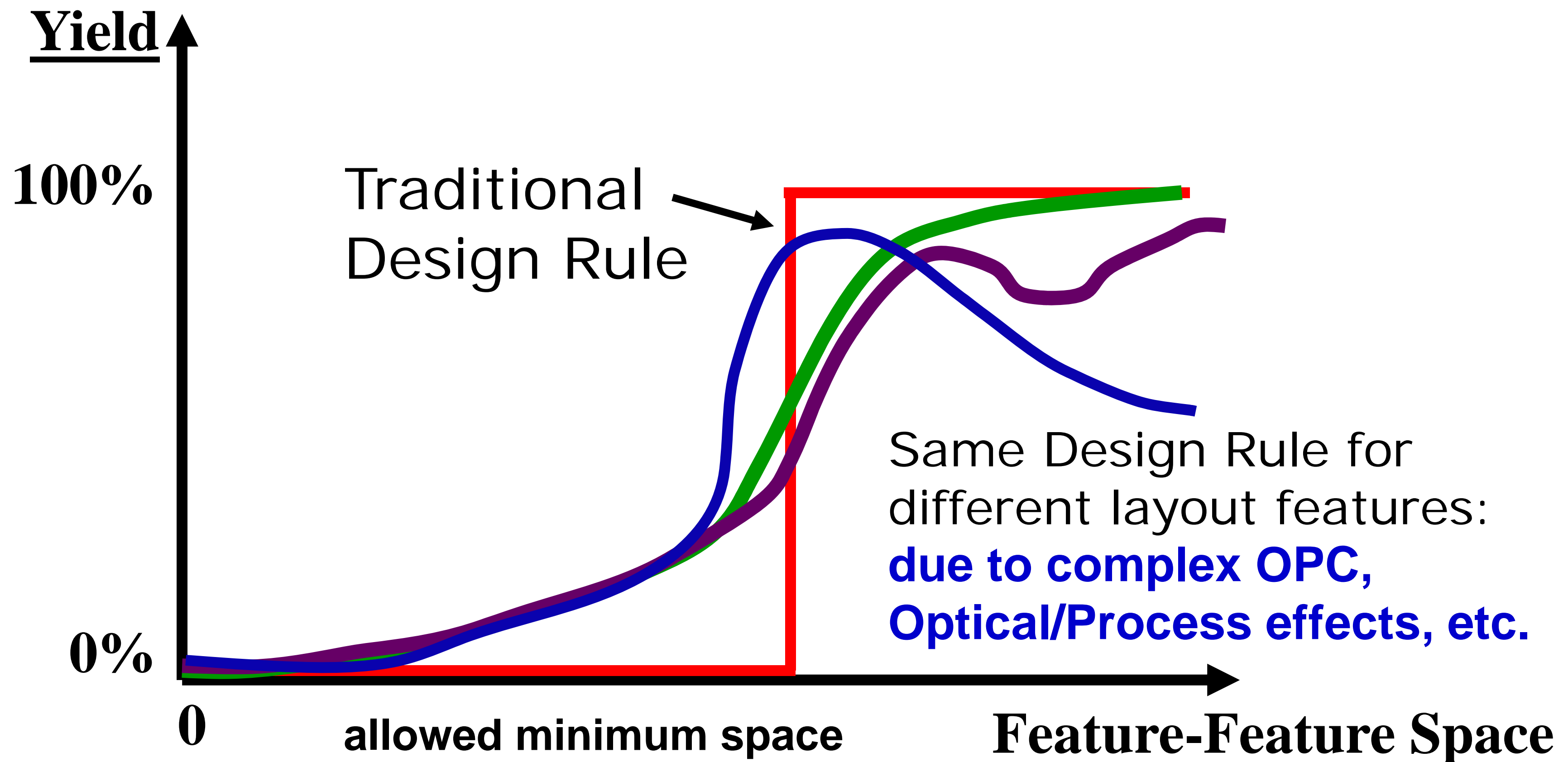

Courtesy of Kevin Lucas (Freescale, Synopsys)

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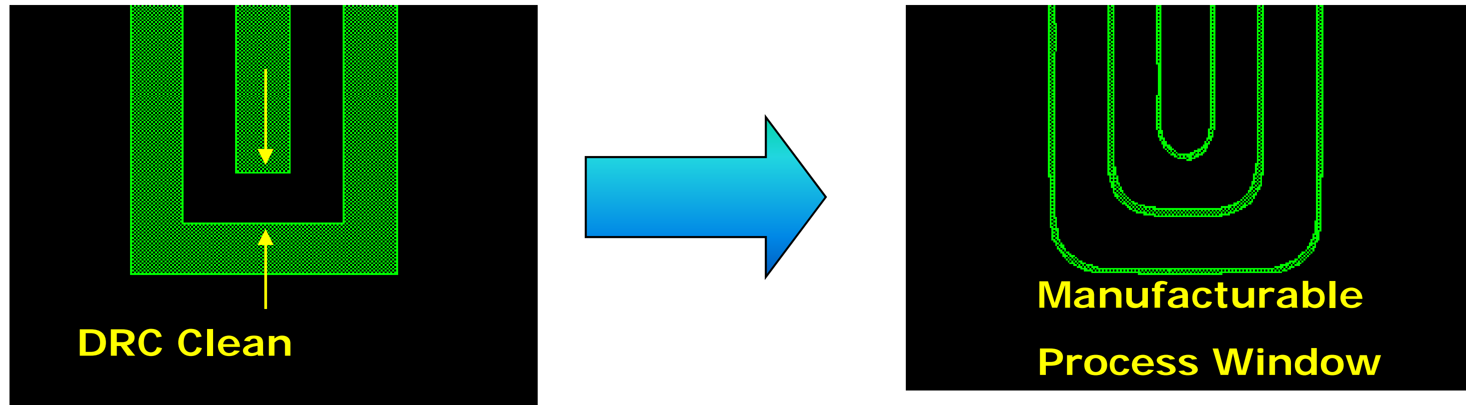
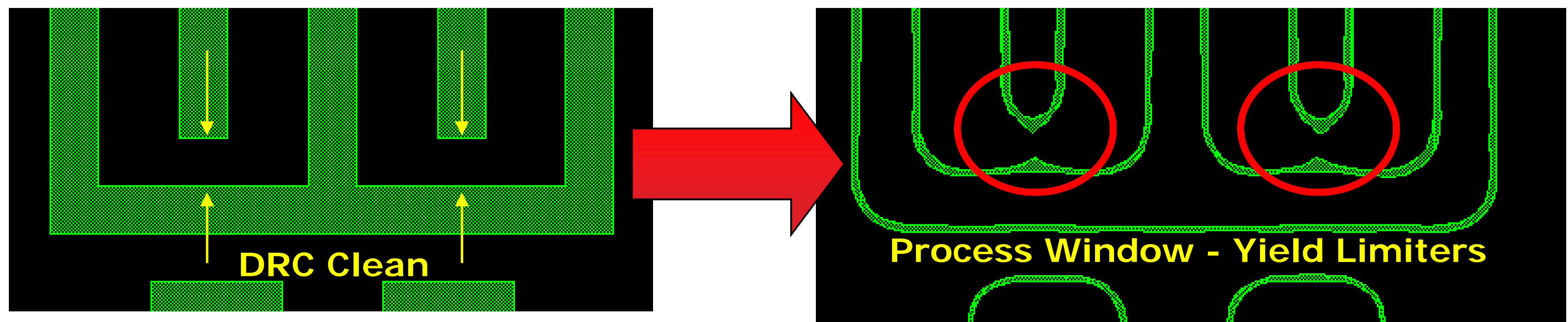
Yield vs. Design Rules at 32,28 and 22 nm



Design-Rules Compliance does NOT guarantee Yield due to:
Non-Linearity Effects Induced by Sub-Wavelength Fabrication.
Furthermore OPC cannot fix all Yield Limiters configurations



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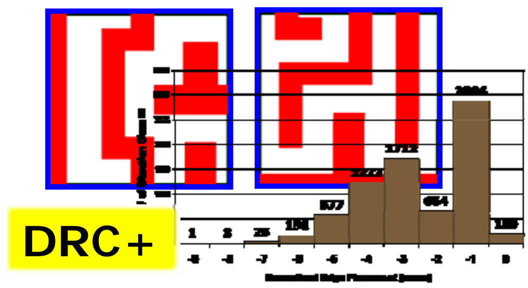
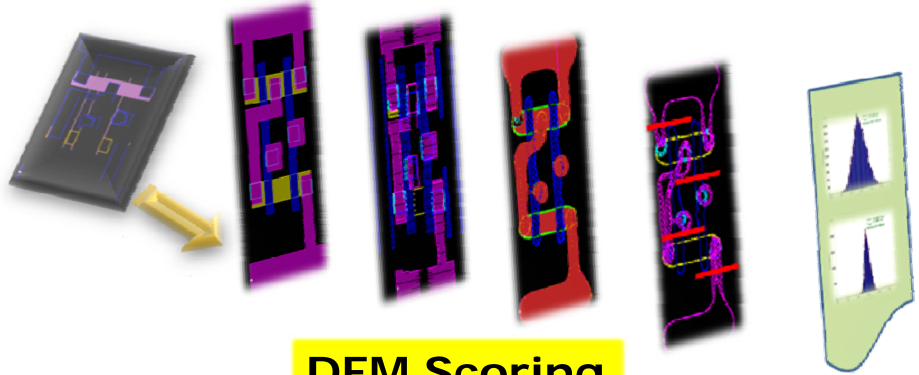
DFM – Enabling First-Silicon-Success

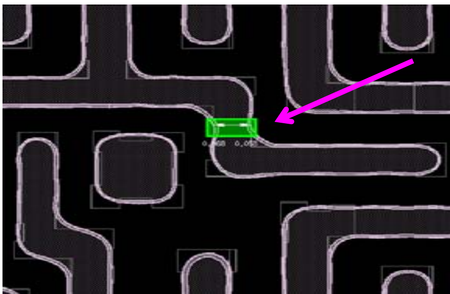
DFM Solutions @GLOBALFOUNDRIES
A *superior* portfolio of TOOLS and SERVICES

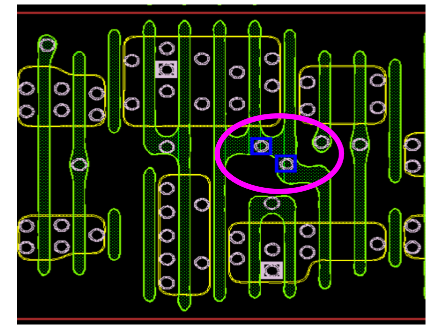


DRC+

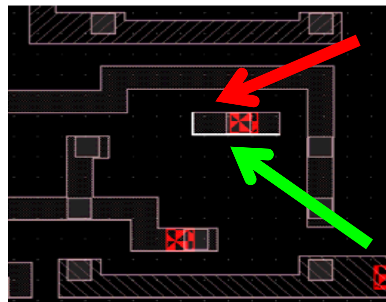


DFM Scoring

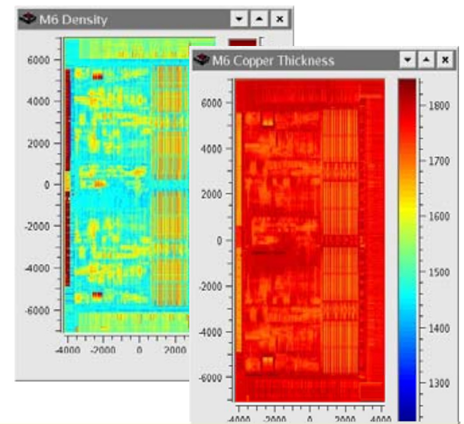




Hotspot Verification

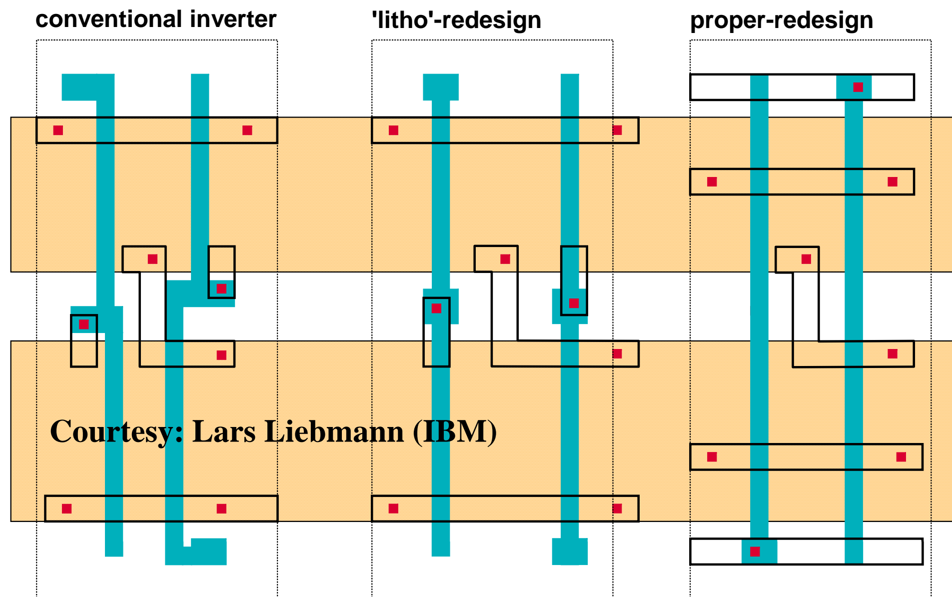


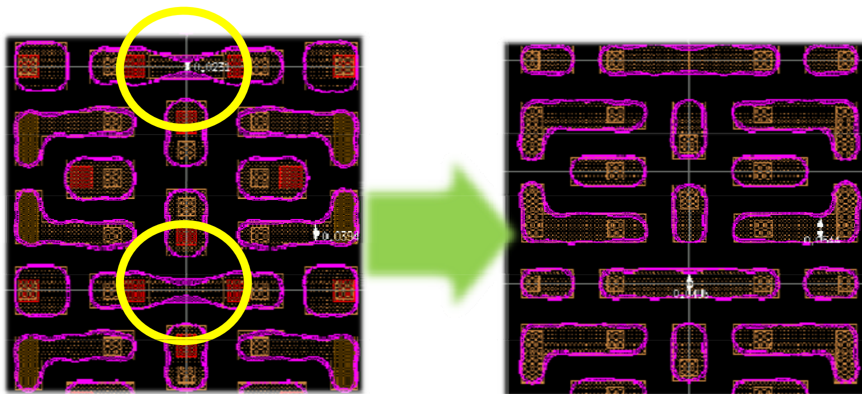
YRC - Rule-Based DFM

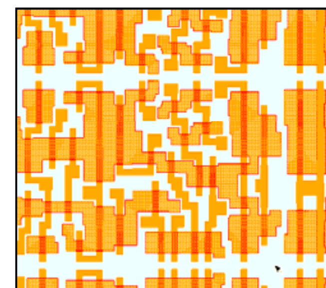


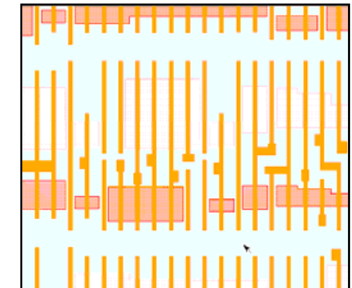
Smart Fill/CMP Modeling

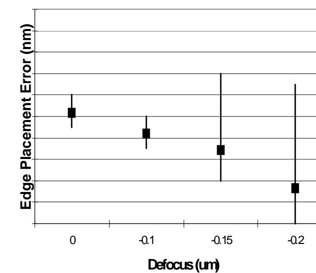
Physical Layout **Re-Design** (32,28nm)

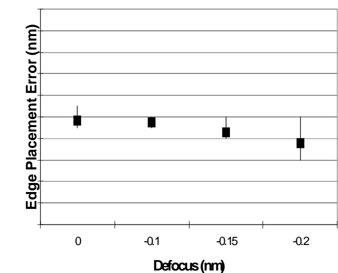





Conventional Layout


Restricted Design Rules





CD Variation Post-OPC: 10,000 gates simulated

Long History of Lithography and Layout Co-Optimization

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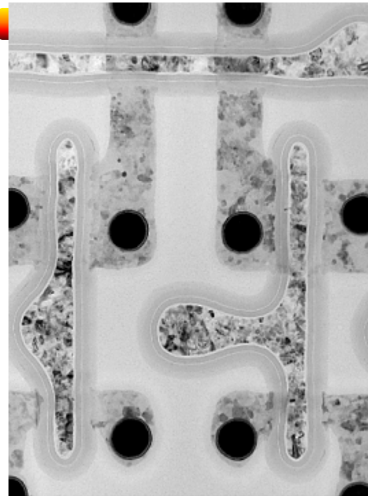
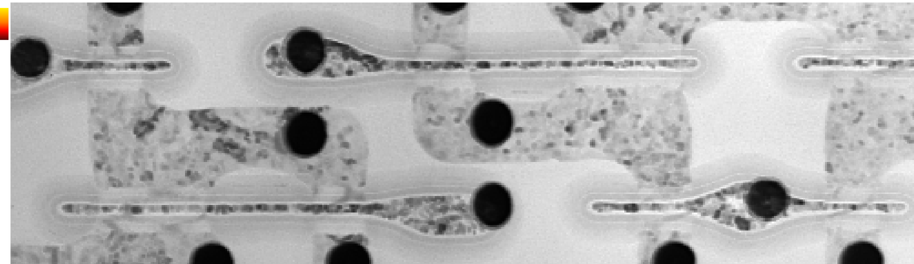
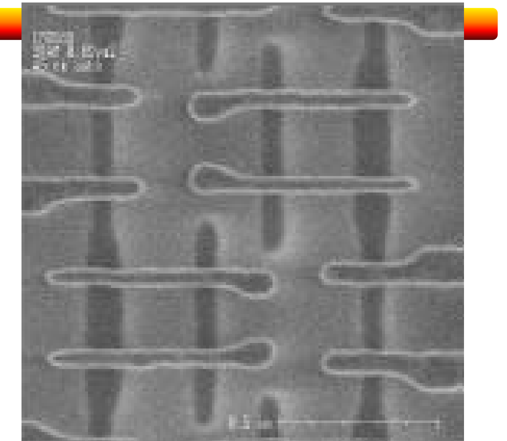


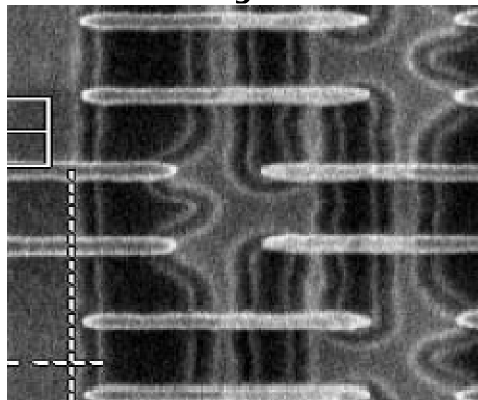
130nm SRAM
Traditional layout



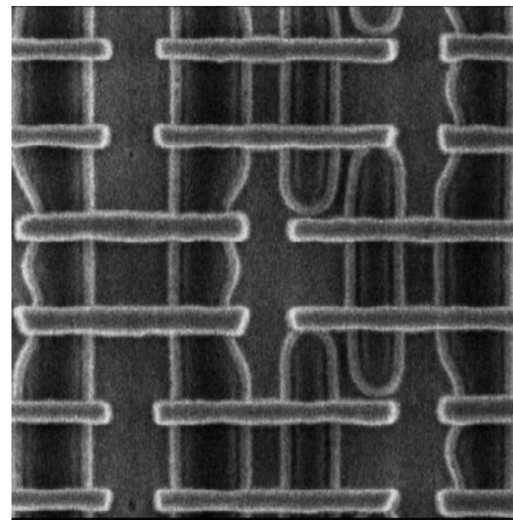
90nm SRAM
Uni-directional poly



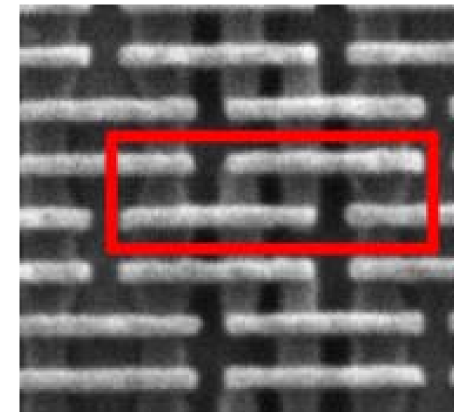
65nm SRAM
Uni-directional active



45nm SRAM
Immersion, uniform poly CD

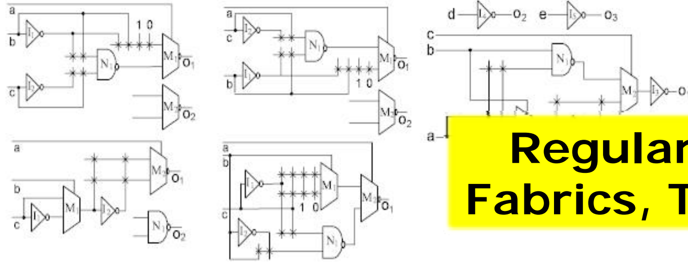


32nm SRAM
Double patterning

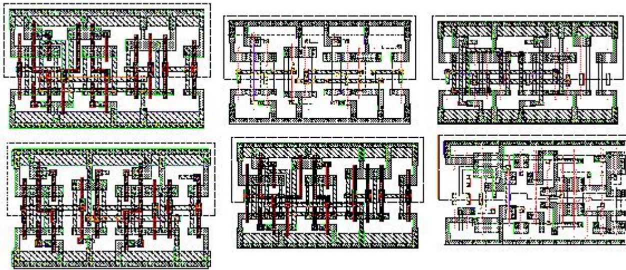


22nm SRAM
Higher NA immersion

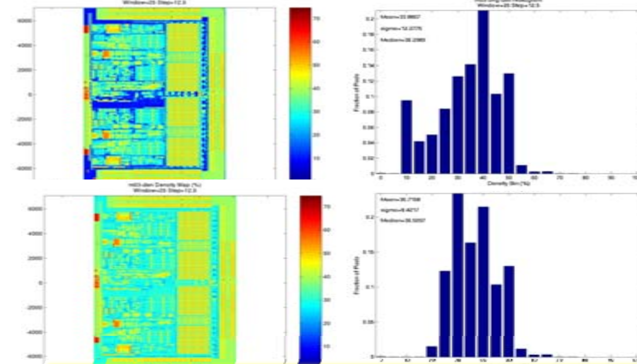
Bridge to 22nm: Process-Aware Design



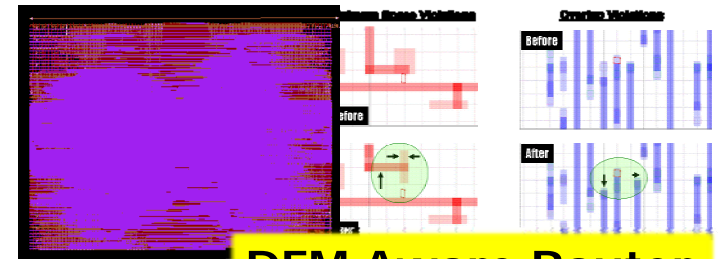
Regular Layout Fabrics, Templates



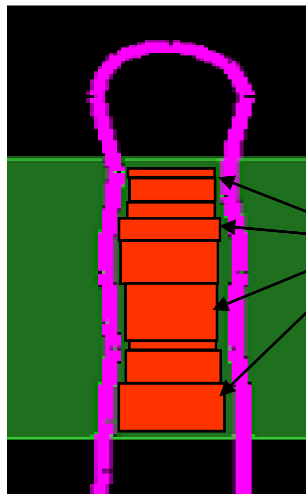
Design/Process Co-Optimization



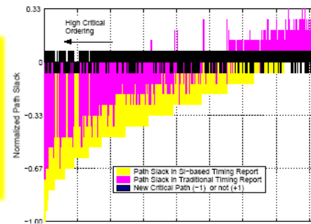
Smart Fill/CMP Modeling

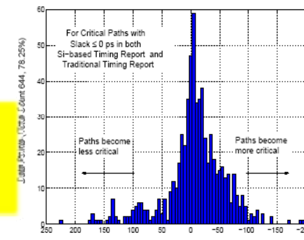


DFM Aware Router

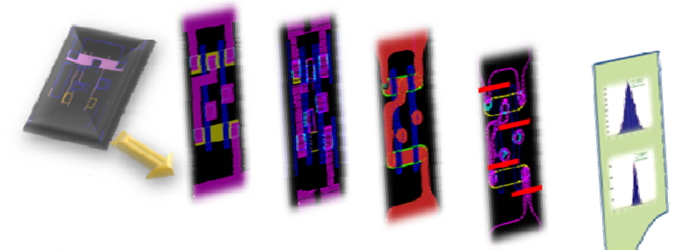


Non-Rectangular Transistor Modeling





Si-Based Timing Analysis



DFM Scoring (CAA/CFA)

Mask Optimization (MO):
Inverse Lithography Model-Based Assist Features

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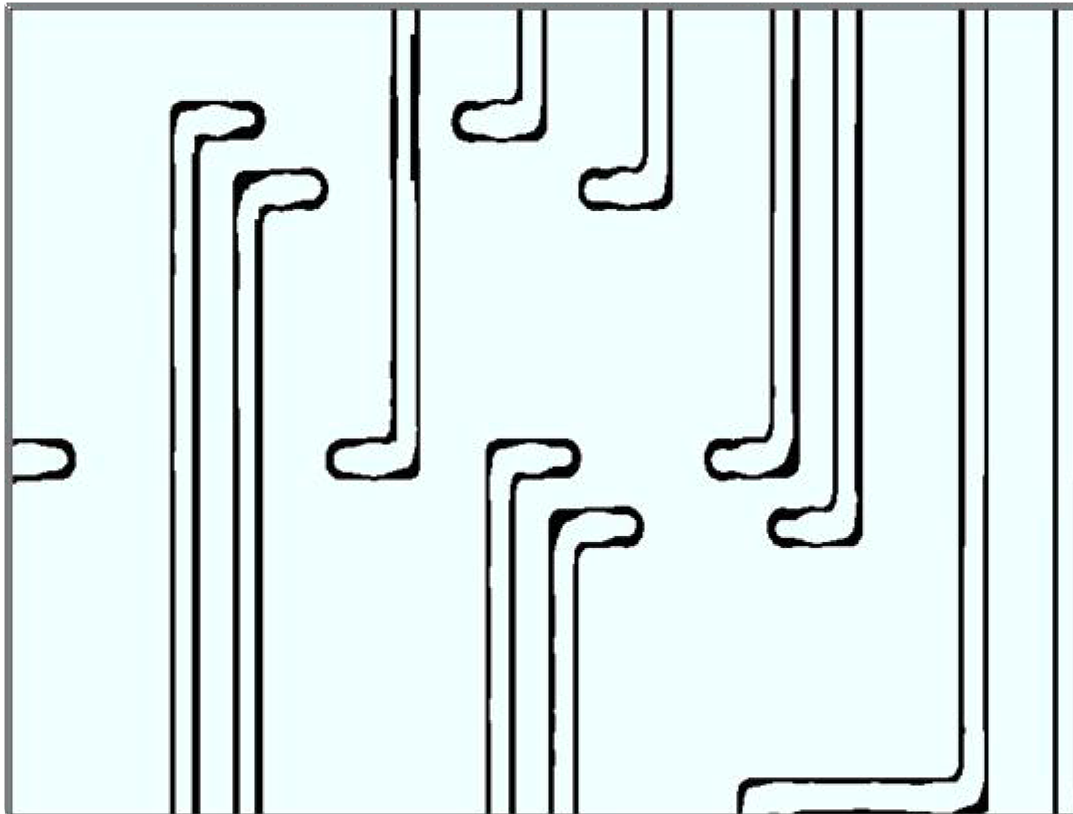

Process Variation Band

Yi Zou,
L. Capodieci, C. Tabery
SPIE XII - 2009

- Various inverse lithography methods for model-based AF insertion have been proposed
- Given a pixel-based objective function, inverse lithography synthesizes mask shapes, based on optical image analysis
- The mask synthesis process generates “corrected” shapes surrounded by AF shapes, both positive and negative

Source Optimization (SO)

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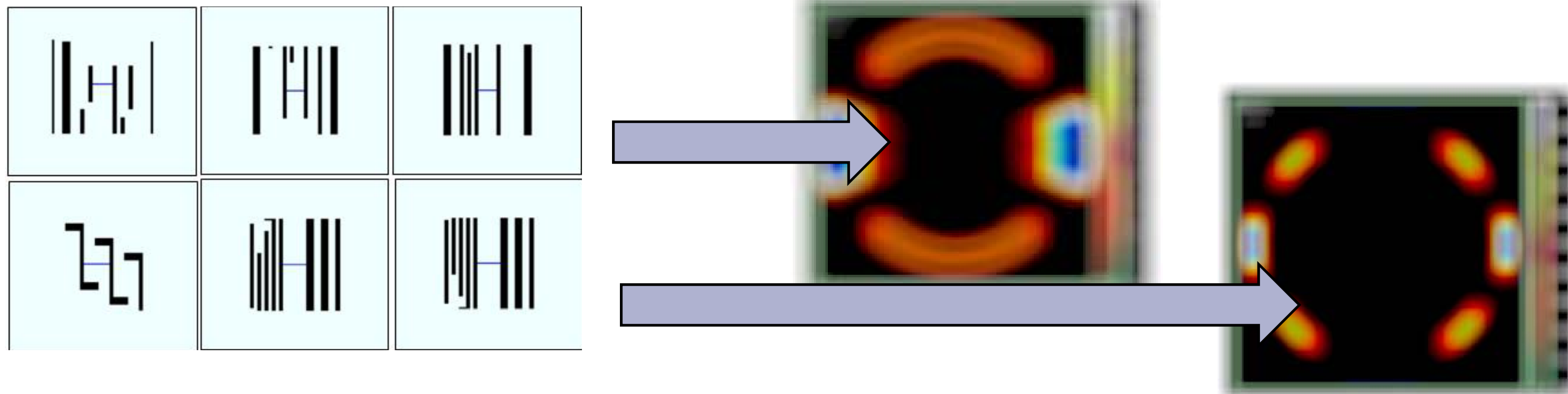
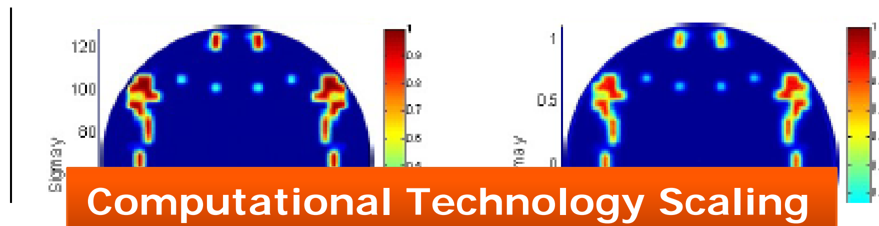
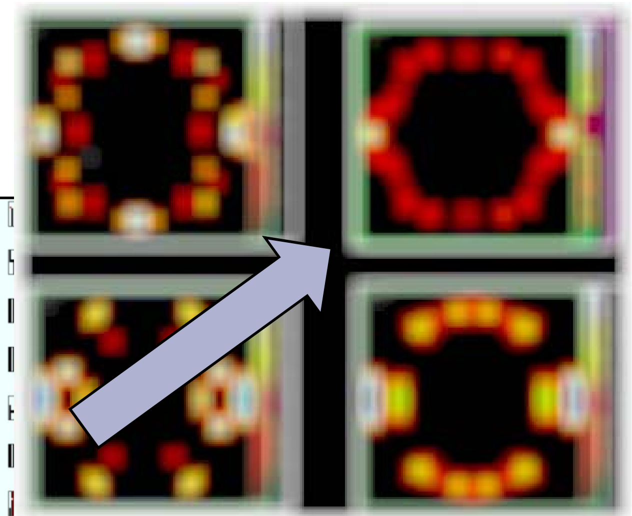




Computational Technology Scaling

- Algorithm:
  - Optimize illumination source **parameters** based on a library of layout features (1D, 1.5D, 2D)



Simultaneous Source Mask Optimization SMO: Theory and Reality

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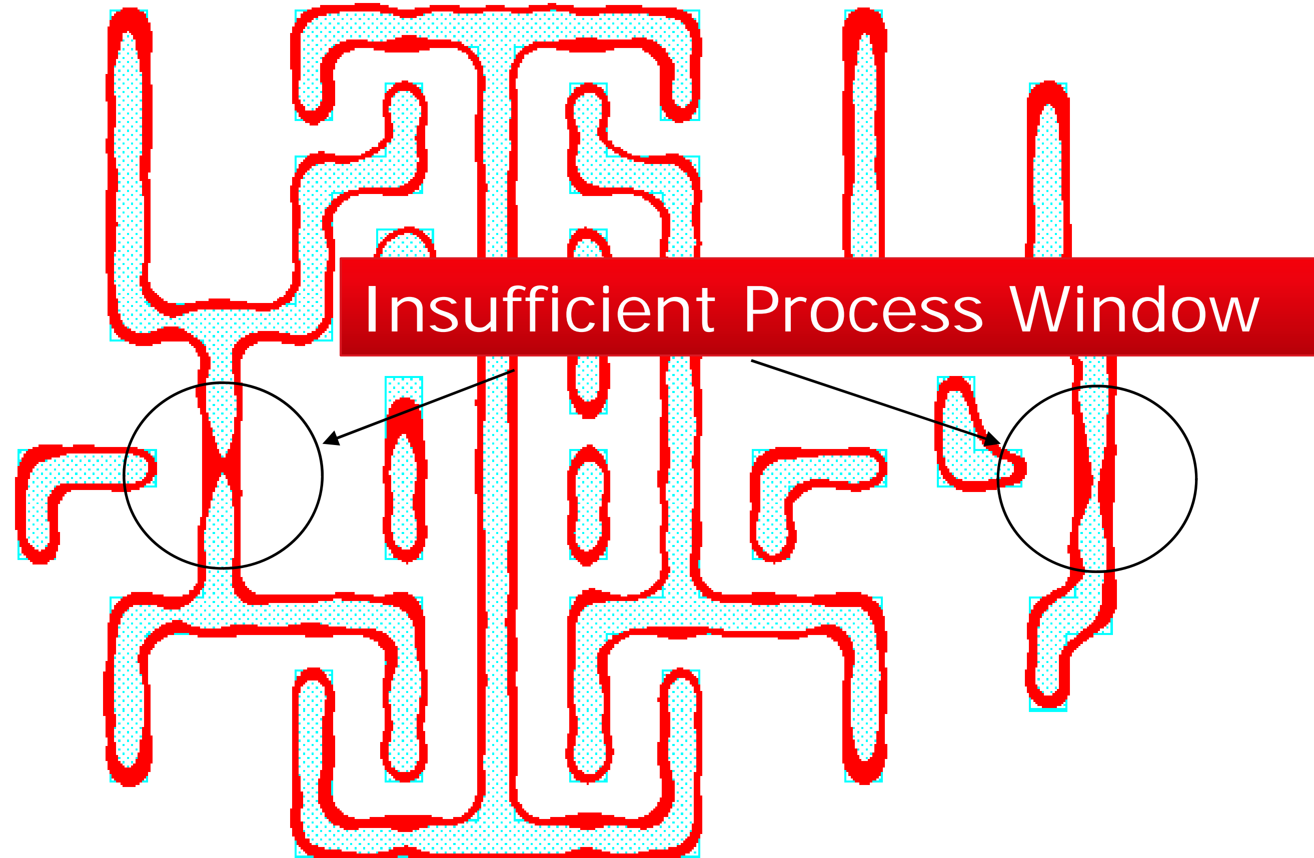
Comparison of 4 different methodologies indicates **Parametric Sources** are indistinguishable from SMO optimization

Limitations of RET and SMO at 22nm



$k_1 \sim 0.35$

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DFM + Restricted Design Rules at 22nm

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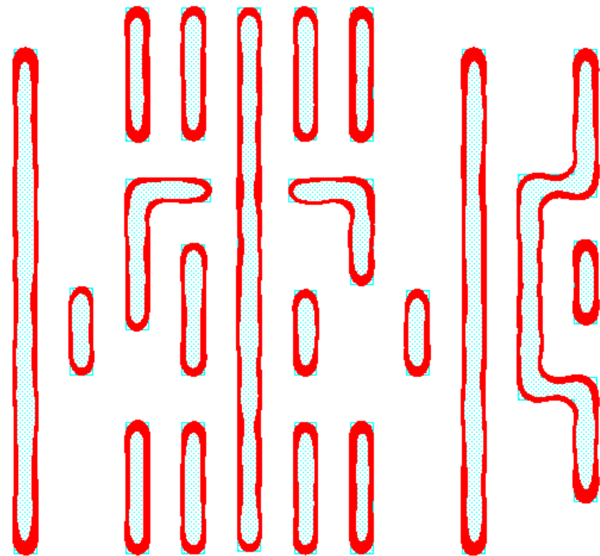
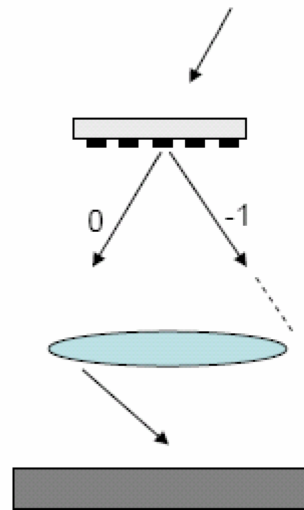
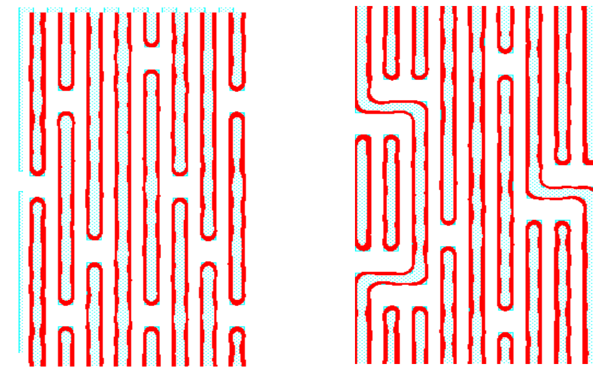


$k_1 \sim 0.35$



... still cannot violate physics laws

Process/Design Co-Optimization could postpone the introduction of double patterning



$k_1 < 0.35$

Double Exposure/Double Patterning at 20nm and below

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Increasing Process Complexity

One Film One Etch	Two Films One Etch	Two Films Two Etches
CEL 'Memoryless Resist' 'New Concepts'	Resist Stabilization -Pattern Freezing -Dual Solvents	Conventional Resist Process

Increasing Resist Materials Complexity

Double exposure single etch (pattern freeze)

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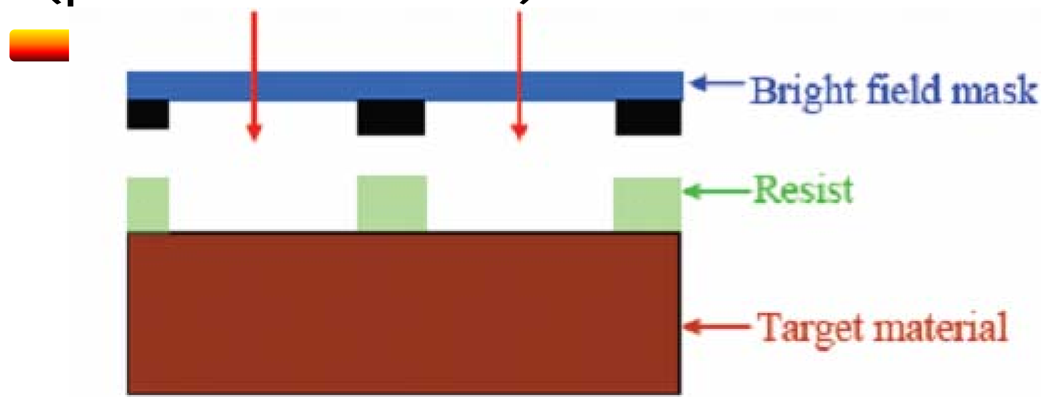
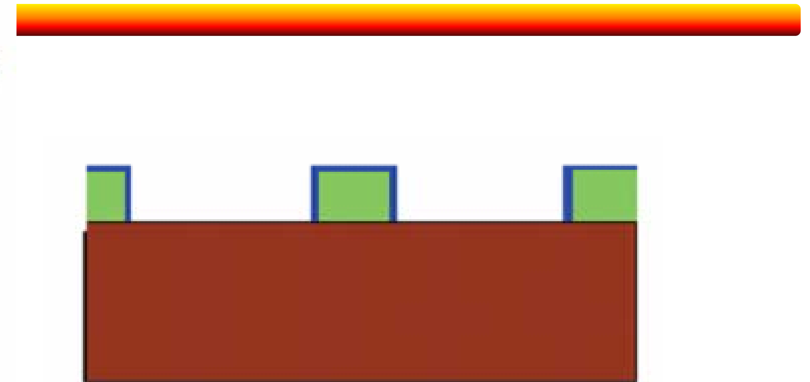
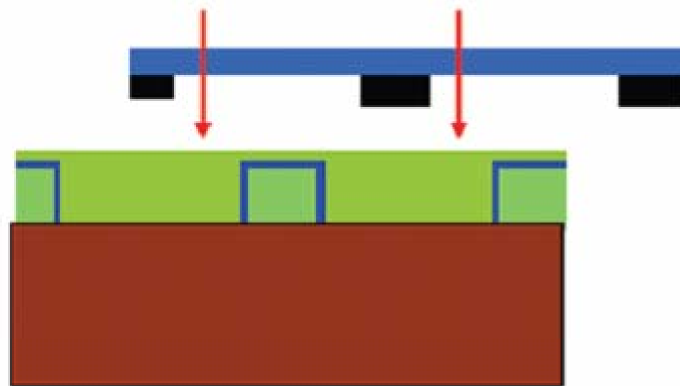


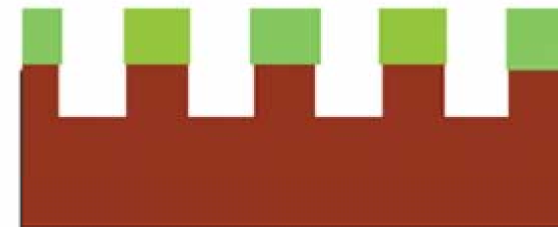
1. Narrow line printing



2. Pattern freeze



3. 2nd patterning



4. Etch transfer

- Positive resist is advantageous for narrow resist line printing
- Positive resist pattern freeze is challenging

Sidewall Image Transfer (SIT)
Self-Aligned Double Patterning (SADP)

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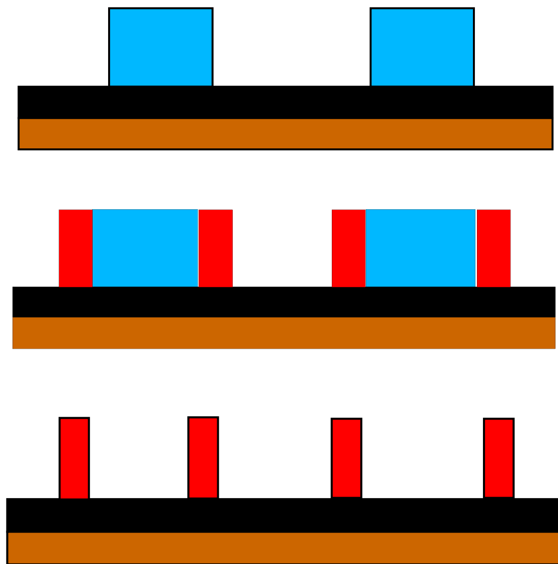

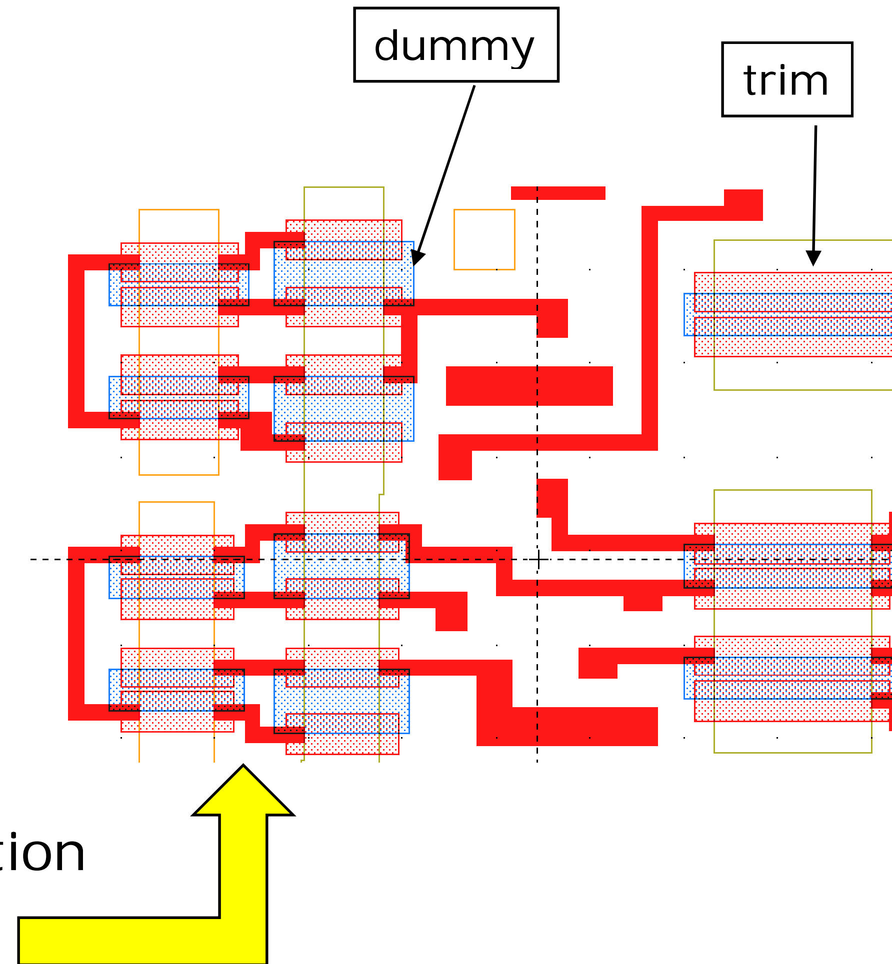

- Straightforward concept in 1D
- For unrestricted 2D layouts:
  - Complex Layout Decomposition
  - Multiple Mask Steps

Spacer-defined patterning: Complex Process Integration

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Resist
BARC
Dummy material
Hard mask
Hard mask
gate poly
gate dielectric
substrate

MASK 1
SPACER
MASK 2
MASK 3

1st Full-Chip EUV Demo: GF/AMD & IBM

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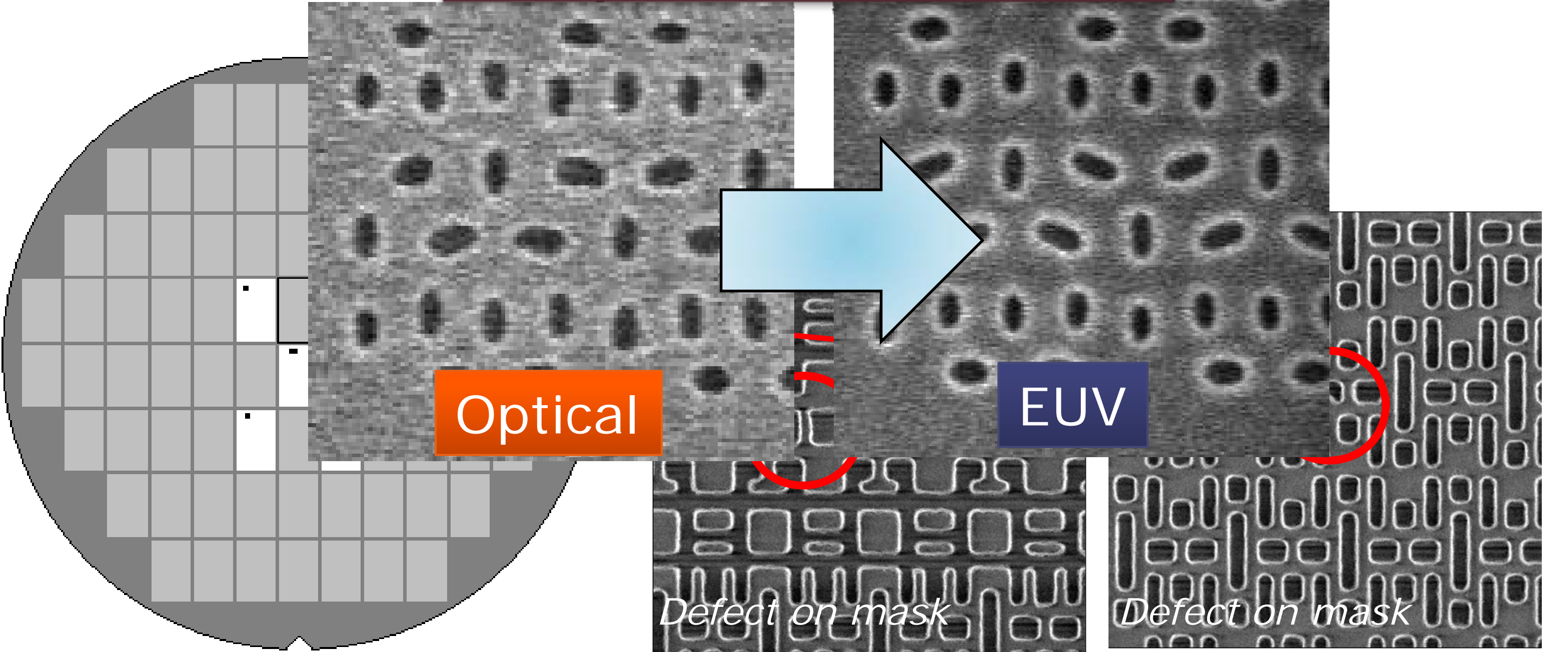

Summary: Current "State" of Patterning

- Extreme RET (DFM, SMO, ...)
  - Viable to 22nm
- Double Patterning (or Multi-Mask Patterning)
  - Needed at 20nm, issues of cost and process complexity
- EUV:
  - Steady progress, but late for introduction at 20nm

- Nano-Imprint
  - Problems: Defectivity, Overlay, Throughput
- Directed Self-Assembly
  - Still in "demo" phase. Can DNA scaffolding provide a breakthrough?
- Maskless
  - Might work for low-volume, issues of low throughput

Acknowledgments

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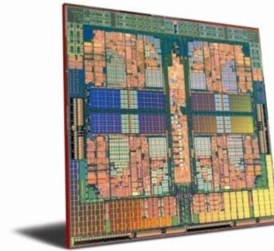
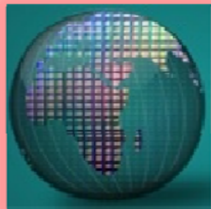
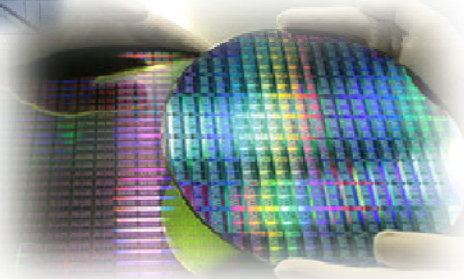

Jongwook Kye, Ryoung-han Kim, Tom Wallow, Harry Levinson, Rich Klein, Norma Rodriguez, Marilyn Wright, Rolf Seltmann, Cyrus Tabery, Sarah McGowan, Carl Babcock, Chris Spence, Yi Zou, Jie Yang, Vito Dai, Ethan Cohen, Uwe Hahn, Mark Craig, JR Zhou, Ed Roseboom, Stefan Roling, FAB1/A/B, Norman Chen, Chidam Kallingal, Jason Cain, ...

... and many, many others at GLOBALFOUNDRIES and AMD