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Capacitorless Double Gate Quantum Well Single Transistor DRAM: 1T-QW DRAM

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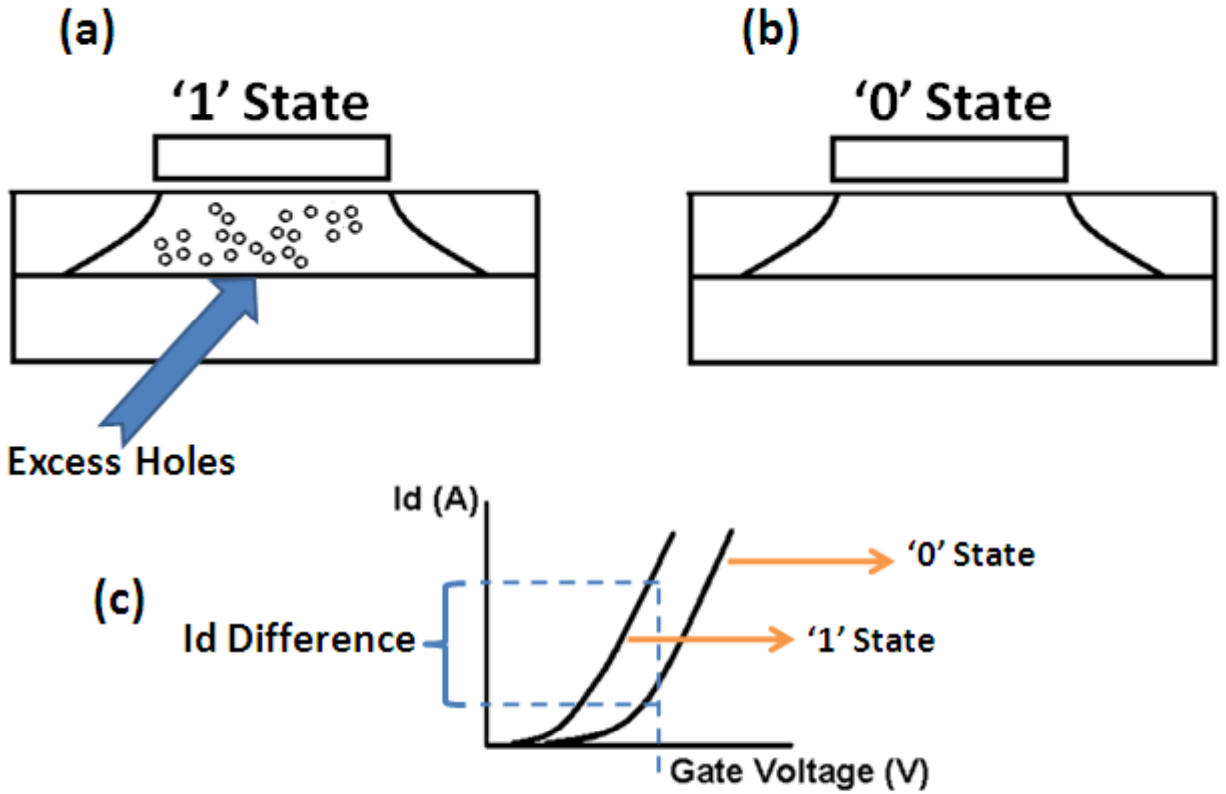
1T-DRAM: Operation Principles

The cell senses whether holes accumulate in the floating body as the threshold voltage (V_{th}) changes.
The source is set to 0 volt, the drain is connected to a bitline (BL), and the gate is connected to a wordline (WL).



Comparison

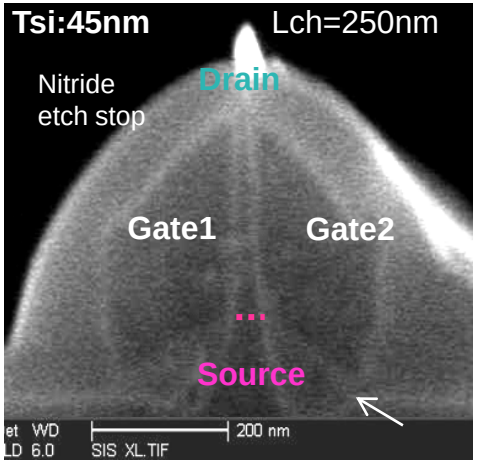
- **Comparison of features of various memories**

	1T QW DRAM	1T DRAM	DRAM	SRAM
Structure	1T	1T	1T/1C	6T
Cell Size	$4F^2$	$4F^2$	$8F^2$	$100F^2$
Storage	Quantum Well	Floating Body	Capacitor	Flip Flop
Speed	Fast	Fast	Fast	Ultra Fast
Read	Non destructive	Non destructive	Destructive	Non destructive
Scalability Issues	Lithography	Lithography Volume reduction	Capacitor	6T size
New Materials	Ge, SiGe, III-V	None	High K	None

What we did?

- **We experimentally demonstrated and characterized a vertical (current flow perpendicular to the wafer) source (bottom)/drain (top), double gate (DG) capacitorless-single transistor DRAM on a bulk silicon wafer.**

The front MOS structure <= conventional switching transistor
The back MOS structure <= to create the floating body storage node.
By reverse biasing the back gate => obtain a memory operation even for the scaled fully depleted devices.



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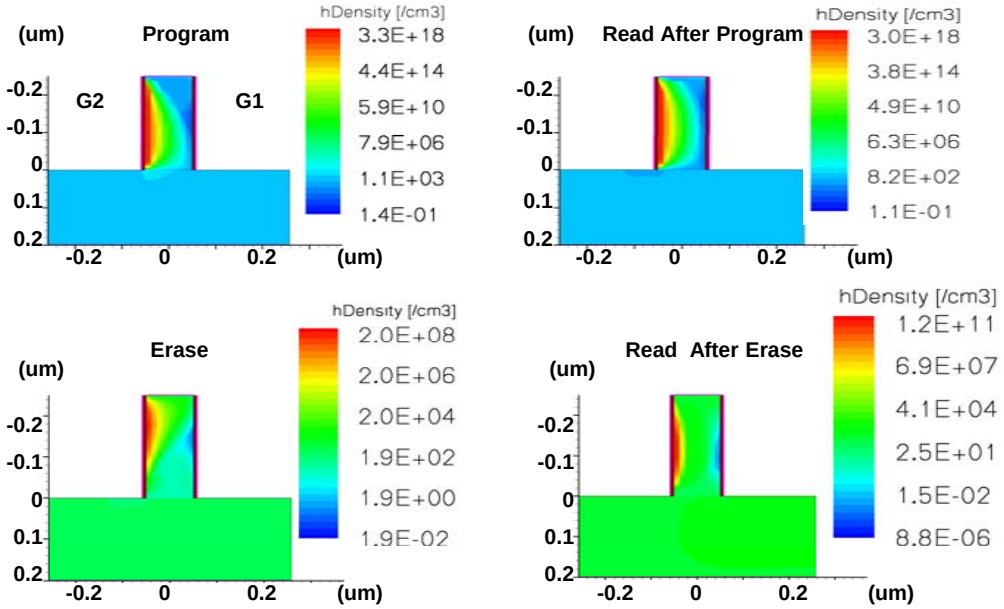
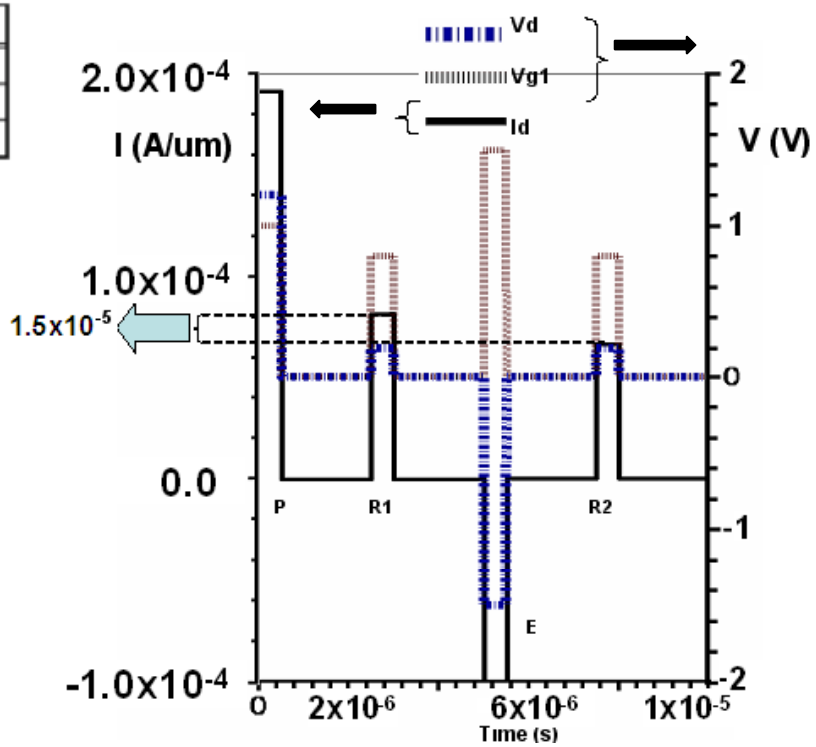
Sentauros Simulation Results:

- **1T DRAM operation**
- **A clear difference in Id for R1 and R2 (~15μA) confirms a memory.**

	Program (Write "1")	Erase (Write "0")	Read	Hold
Gate 1 Voltage (V)	1	1.5	0.8	0
Drain Voltage (V)	1.2	-1.5	0.2	0
Gate 2 Voltage (V)	-1.5	-1.5	-1.5	-1.5

Table shows the operating voltages for the DRAM cell





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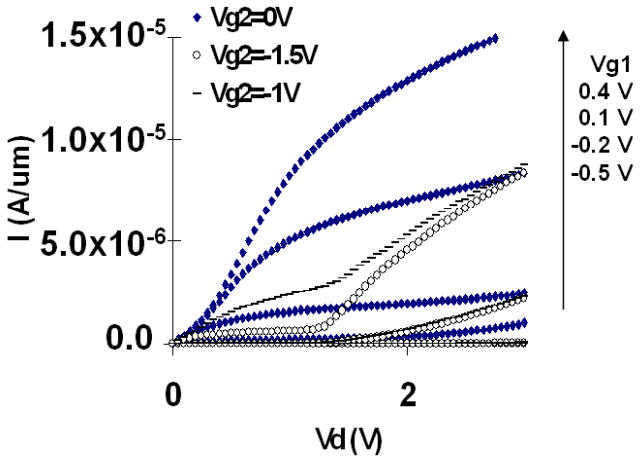
Experimental Data: I_d vs. V_d

Figure shows the onset of kink effect caused by excessive hole accumulation aided by negative Vg2.

Also, experimentally: A 3-6μA/μm Id difference between fresh and programmed cell reads is maintained up to 10ms; whereas a sensed current difference is ~1μA/μm after 25ms of retention.



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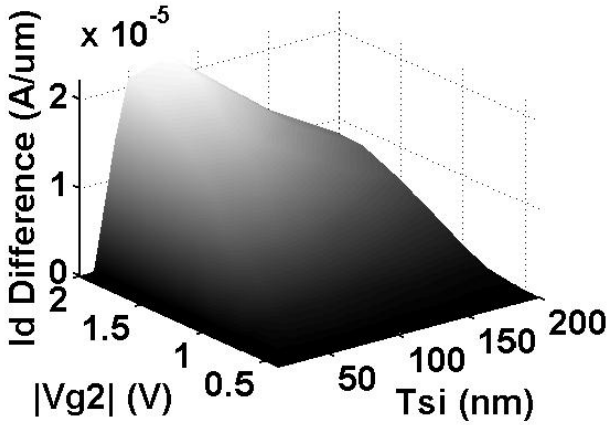
Simulation:



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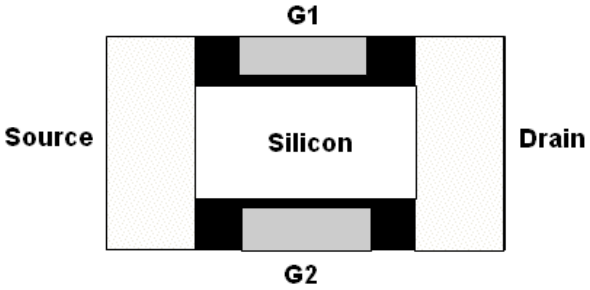
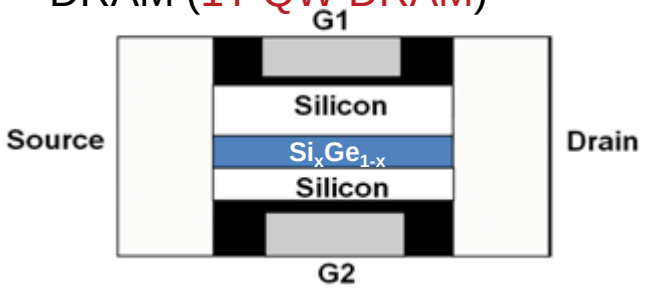
Novel 1T-QW DRAM

- **We propose a new kind of capacitorless DRAM: 1Transistor-Quantum Well structure:**
  - **"storage pocket"**
  - **opportunity to engineer spatial hole distribution within the body of the device**

Double Gate Single Transistor Capacitorles DRAM



Double Gate Quantum Well Single Transistor Capacitorles DRAM (1T-QW DRAM)



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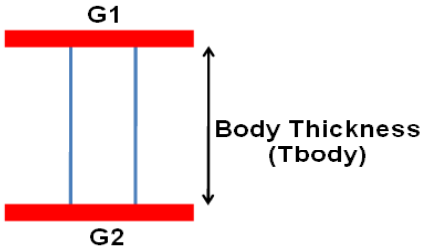
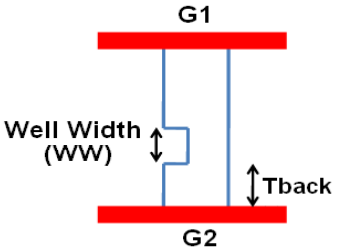
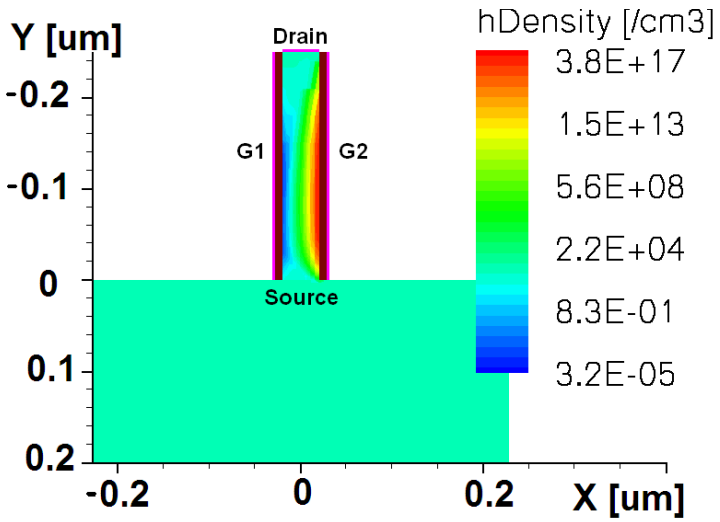


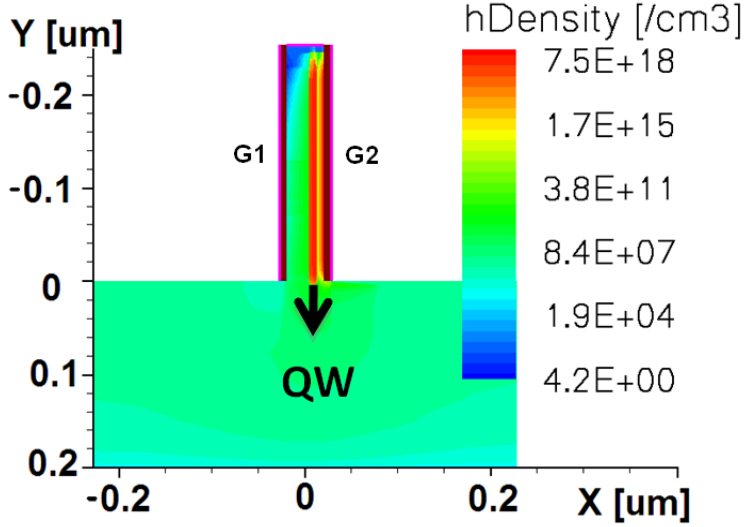


Spatial Hole Distribution Engineering

Hole Density during Program (Tbody=40nm, No Quantum Well).



Hole Density during Program in the device with Quantum Well (Tbody=40nm, Tback=10nm).



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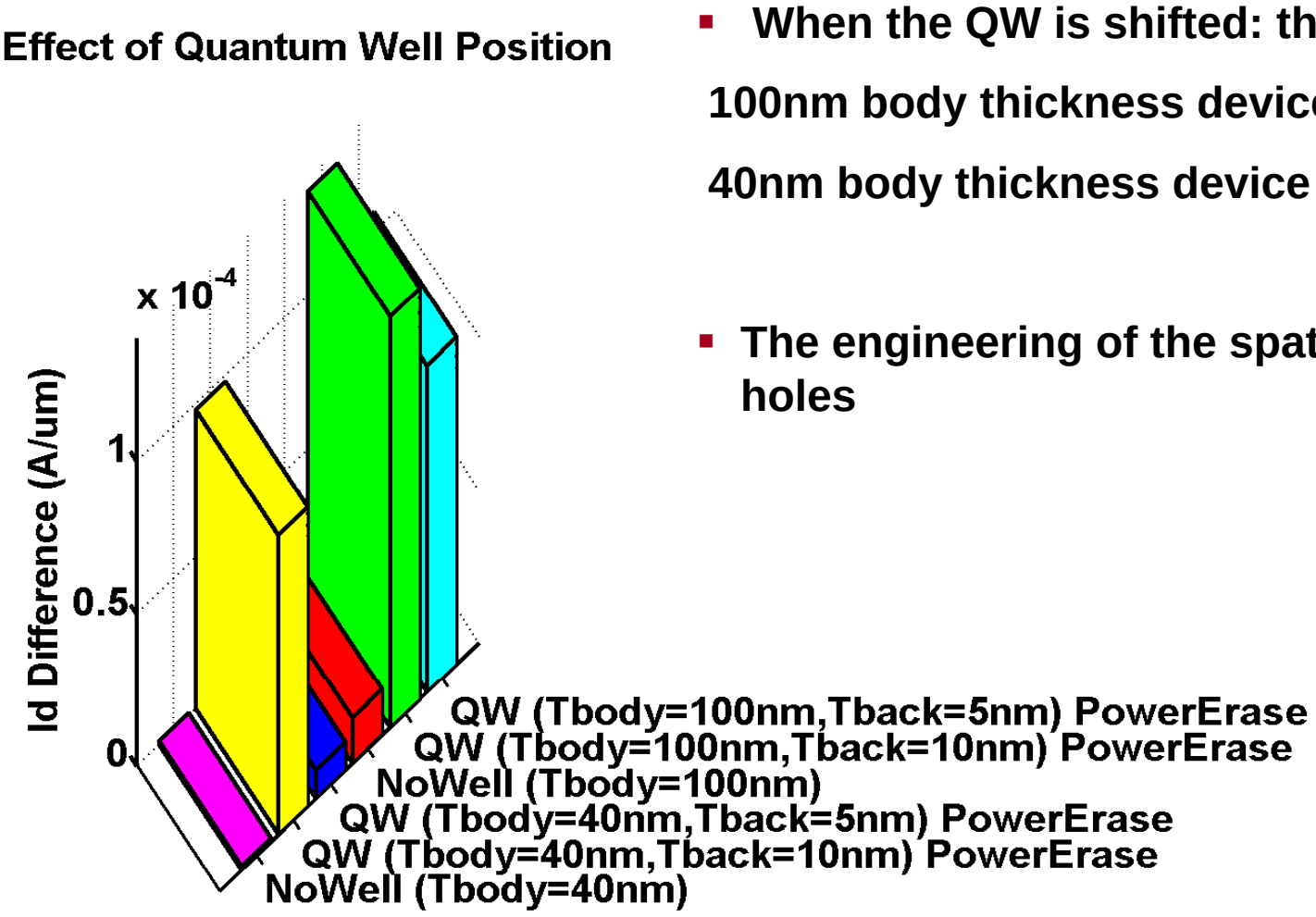
Effect of QW position:



- **When the QW is shifted: the improvement:**

100nm body thickness device 7x => 9x

40nm body thickness device 8x => 86x

- **The engineering of the spatial distribution of holes**

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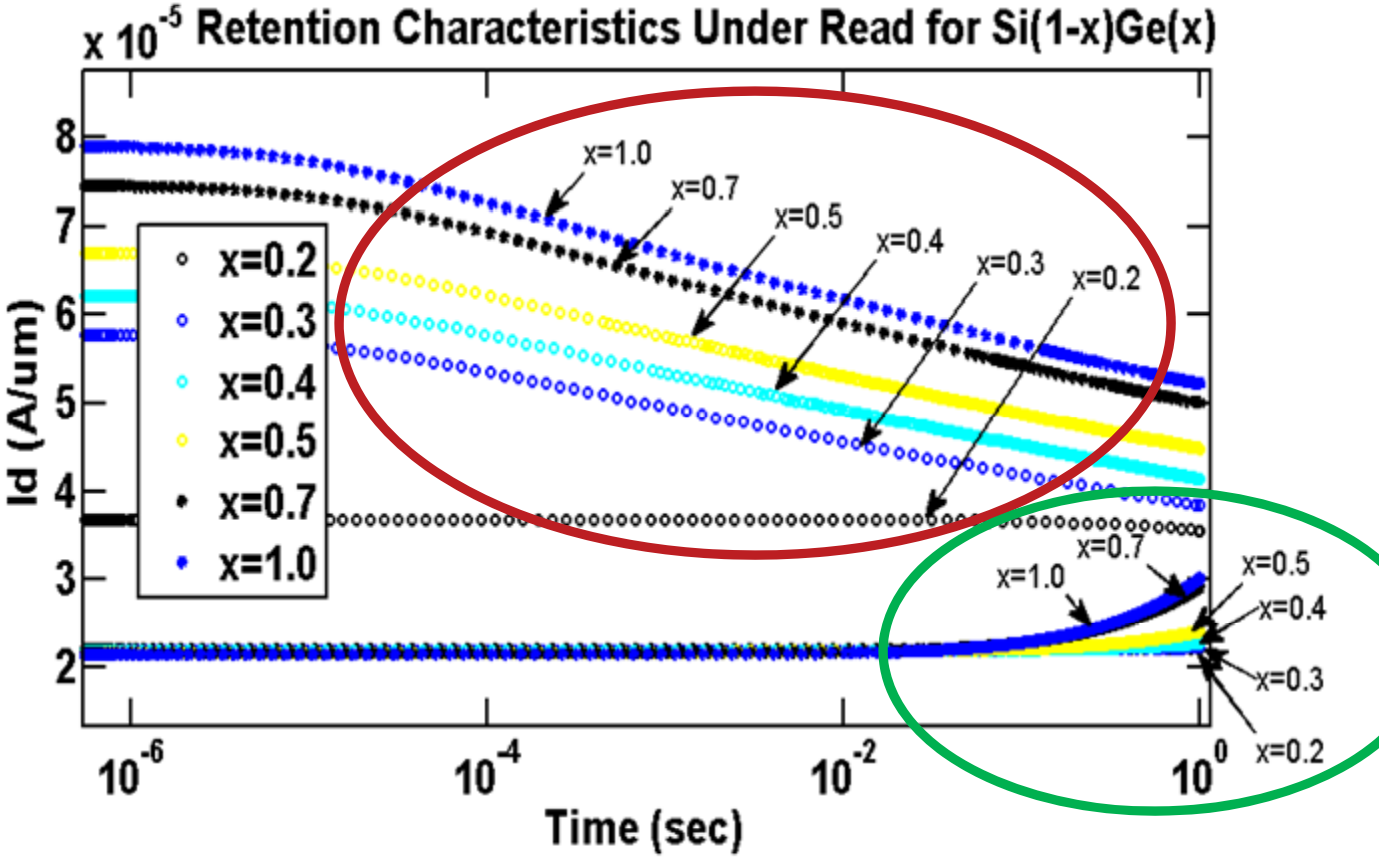
Retention: Ge Content

SiGe:

i) **Improvement in erased state degradation**
ii) **Reduction in the need for PowerErase**
iii) **Easier fabrication**



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Conclusions

	1T DRAM
Structure	1T
Cell Size	$4F^2$
Storage	Floating Body
Speed	Fast
Read	Non destructive
Scalability Issues	Lithography Volume reduction
New Materials	None

Vertical DG 1T DRAM

1T QW DRAM

We have experimentally shown:

- For the first time a vertical double gate (DG) capacitorless-single transistor (1T) DRAM
- on a **bulk silicon** wafer,
- fabricated with process innovations

- **Double Gate Capacitorless DRAM is analyzed.**
- **A novel single transistor double gate quantum well DRAM (1T QW DRAM) is introduced.**
- **This new DRAM has several advantages in terms of performance and scalability.**
  - "storage pocket" within the device.
  - possibility of engineering the spatial distribution of the holes
  - ability to have higher V_t shift and also retention values
  - better candidate for scaled new technology nodes.