Z-RAM® Floating Body Memory: Materials, Devices and Processes

Pierre Fazan

Innovative Silicon

1015 Lausanne, Switzerland

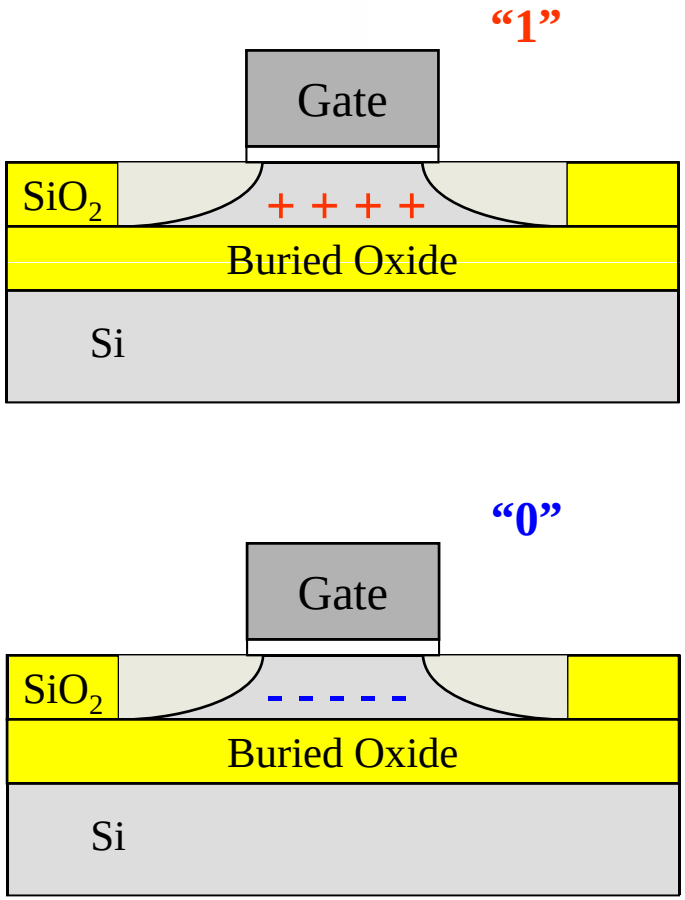
Outline

- Introduction:
  - Floating Body Memory
  - Z-RAM® Floating Body Memory
  - Applications
- Z-RAM Floating Body memory Roadmap
- Materials used
- Devices considerations
- Processes integration
- Conclusion

Floating Body Memory (FBM)

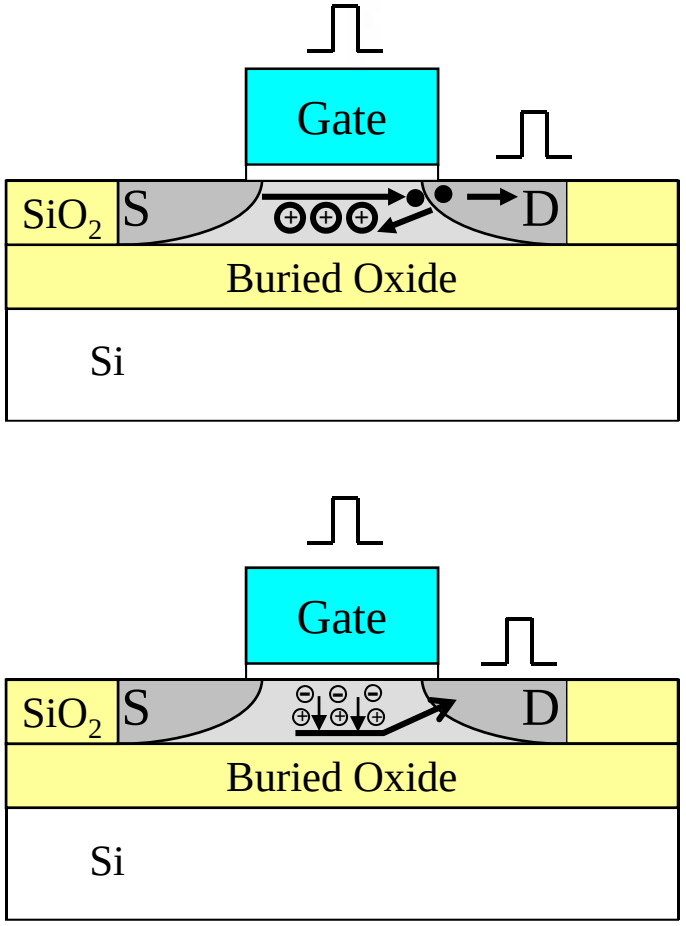
- Exploit isolated (SOI or others) transistors Floating Body (FB) effect
- FB is used as a storage node
- Presence of carriers (holes) in FB defines a 1st memory state
- Emission of carriers (holes) by junction forward biasing defines a 2nd memory state
- Vt difference, current sensing
- Under development & qualification by many (ISi, AMD, Intel, Hynix, Samsung, Toshiba, Fujitsu, ST Micro,...)

Ex: NMOS



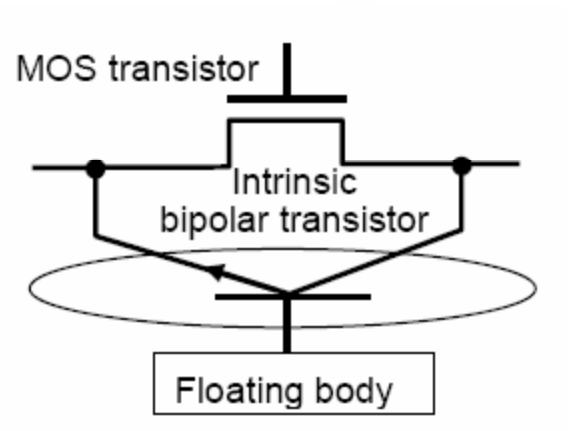
History: 2001: FBM

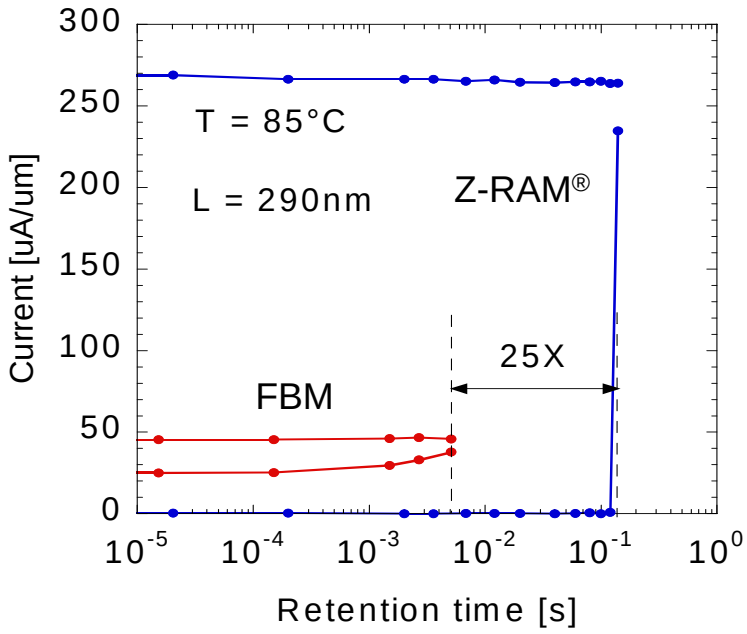
- 2001: 1st bit addressable memory proposed by S. Okhonin et al. (Innovative Silicon), IEEE SOI Conf. Positive biases
- 2002: T. Ohsawa et al. (Toshiba), ISSCC Conf. Positive & Negative biases
- Both states obtained by pulsing 2 terminals: possibility to create bit addressable memory
- Write state “1” by MOS impact ionization
- Write state “0” by junction forward biasing
- 3 ns operation demonstrated by ISi



History: 2007: Z-RAM® Floating Body Memory

- 2007: bipolar mode operation by S. Okhonin et al. (Innovative Silicon), IEDM Conf.
- BJT operation for write & read, hold in accumulation
- Key advantages: more margin, longer retention time, higher read current, lower power, less variability, more scalable (PD, FD, 3D)
- Named Z-RAM® floating body memory by Innovative Silicon

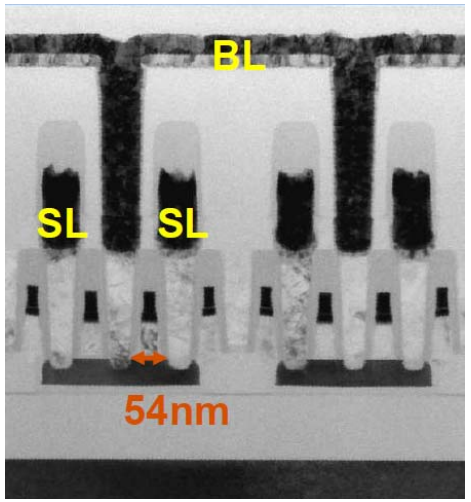




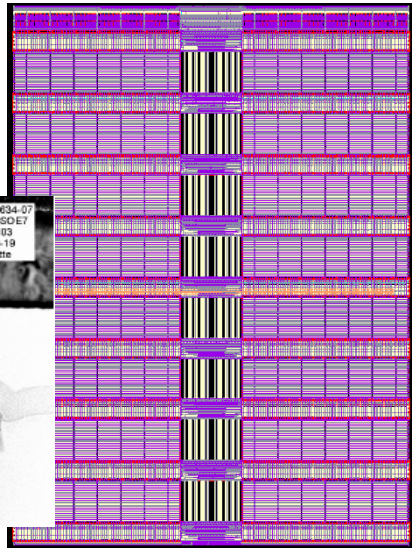
Applications

- Standalone DRAM replacement
  - 4 to 6F^2 cell
  - Memory technology
  - Hynix/ISi VLSI Symp. 2009
  - 54 nm demonstrator
- Embedded DRAM & SRAM replacement
  - 35 to 45 F^2 cell
  - Logic technology
  - AMD/ISi ISSCC 2009
  - 45 nm demonstrator

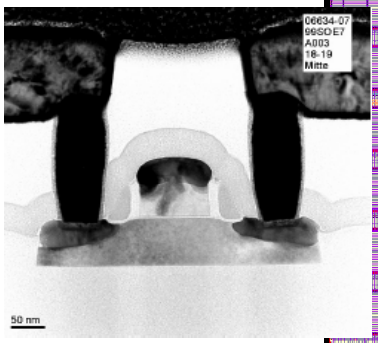
54 nm 6F^2 Cell



45 nm 4Mb Macro



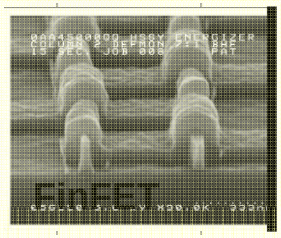
45 nm 45F^2 Cell

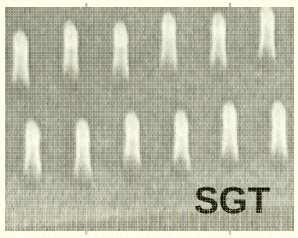


Z-RAM Floating Body Memory Roadmap

ITRS Year	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Z-RAM ½ Pitch (nm)	58	50	45	40	36	32	28	25	22	20

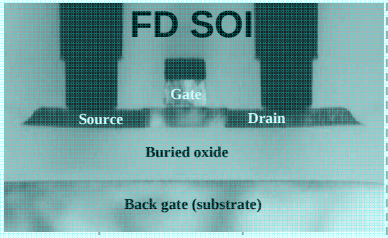
Standalone Memory Application





Planar SOI → 3D Devices on Bulk Si

Embedded Memory Application

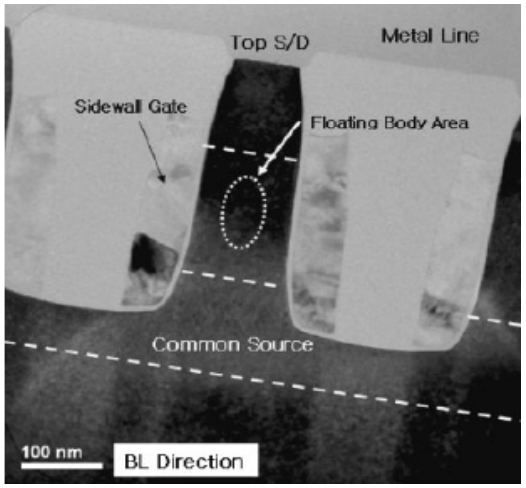


Planar Devices on SOI

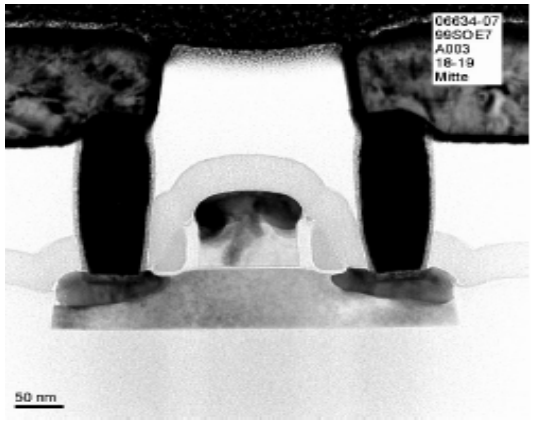
Materials Challenges

- Standalone applications
  - 3D devices, engineered substrates
  - Low R gates, contacts & lines (WL, BL, SL) in memory process
  - Quality of various interfaces (retention)
  - Reduced defects
  - Tight pitch contacts
  - Tight pitch low R interconnect
- Embedded applications
  - Engineered substrates
  - PD SOI
  - FD SOI: ultra thin Si and ultra thin Box
  - Quality of interfaces (retention)
  - Reduced defects

Source: Samsung

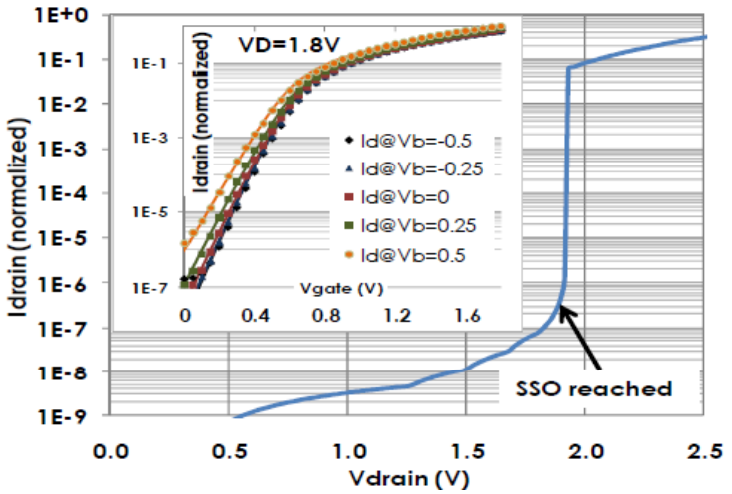


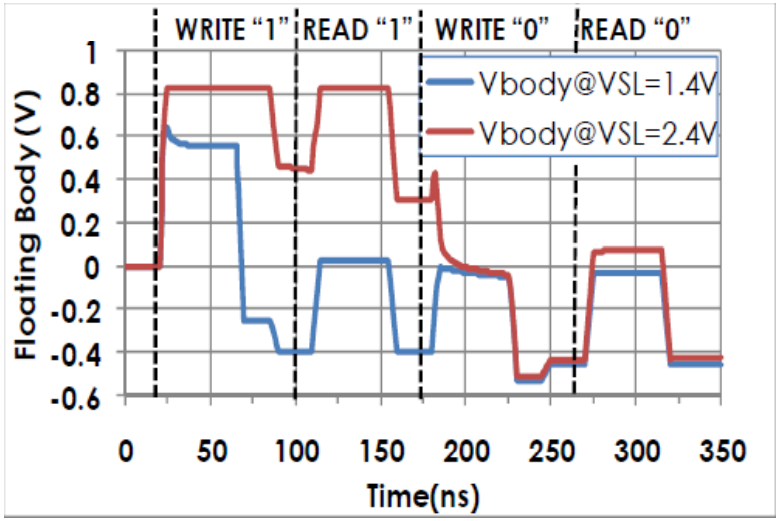
45 nm PD SOI Device



Devices Considerations

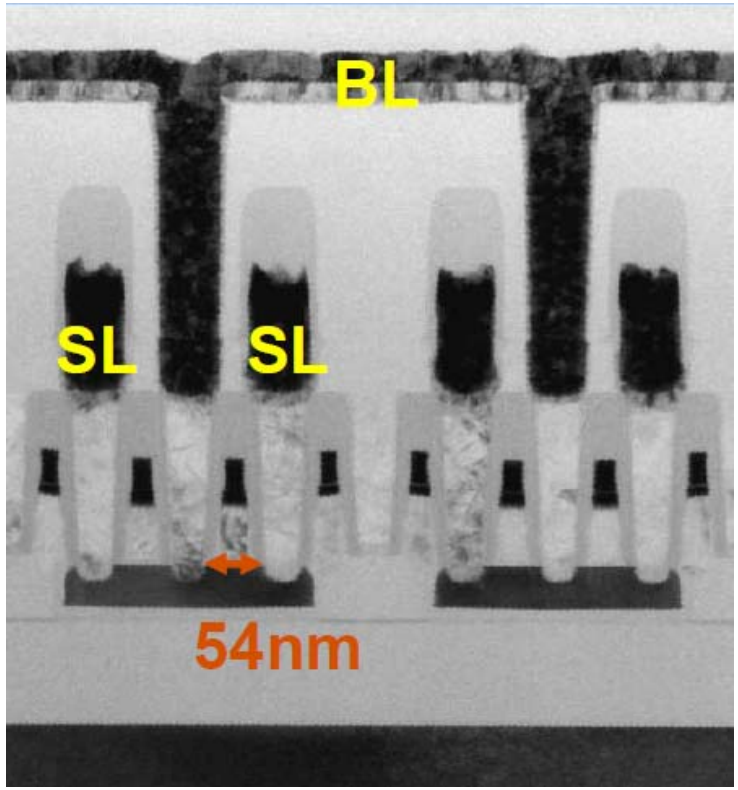
- Need to understand, develop and model various aspects of the memory operation:
  - MOSFET
  - Parasitic BJT
  - Charge generation
  - Leakage currents
- Spice and TCAD models
  - Predict Self Sustained Operation (SSO), write, read, programming window





Processes Integration

- Standalone applications
  - 3D structure integration
  - Optimum doping level for MOSFET, BJT, charge generation, leakage and various operation modes
  - Self Aligned Contacts
  - Tight pitch interconnect
- Embedded applications
  - Ultra thin Si device integration
  - Optimum doping level as above
  - Elevated S/D



Conclusion

- SRAM, DRAM scaling challenges
- 1T memory: simple solution
  - FBM
  - Z-RAM floating body memory
- Applications: standalone or embedded RAMs
- Materials challenges: 3D devices, Ultra thin SOI, data retention
- Devices optimization for various operation modes
- Process integration: 3D devices, density