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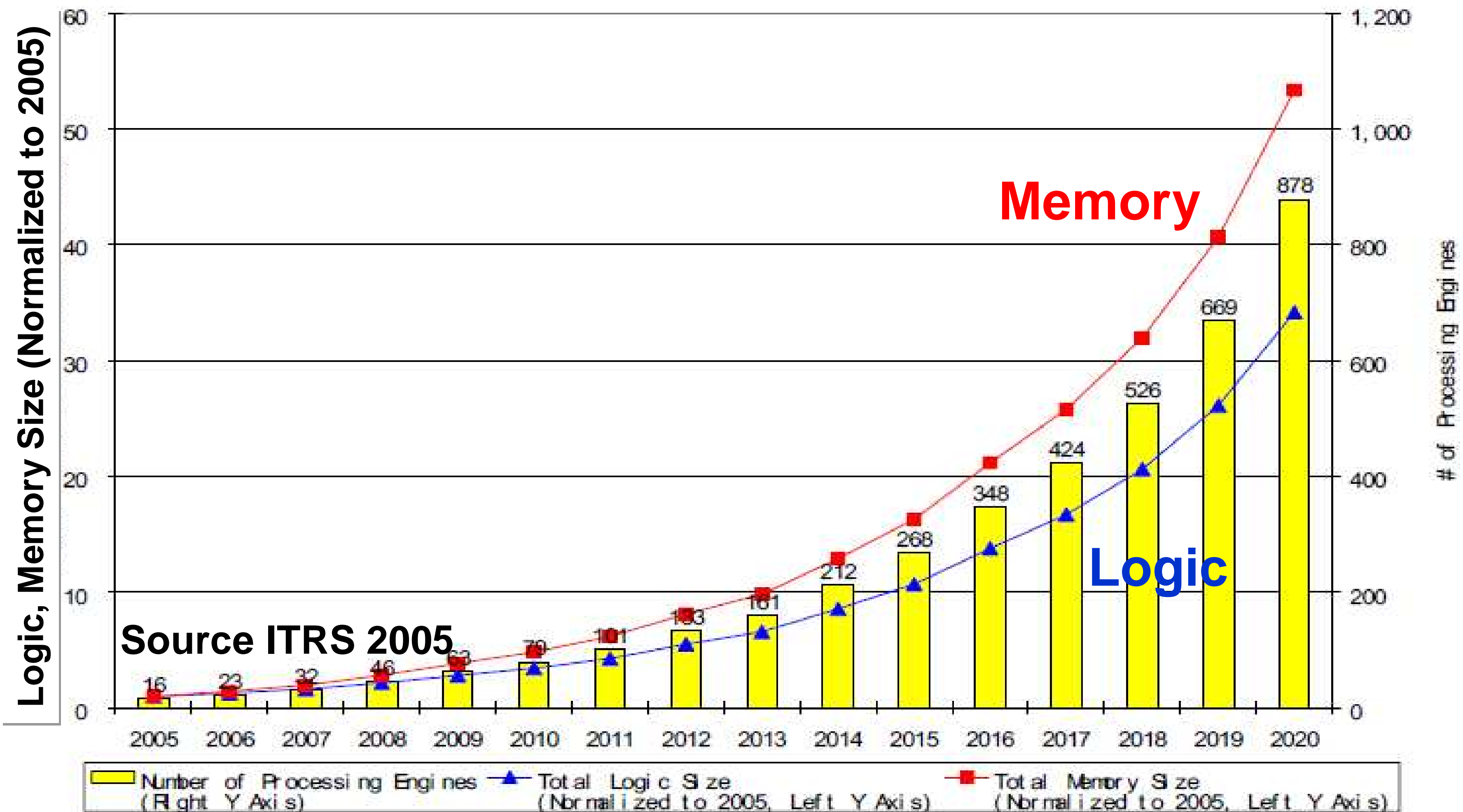
Challenges of the Integration of New Memory into CMOS Platforms

2009.10.20

NEC Electronics Corporation
Masao Fukuma

Memory in SoCs

- **The total memory size in SoC grows faster than total logic size.**



Embedded Memory

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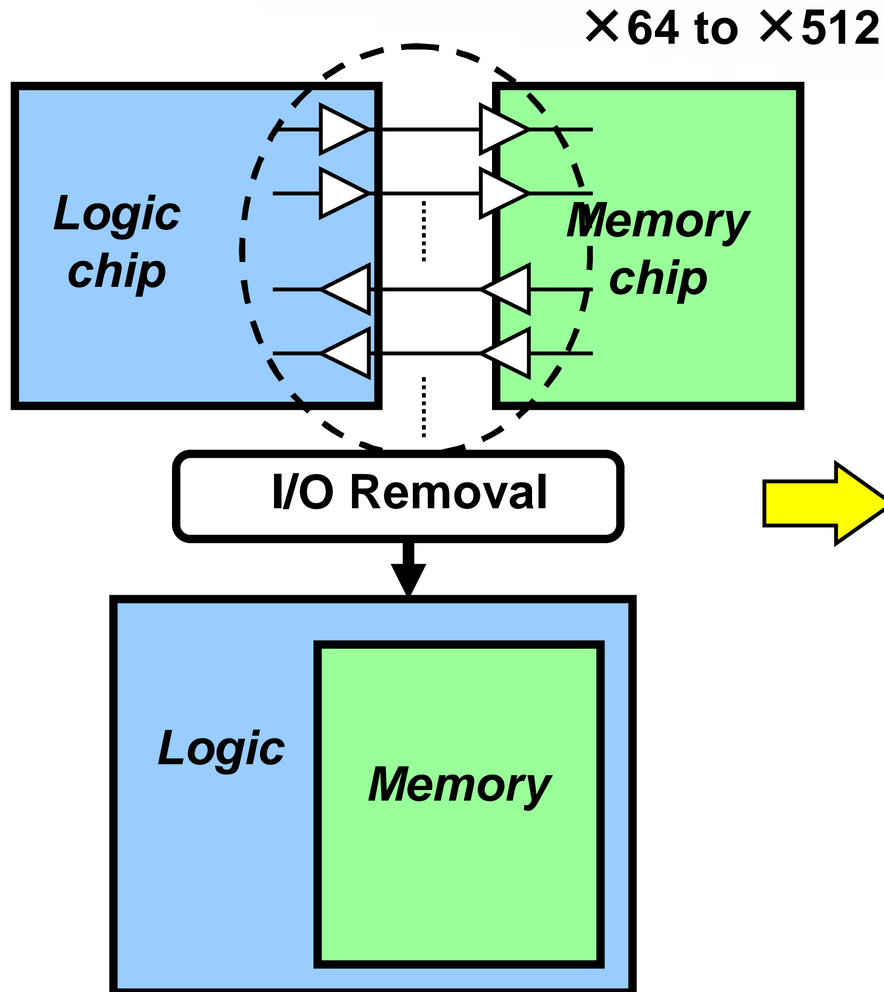
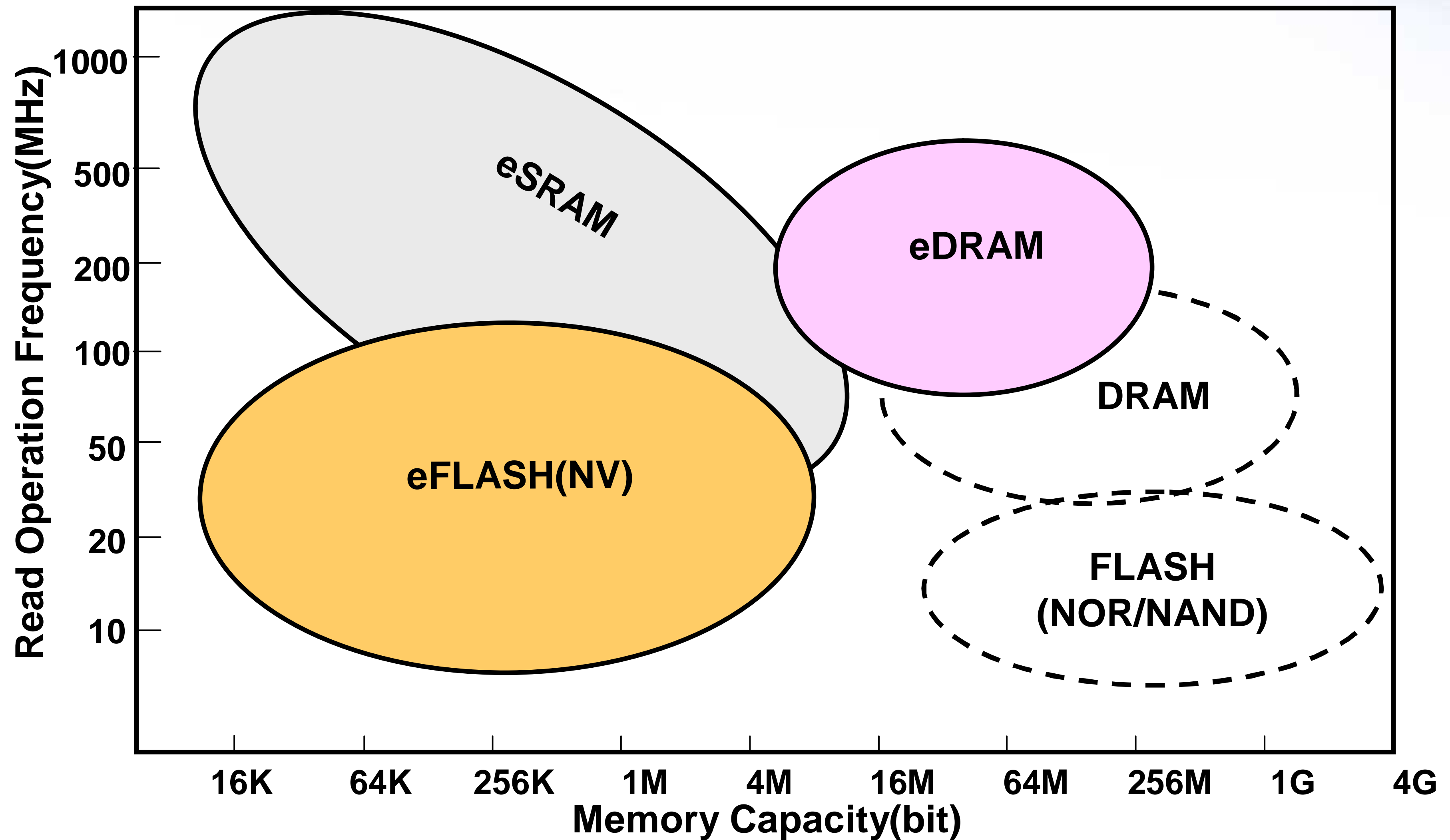
I/O Buffer: Logic⇔Memory Data Transfer

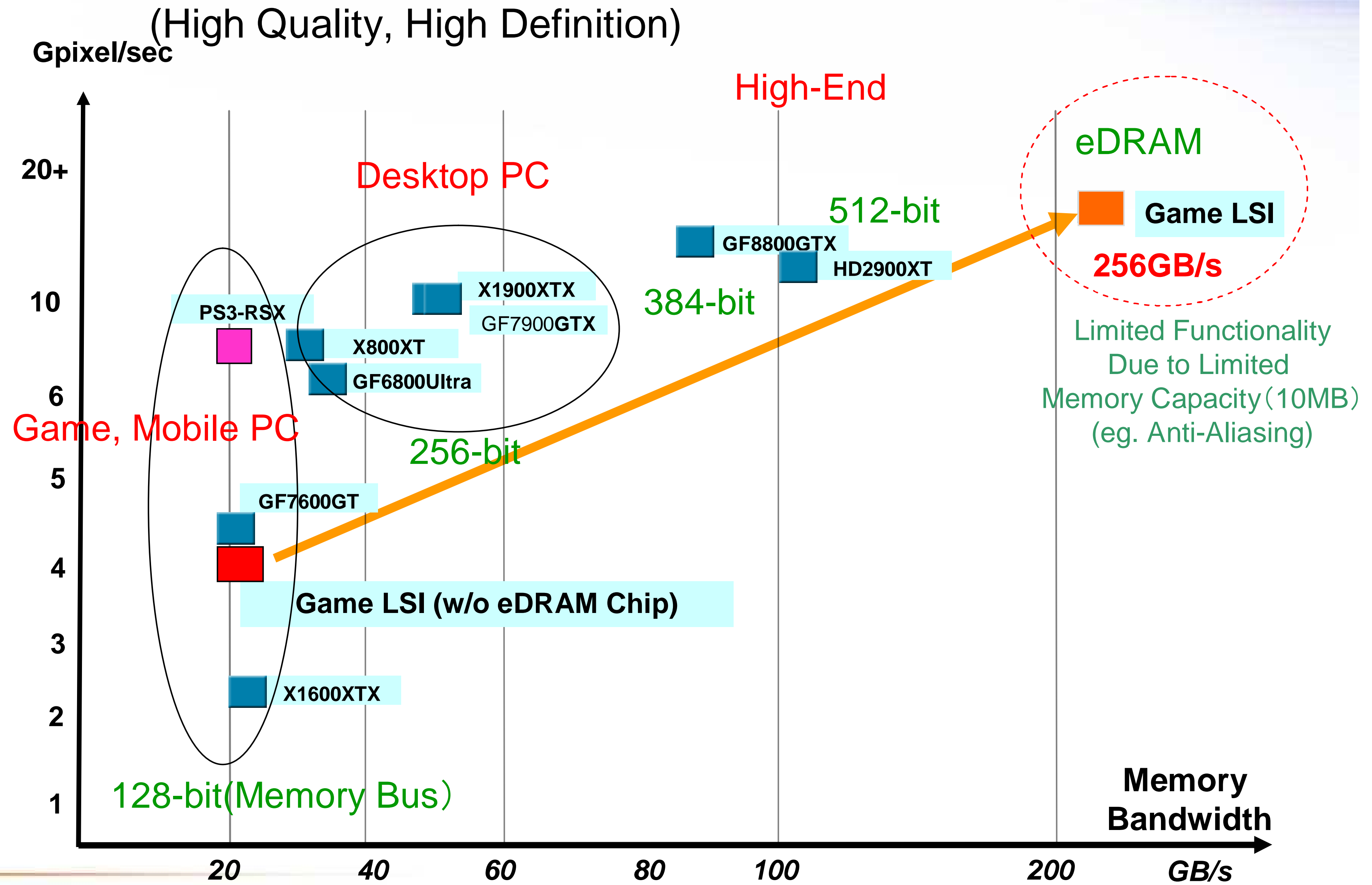


- ☑High Bandwidth
- ☑Low Power
- ☑Reduce PKG pin #
- ☑Reduce Board Area
- ☑Low Noise

Positioning of Embedded Memories



GPU Performance and Memory Bandwidth



55nm eDRAM

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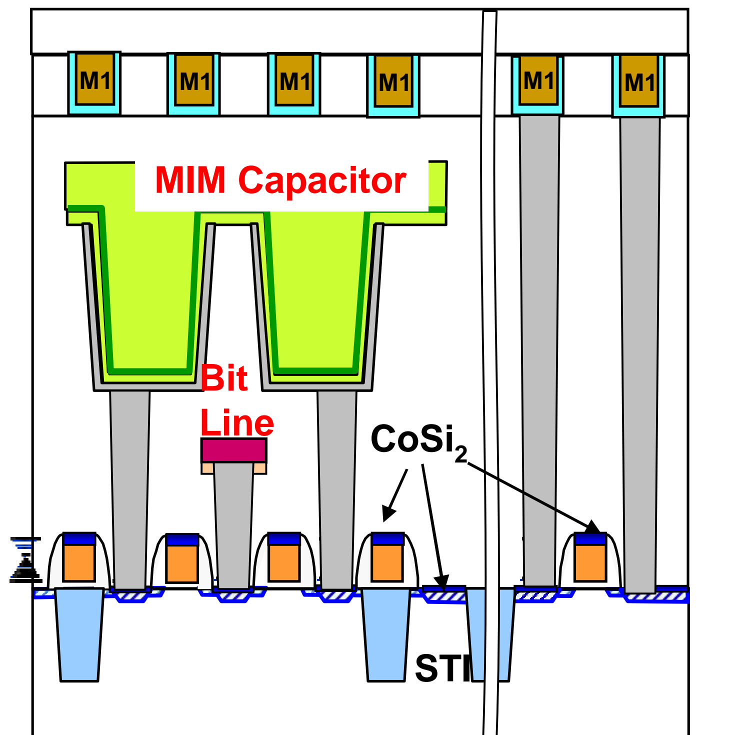
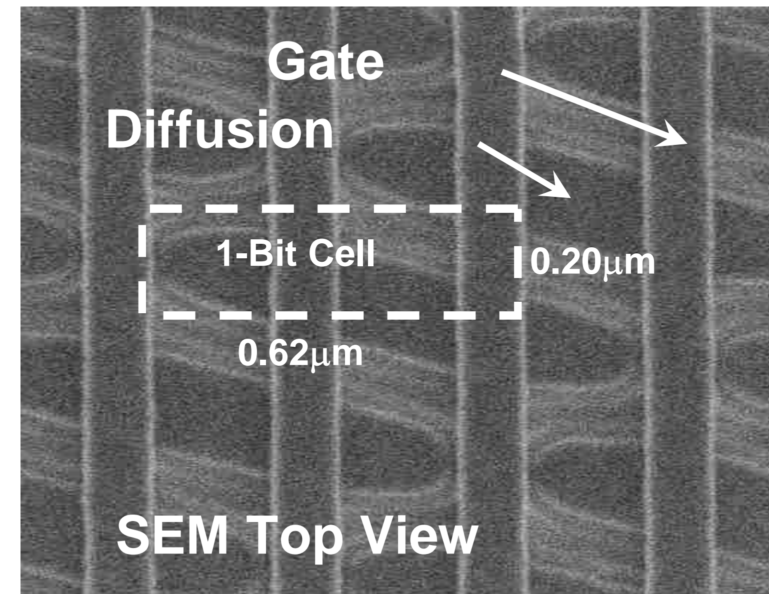
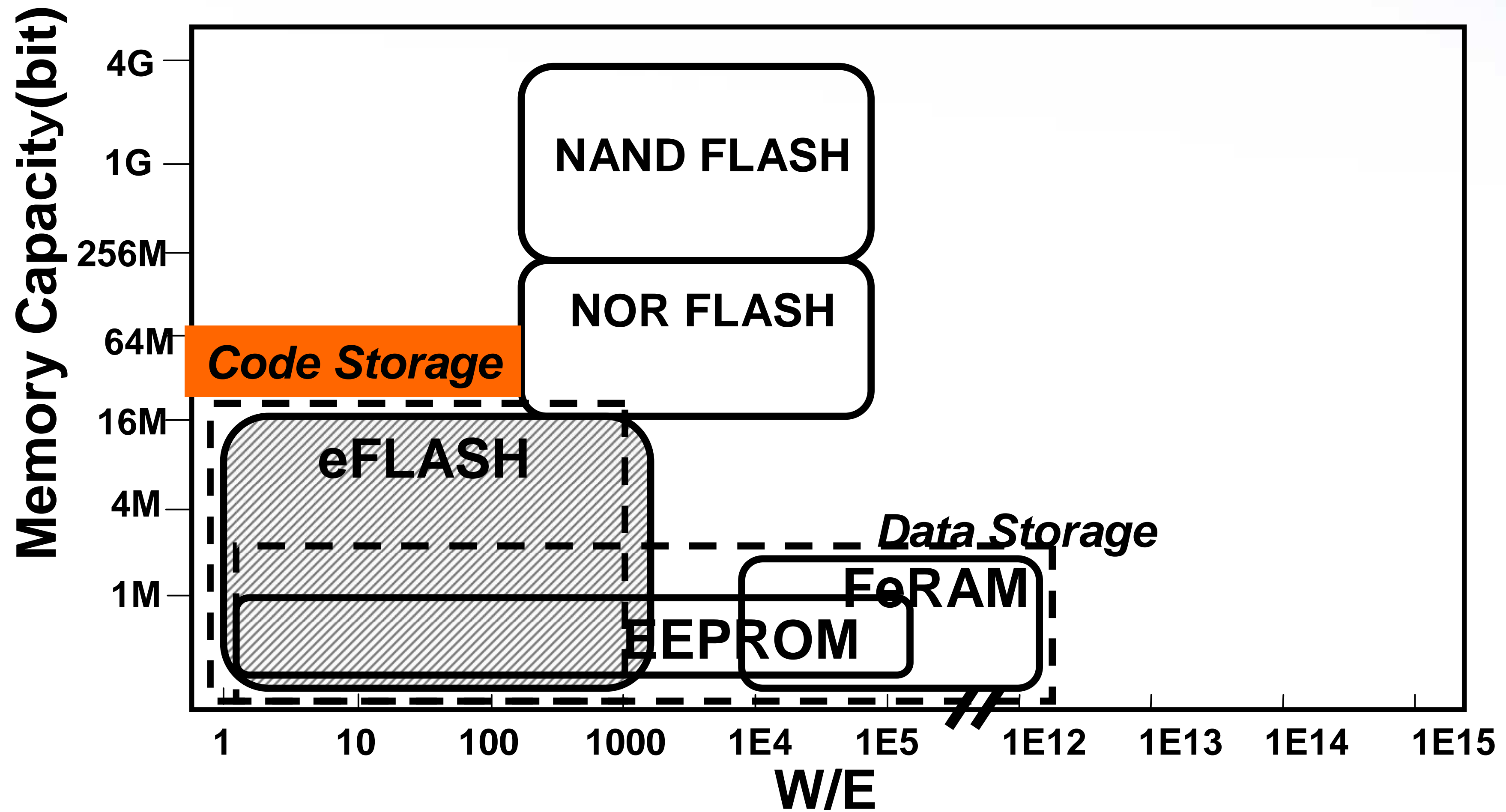
- FMD(Full-Metal Structure) enabling *high performance / low power*
- Low temperature MIM formation enabling *logic CMOS Tr. compatibiity*
- ZrO2 implementation enabling *low leakage/high capacitance* MIM





Embedded NV Memories



Embedded Memory Issues

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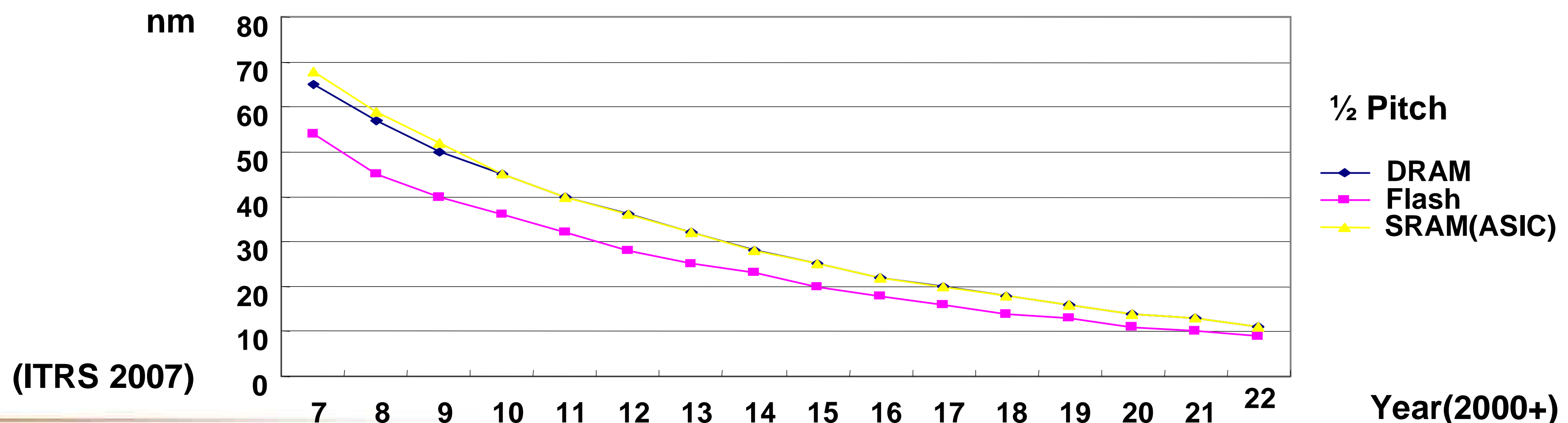
- **Limits of Scaling**
  - **eSRAM**
    - Large leak current, small operating margin, complicated Ckt
  - **eDRAM**
    - Size of storage capacitance, difficulty in low leakage Tr.
  - **eFlash**
    - Non-scalability of dielectrics, poor reliability

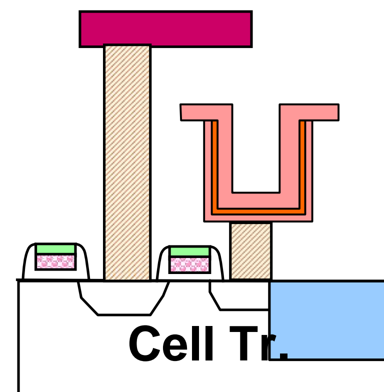
⇒ **New Memory**
BEOL base because of standard CMOS compatibility



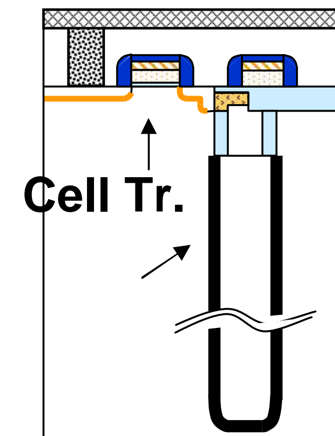
BEOL Memory Integration

- Memory Integration in Backend Process
  - CMOS Compatibility
  - Complexity Reduction

- CMOS Platform Compatible Flow and Structures
  - Memory Integration only at the Backend
    - × eDRAM (trench)
    - △ eDRAM (stacked)



eDRAM (trench)



eDRAM (stacked)

BEOL Memory Integration

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- New Memory Candidates for BEOL Integration
  - MRAM
  - ReRAM
  - FeRAM
  - PCRAM
  - NanoBridge

  ....

Process compatibility

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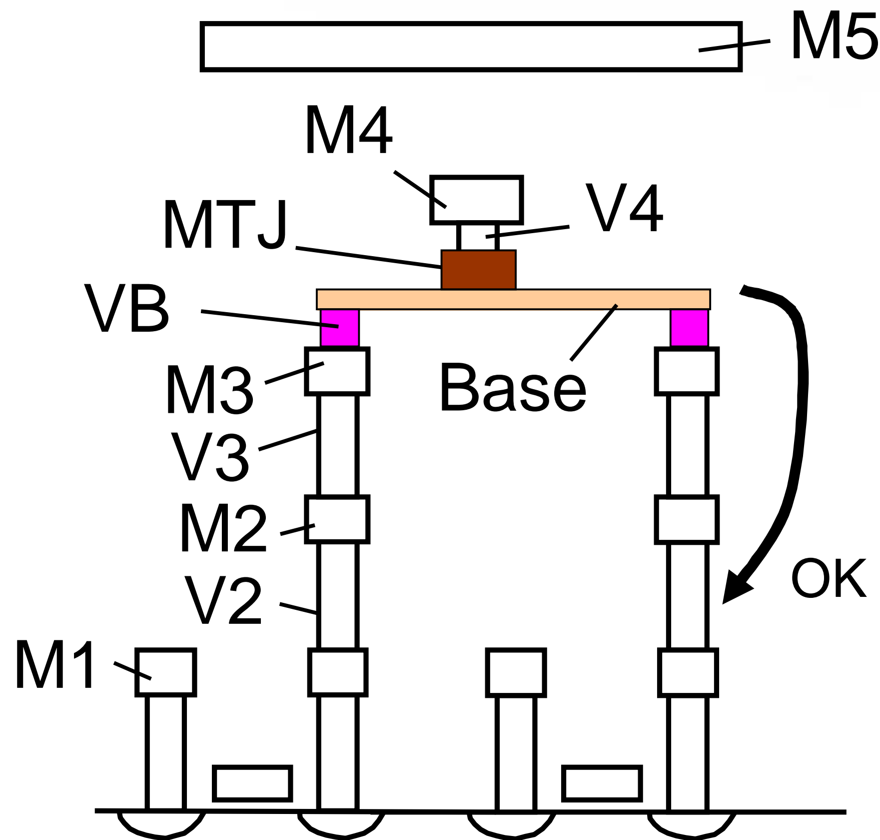
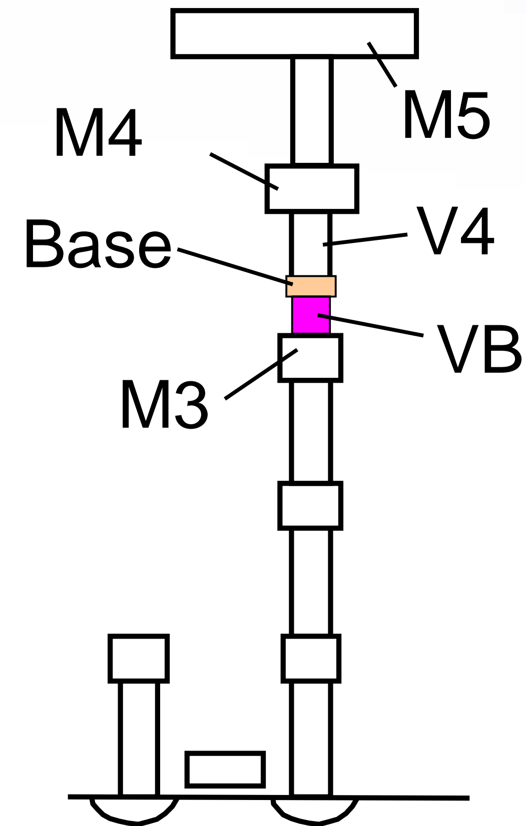
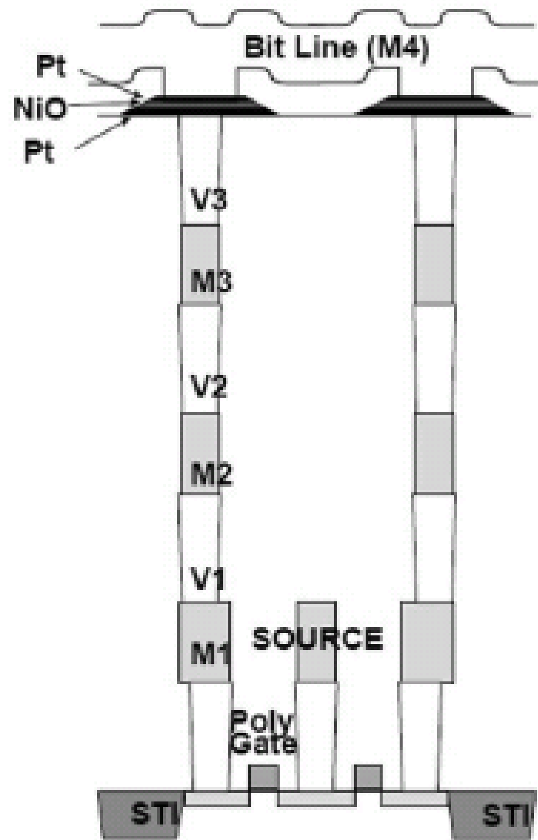
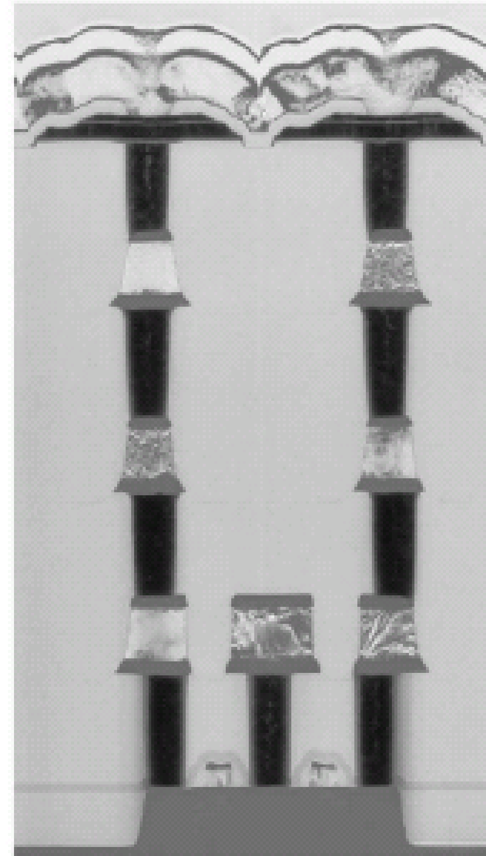




Added MRAM process: three mask layers,
no effect on logic circuits,
inserted in any interlayer over M1

ReRAM

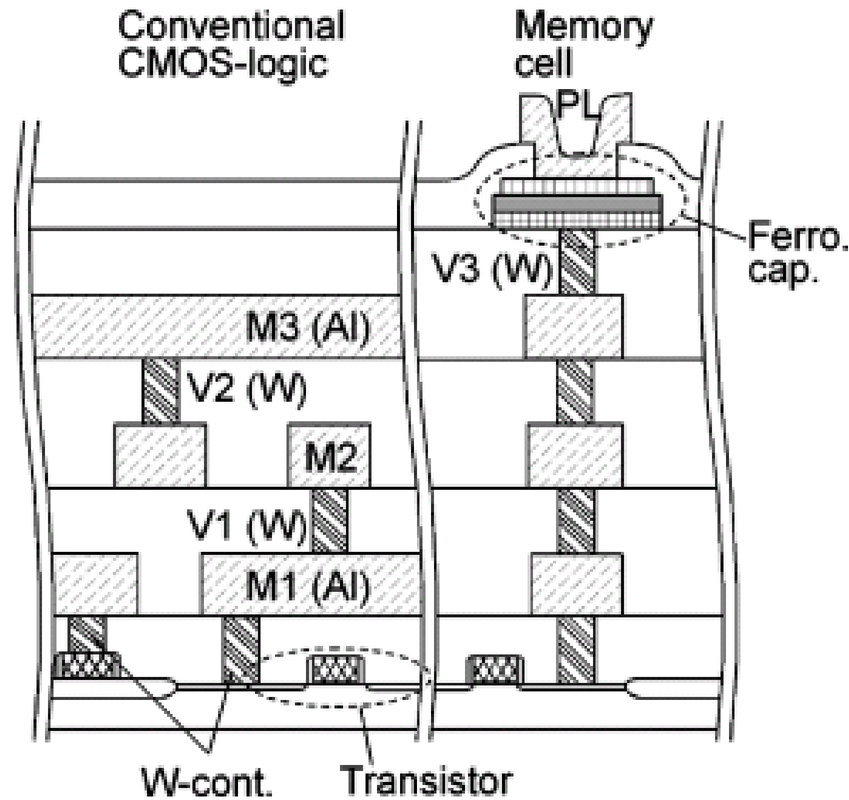


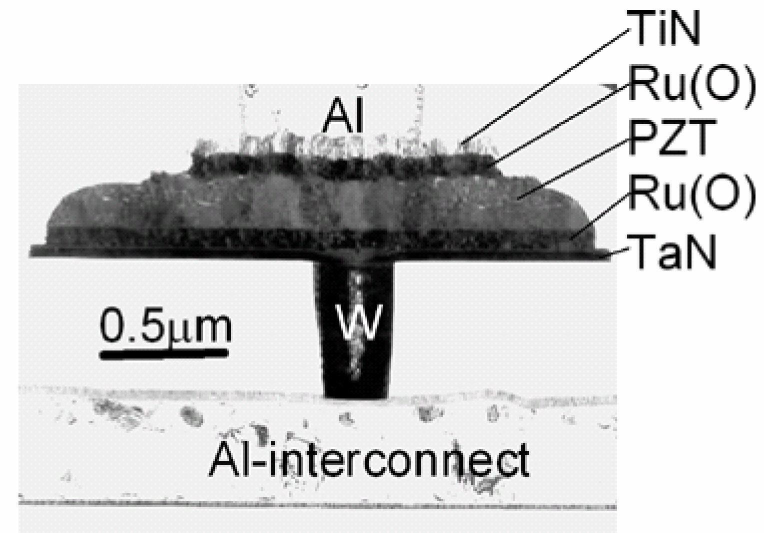


Sub-100-μA Reset Current of Nickel Oxide Resistive Memory Through Control of Filamentary Conductance by Current Limit of MOSFET

(Fujitsu, IEEE Trans. ED08)

FeRAM





PZT MIM Capacitor With Oxygen-Doped Ru-Electrodes for Embedded FeRAM Devices

（Hayashi, IEEE Trans.ED 05)

NanoBridge

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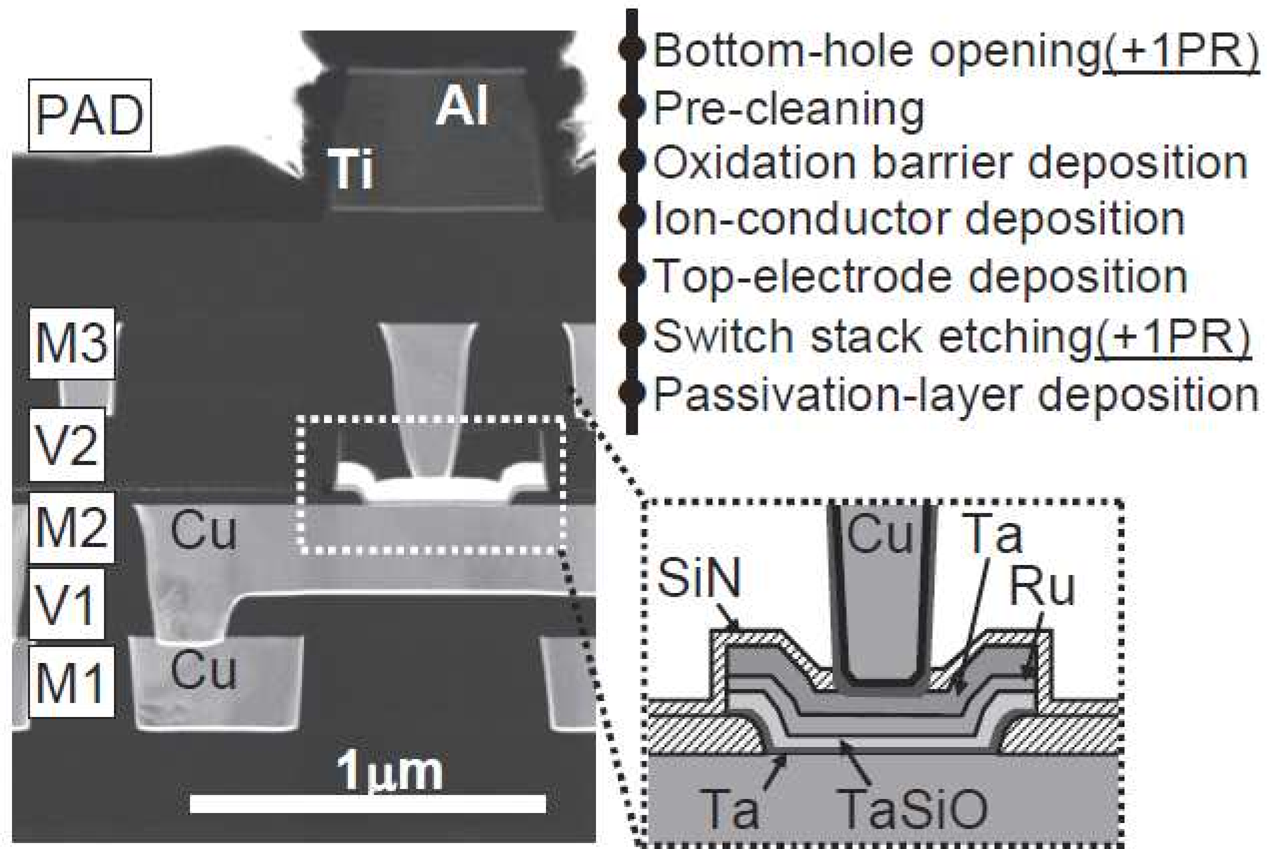

Nonvolatile solid-electrolyte switch embedded into Cu interconnect

(Sakamoto, VLSI Symposium 09)

BEOL Memory Integration Issues

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- **Process Flow Issues**
  - Temperature
  - Contamination
  - Etching Damage
  - Leakage
- **Structure Issues**
  - Damage
  - Layout Pattern Restrictions
  - Library Compatibility
  - Design Flexibility

A Solution for New Memory Integration

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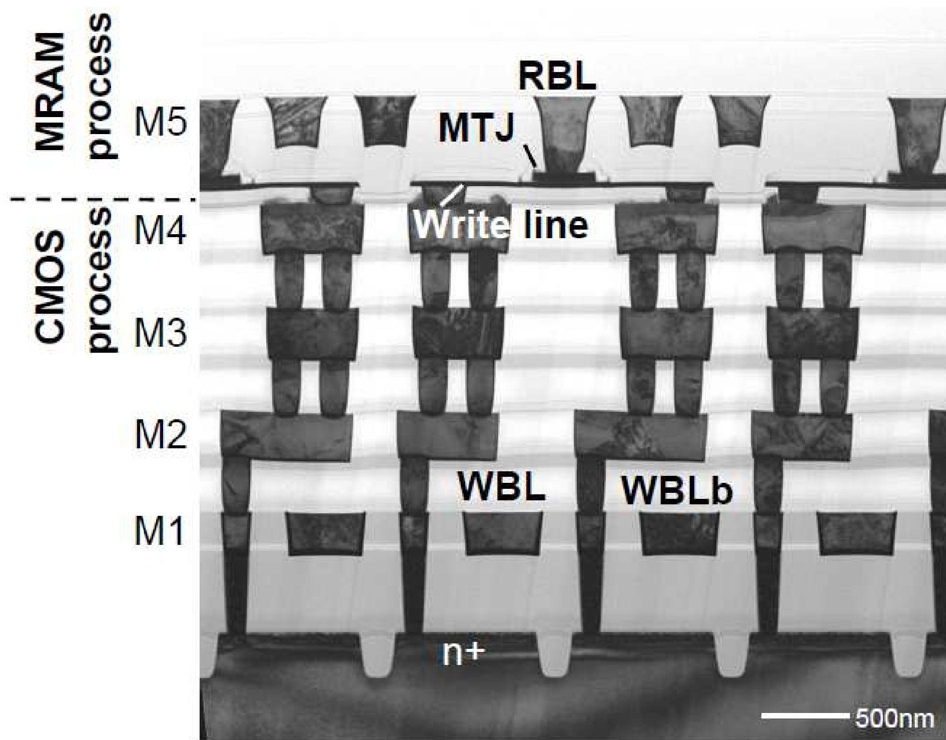
- Limits of conventional embedded Memories (eDRAM・Flash)

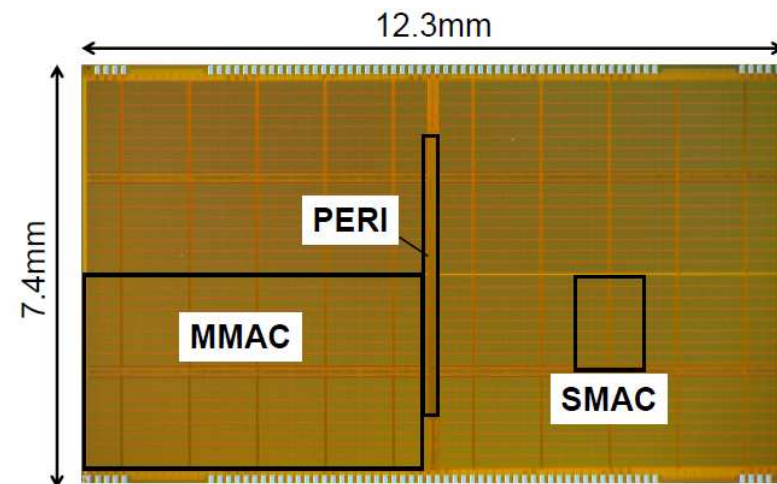
- Business Point of View: Separation of Frontend and Backend
  - Separation of Standard and Differentiation
    - Frontend (CMOS PF): Standard
    - Backend (Memory Integration): Differentiation
  - Cloud Manufacturing
    - Fab Virtualization for Frontend Manufacturing

- MRAM for Next Generation eMemory Device
  - BEOL memory
  - High Speed and Good Scalability
  - Non Volatile but No R/W Limitation

MRAM

- 32Mb 2T1MTJ MRAM chip
  - MRAM on 90nm CMOS
    - cycle time 12ns



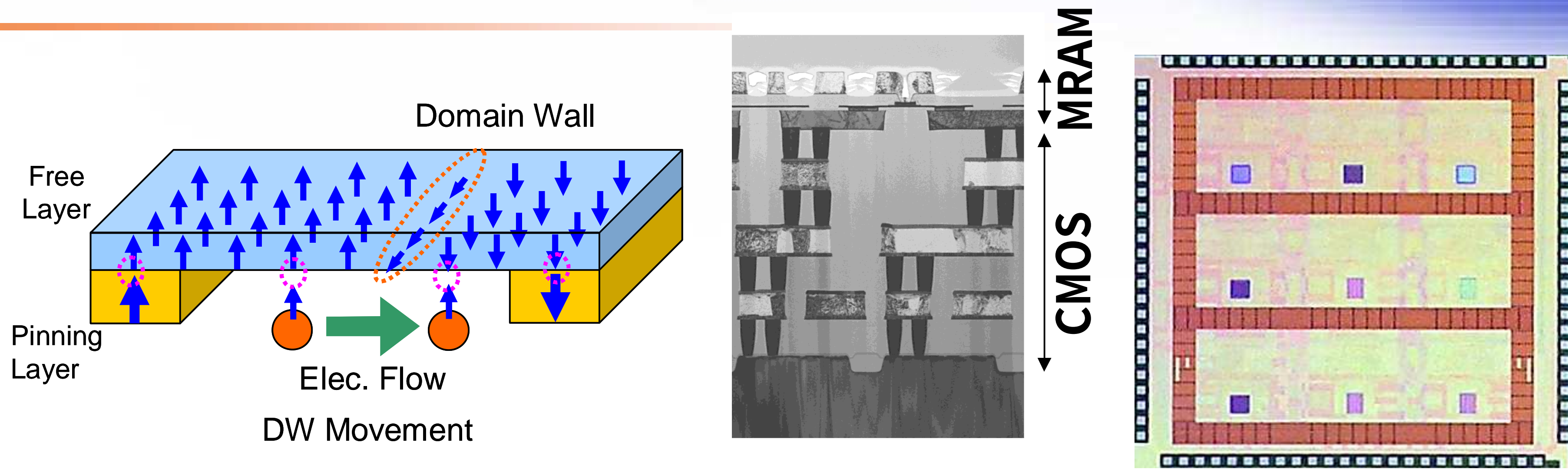


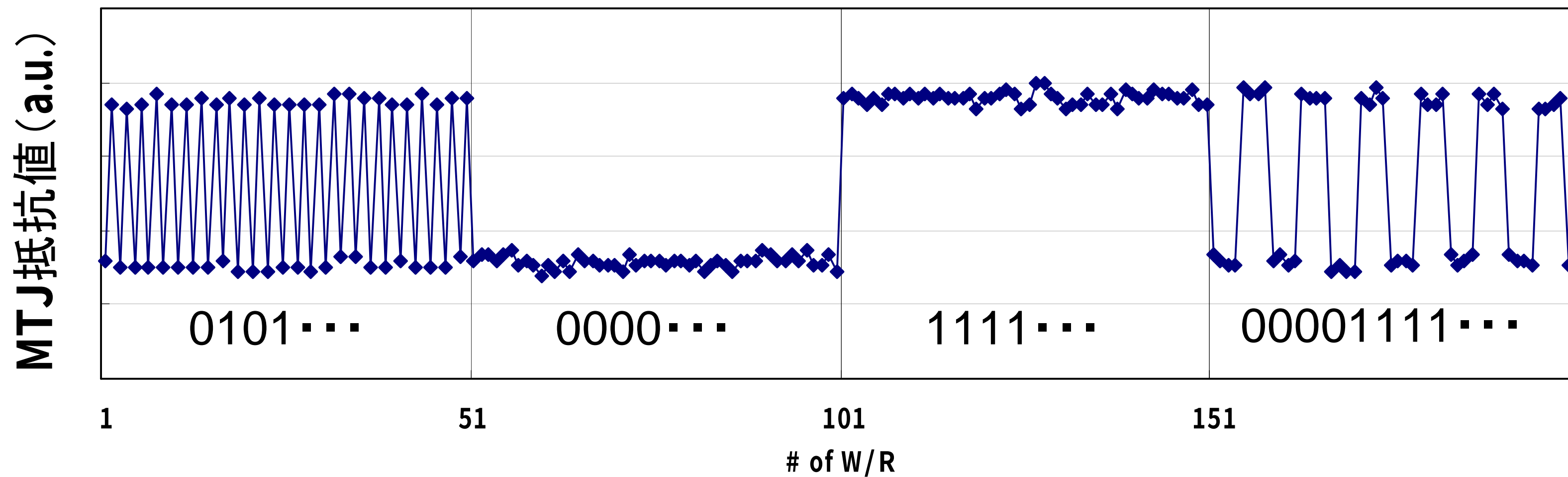
MMAC : 10Mb macro (8Mb+2Mb)
SMAC : Sub macro (1Mb)
PERI : Peripheral circuit

A 90nm 12ns 32Mb 2T1MTJ MRAM

(Nebashi, ISSCC09)

Domain Wall Movement Type





Embedded MRAM Contribution

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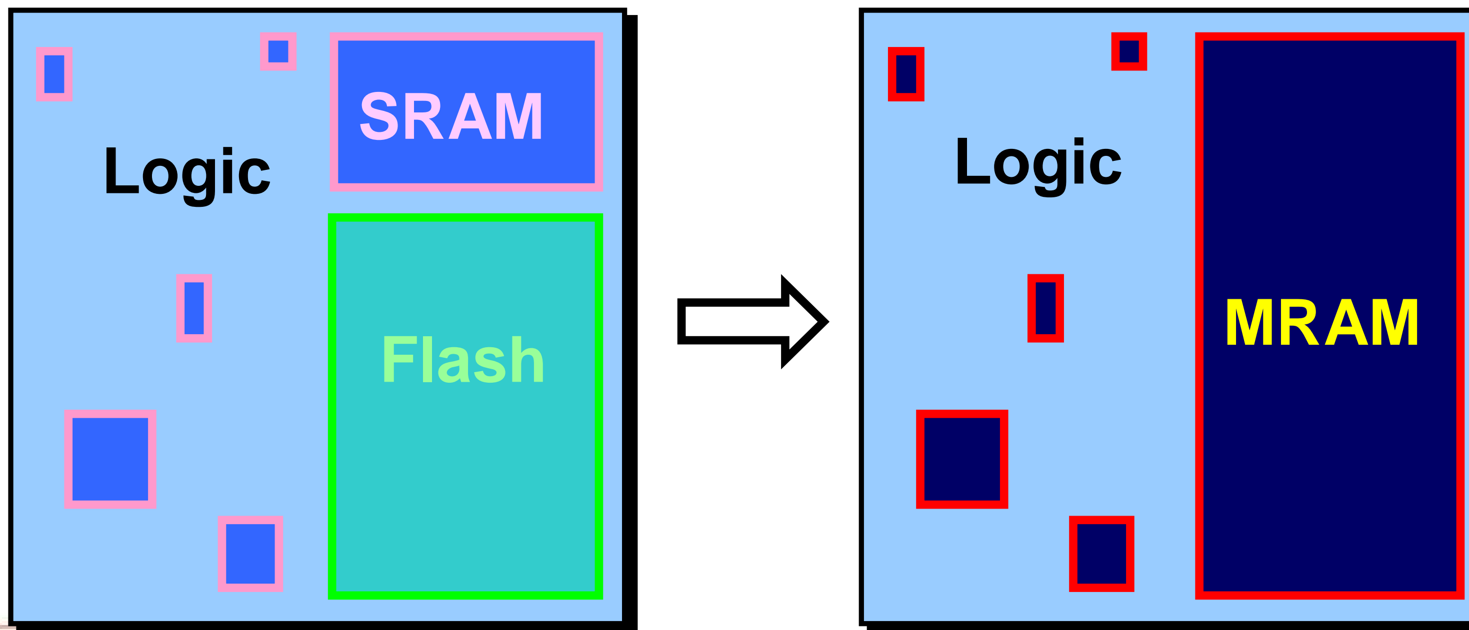
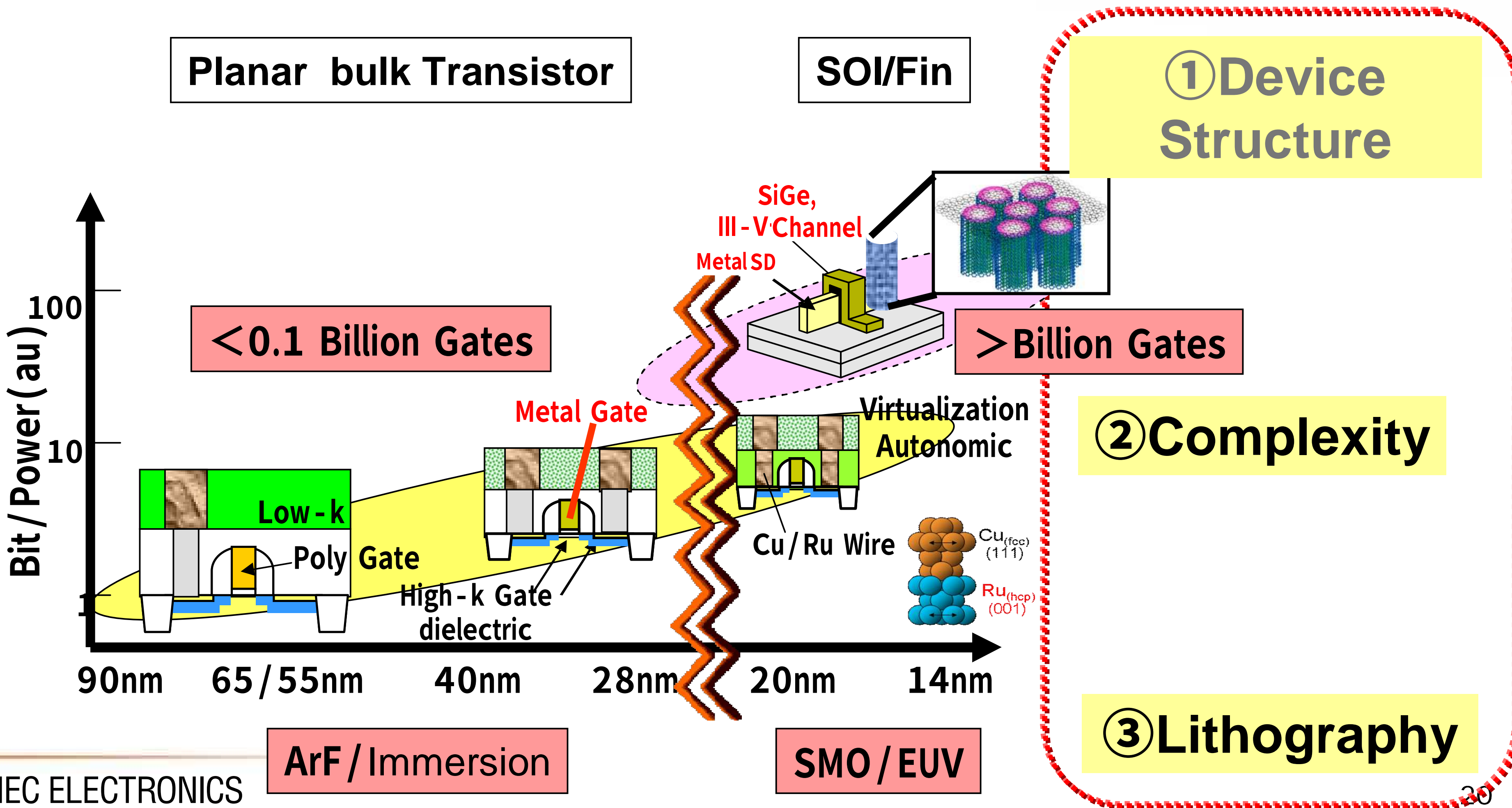
- Unification of RAM / ROM
- Low Voltage Operation
- Zero Stand-by Current
- Reduction of Process Steps



Paradigm Shift ?

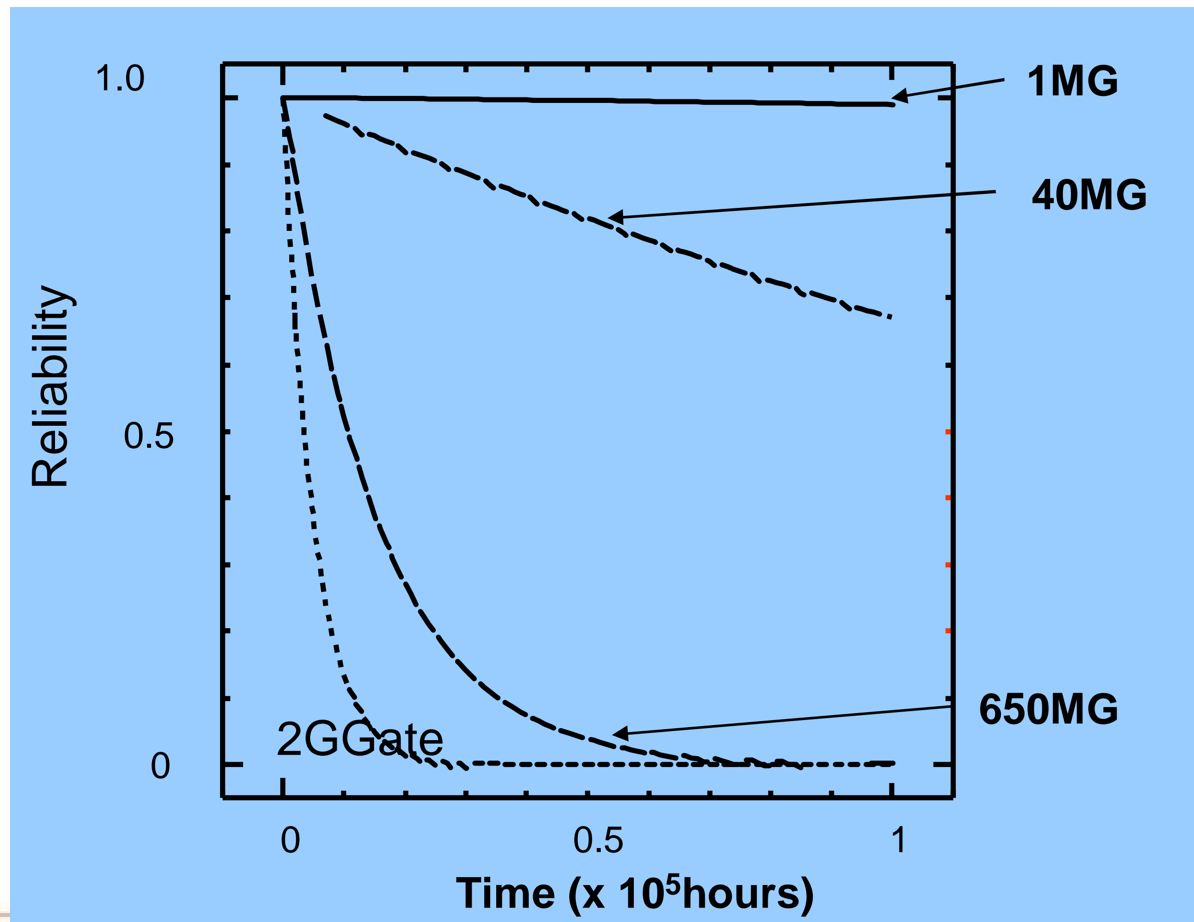
Emerging Challenges after 22/20nm

- Paradigm Shift in 22nm generation due to Physical Limits of Silicon
  Changes in Design, Device, Structure, Materials and Lithography



②Design Complexity: Reliability, Variability

Reliability of transistors decrease with scaling, and the reliability of LSI falls down with the increase in gate count
⇒ Dependable LSI design



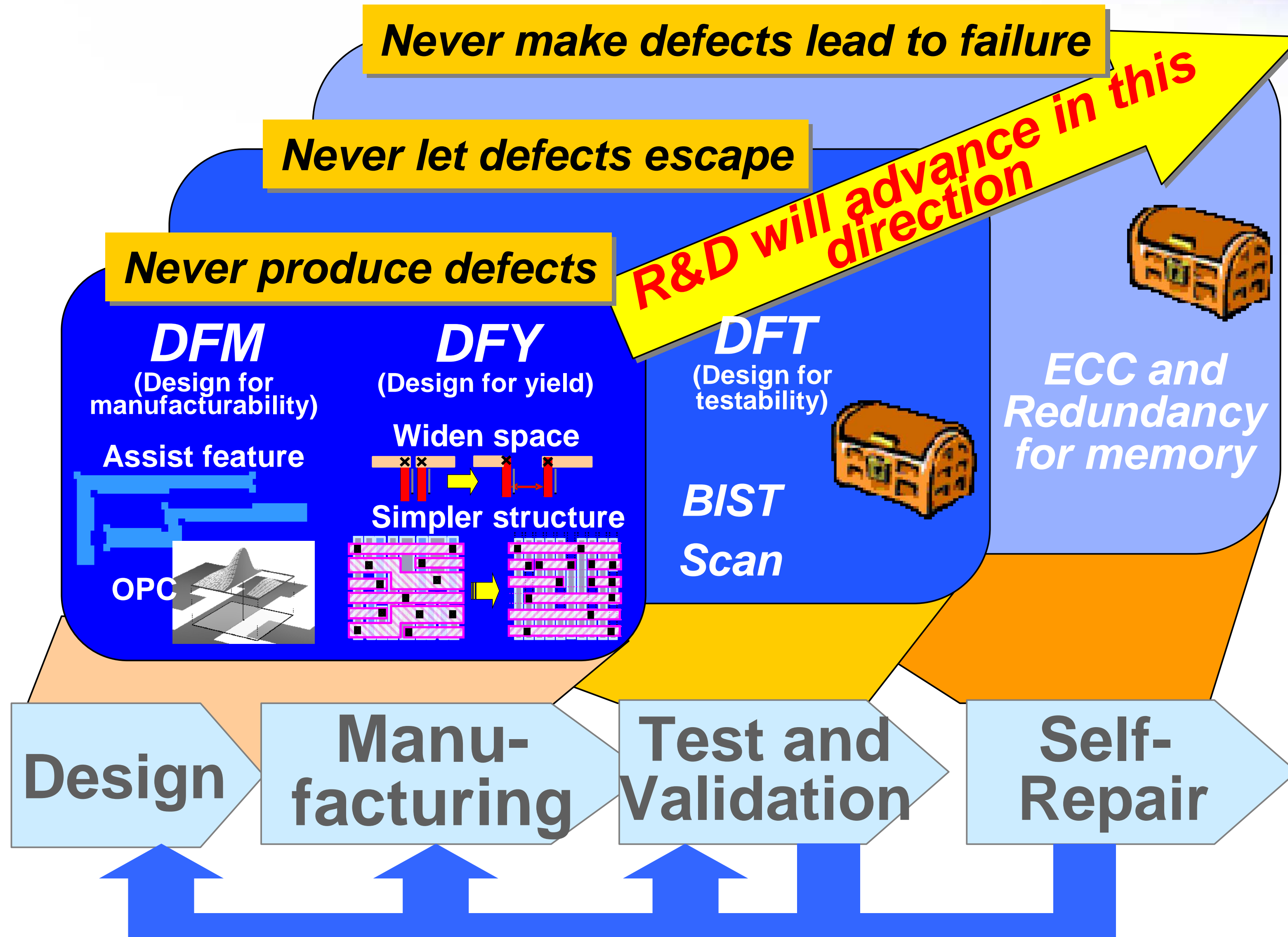
55nm：10MG

40nm：20MG

28nm：40MG

20nm：80MG

Design for Dependable LSI



Autonomous Reconfigurable Cell Array

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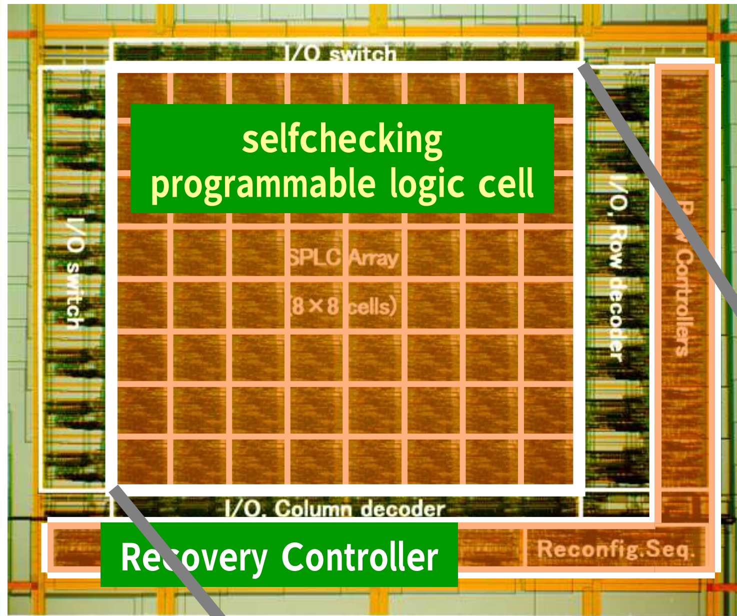
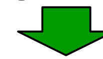
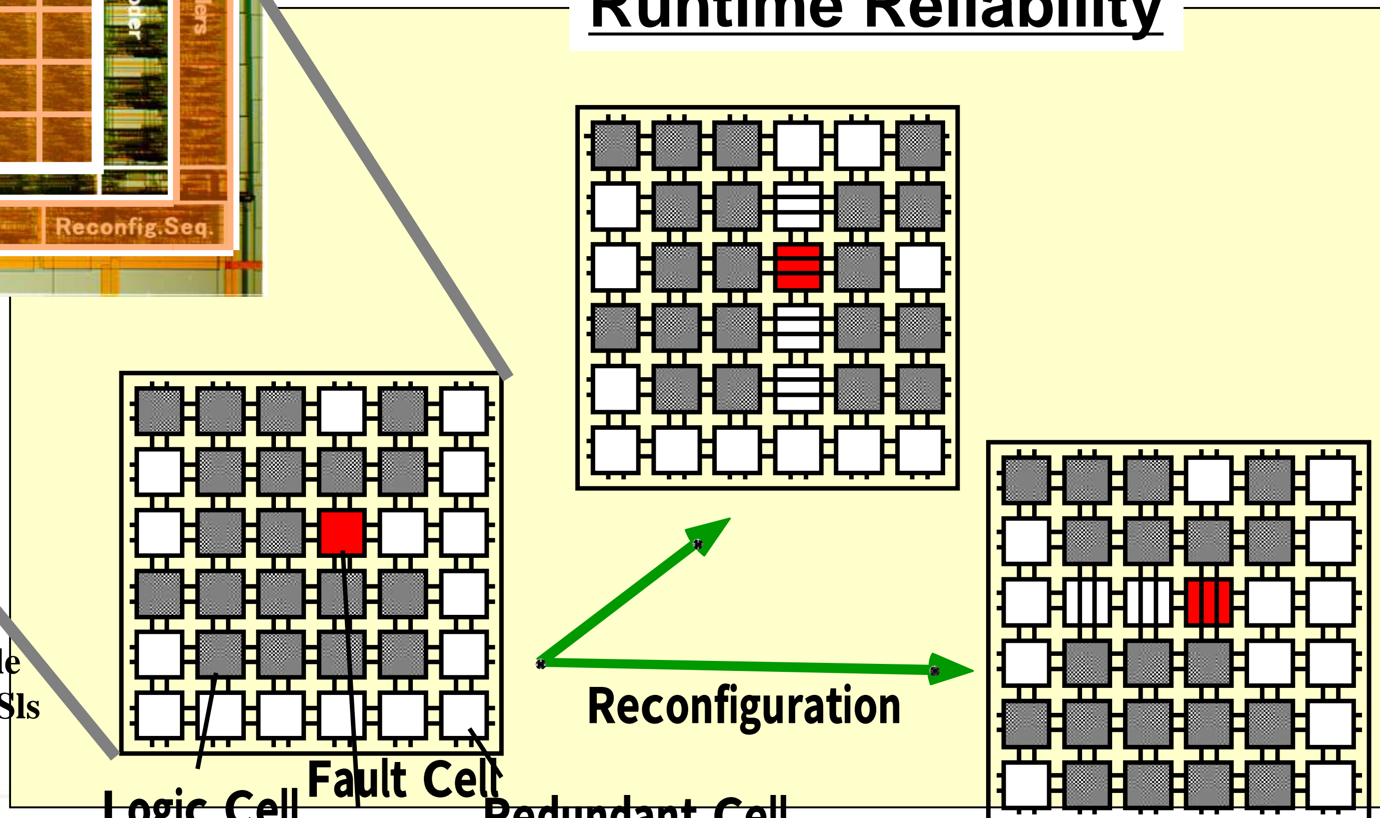


Self-checking programmable logic cell self-detects faults in real-time and automatically recovers while remaining on-line





An Autonomous Reconfigurable Cell Array for Fault-Tolerant LSIs (Shibayama, ISSCC97)

③Lithography (Cost Issue)

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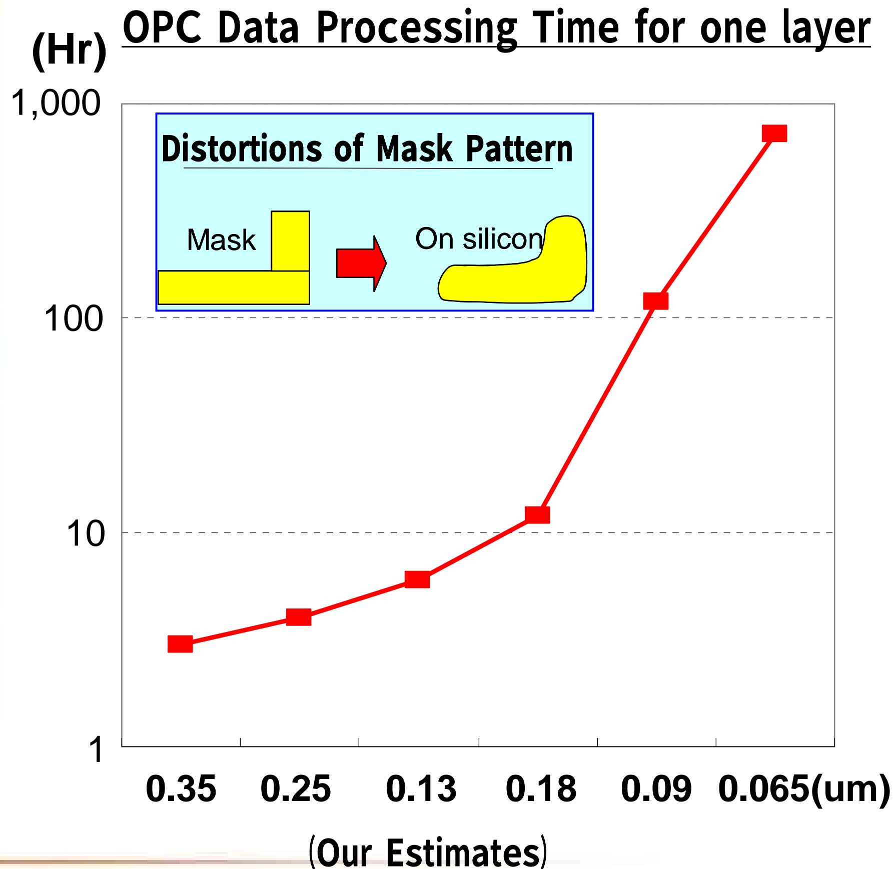
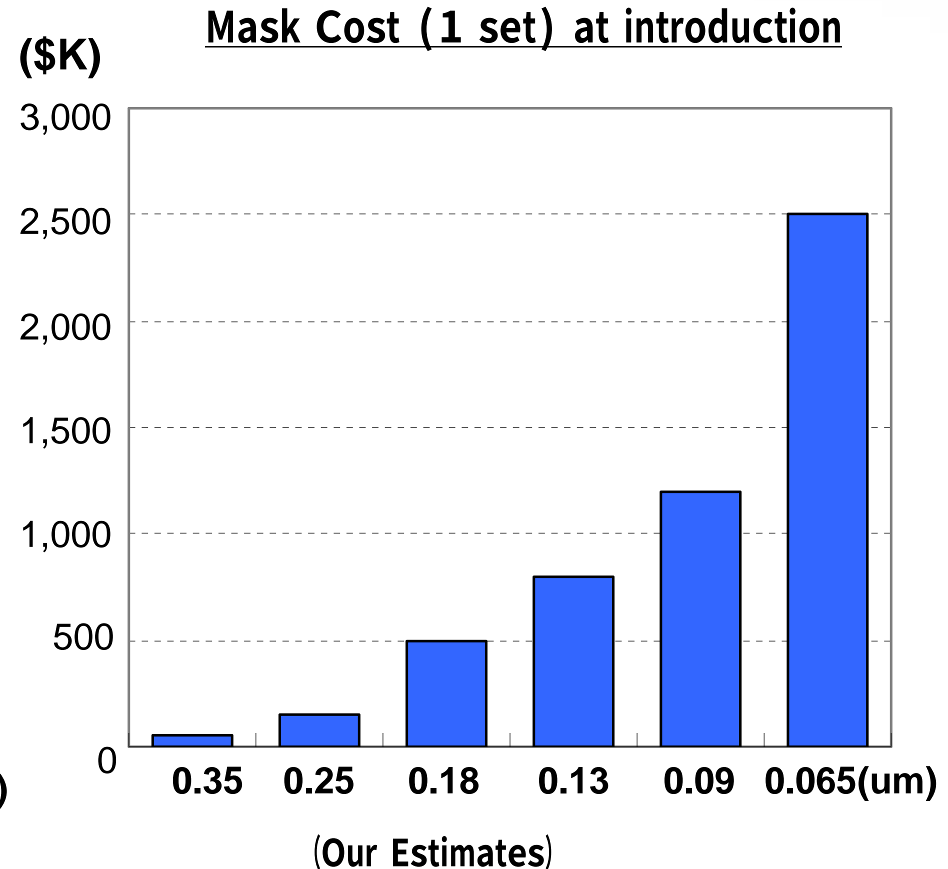
Scaling below exposure wavelengh requires OPC or other lithography techniques

⇒Cost problem (Mask cost)

(Exposure Wavelength：KrF=248nm, ArF=193nm)





EUVL　Accuracy of projection optics

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ArF Scanner（λ：193nm）
Lens surface：1 nm

EUVL Scanner（λ：13.5nm）
Mirror surface：0.1 nm

Equivalent to 0.7 mm roughness in the circle which surrounds Japanese archipelago

Equivalent to 1/5 of Subaru telescope Main Mirror's roughness

Regularity reduces Complexity and Lithography (cost) Problems

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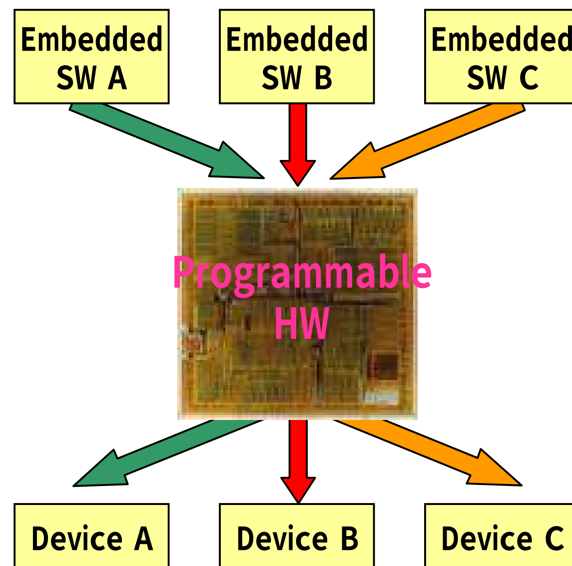
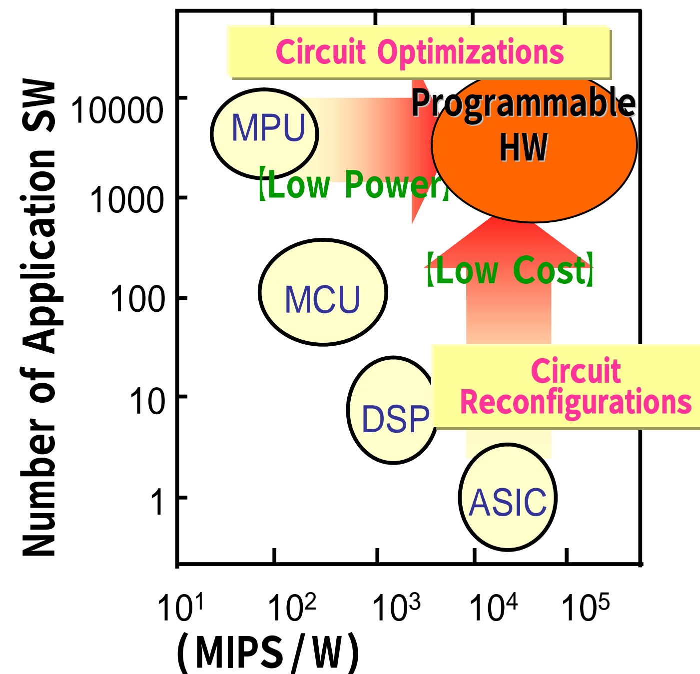
Dependable and Litho Friendly Circuits and Architectures

- Memory⇒ OK
- Logic⇒ Dynamically Reconfigurable HW
  (Static FPGAs suffer low Gate density)





DRP : Dynamically Reconfigurable Processor

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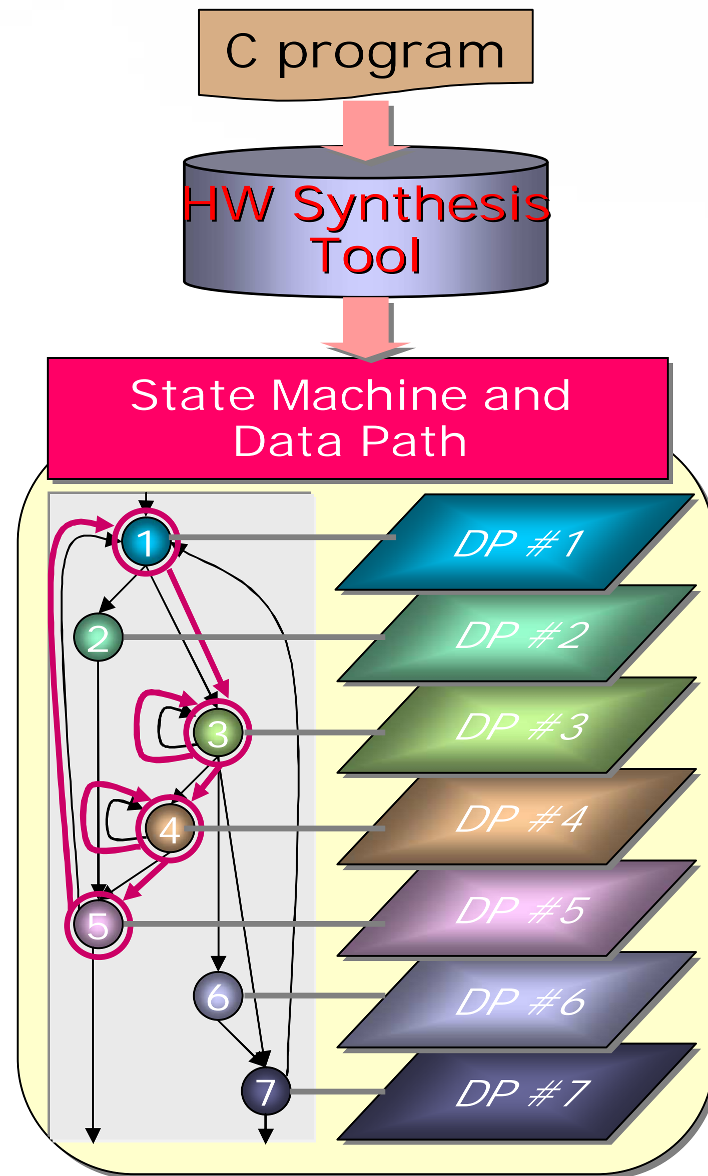
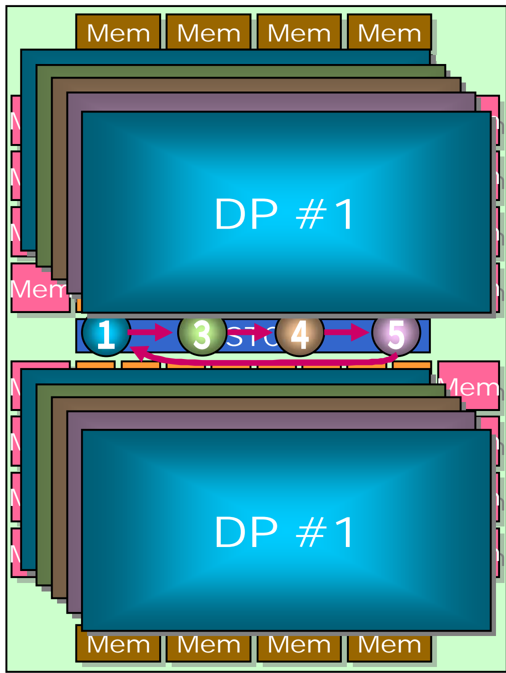
- Design and Manufacturing Cost is reduced by employing Regular Architecture
- Dynamic Reconfiguration of Programmable HW achieves (equivalent) Higher Gate Density



Runtime Reconfiguration

Mapping Target Runtime Model into Programmable HW



STP Engine（DRP）based SoC: XBridge

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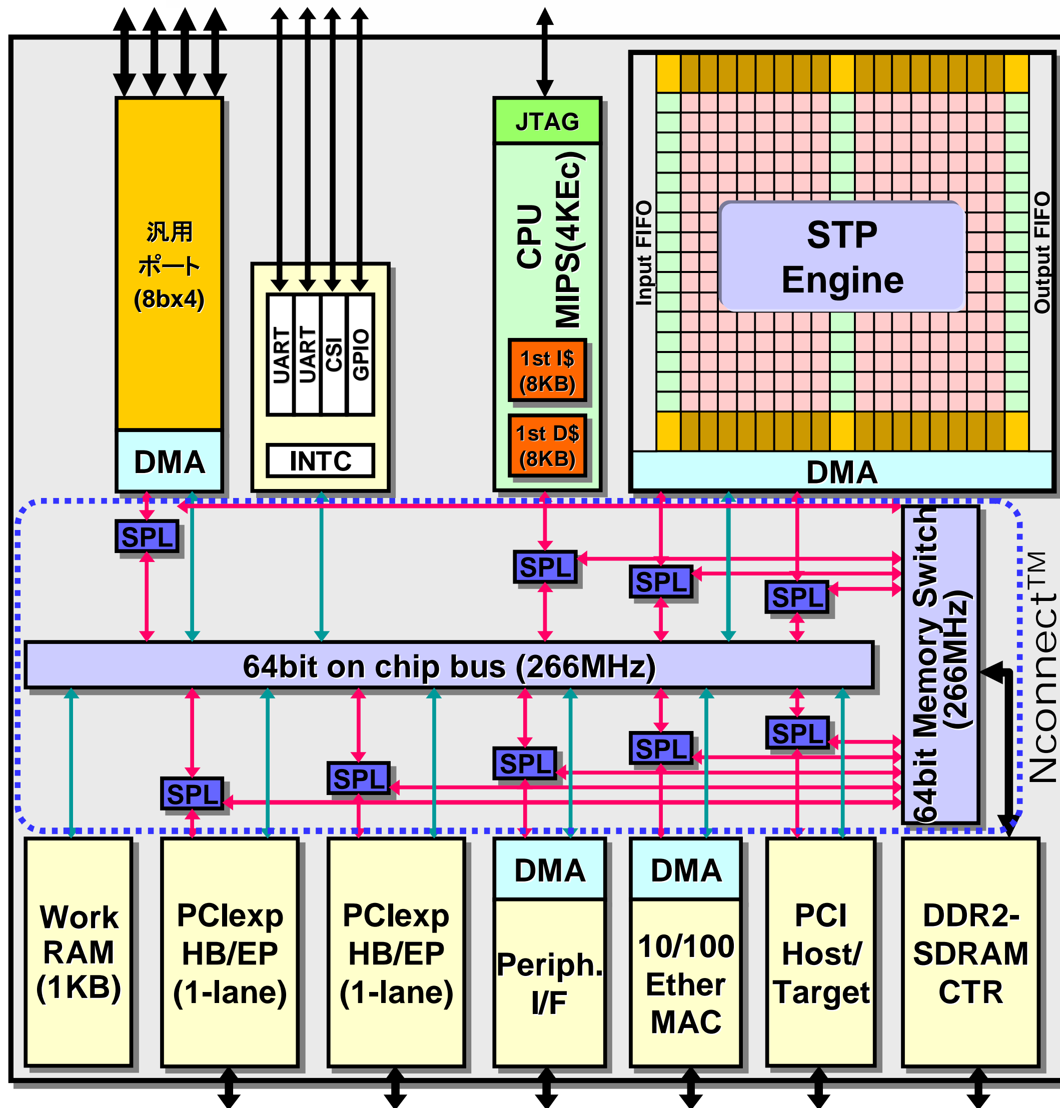

- 90nm Process
- 960pin 0.8mm pitch FCBGA (27mm□)
- Clock frequency:
  - System: 266MHz
  - STP Egine: 33-100MHz
- Power Consumption: 2W(Worst)

STP Engine

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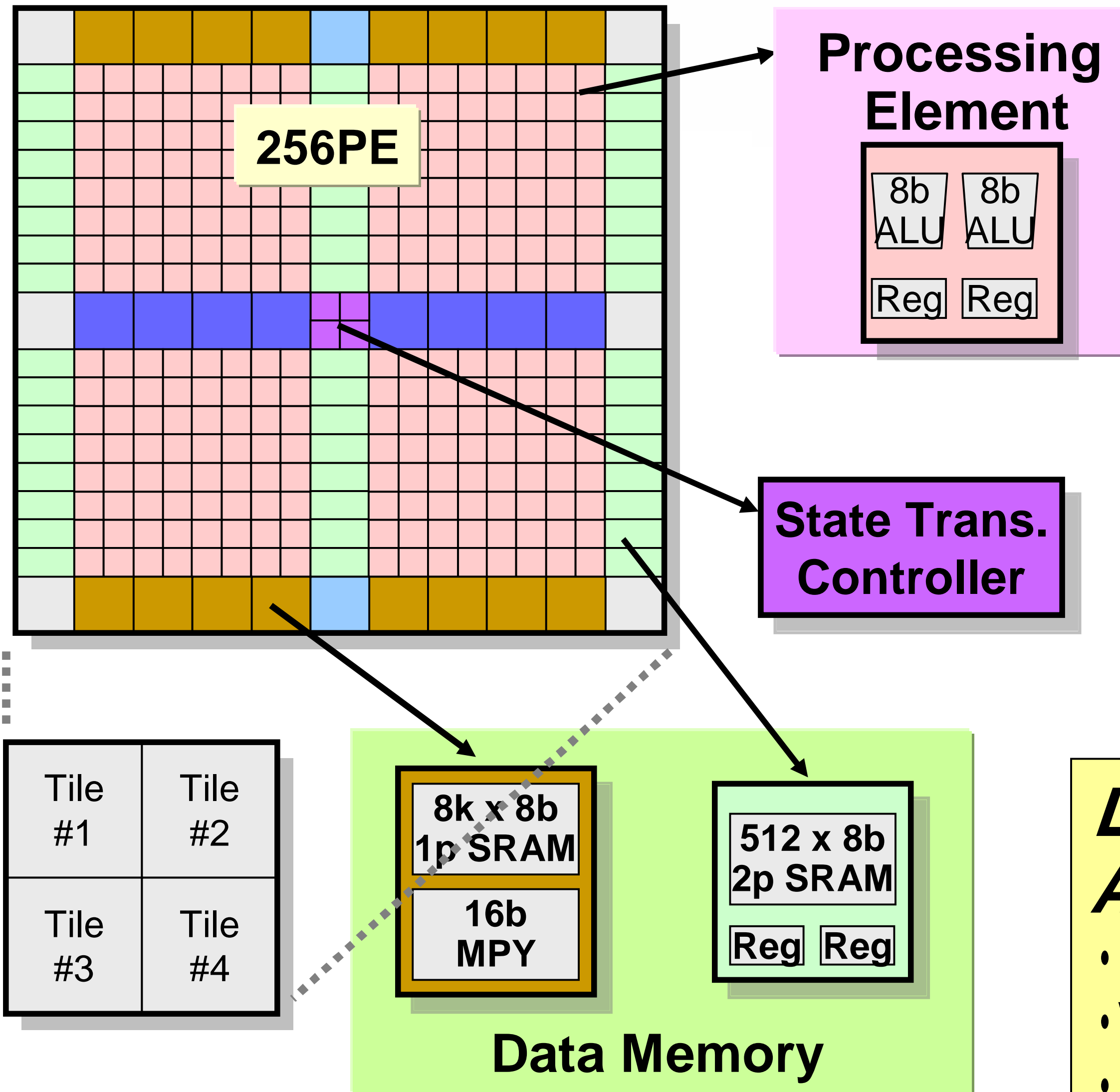

- **Processing Elements (4Tiles)**
  - **8b ALU: 512**
  - **16b MAC: 32**
- **Data Memory(4Tiles)**
  - **2 x R/W DataRAM**
    - **56 x 512B = 28KB**
  - **1 x R/W Data RAM**
    - **16 x 8KB = 128KB**

Low cost dependable Architecture

- **Litho friendly**
- **Virtual/Autonomic Capability**
- **Power Efficient**

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A Solution beyond 22/20nm

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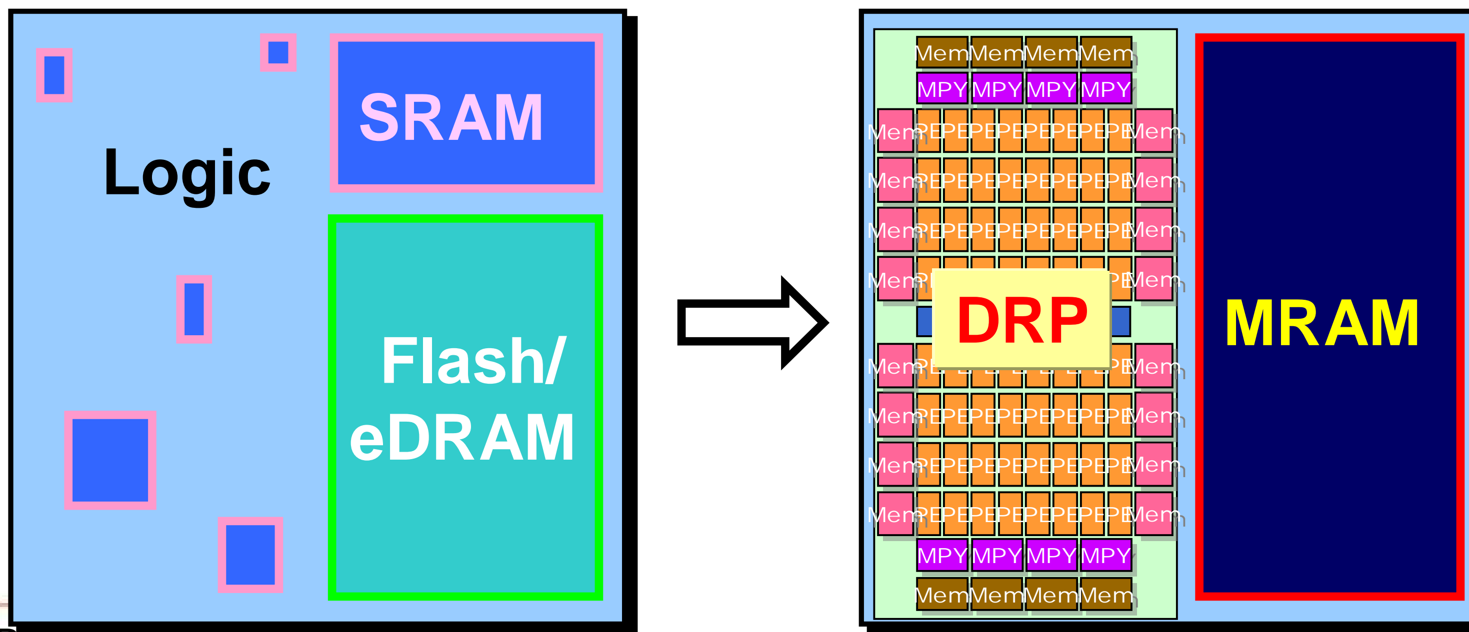
Technology Directions

①Device Structure⇒FIN、Ultra thin SOI、Air Gap
②Complexity (Reliability) Issue ⇒ Dependability
③Litho (Cost) Issue ⇒ Regularity

Logic ⇒ DRP: Programmable Hardware with Regularity
Memory ⇒ MRAM: Replace & Unify SRAM, eDRAM, Flash



Conclusions

- Embedded Memory
- Memory Integration Issues
  - FE/BE seperation
    - Process flow, Structure Issues
- Candidates for New Memory （MRAM)
- Challenges after 22/20nm
  - Reliability/Lithography(Cost) Issue
  - Regular Logic：DRP + Universal Memory

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