Scaling limits of MRAM

Han Guchang

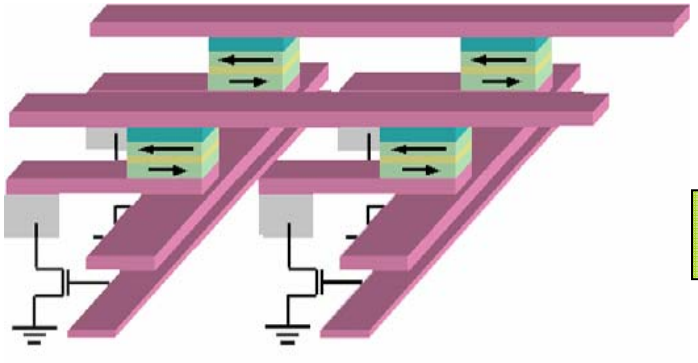
Data Storage Institute, A*STAR

Why MRAM

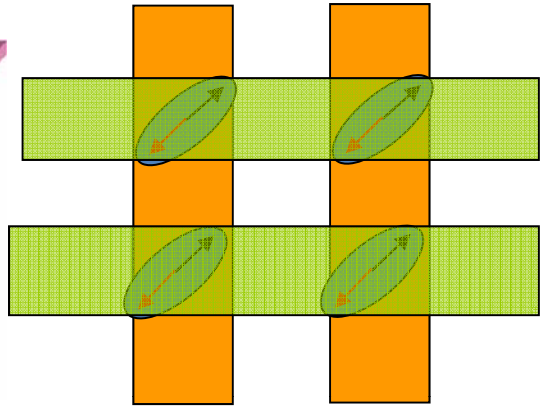
	SRAM	DRAM	FLASH	MRAM	CRAM
Nonvolatile	No	No	Yes	Yes	Yes
Read speed	Fast	M*	M	Fast	Fast
Write speed	Fast	M	Slow	Fast	Fast
Density	Low	High	High	High	High
Cost	High	Low	M	Low	Low
Power consumption	Low	high	Low	Low	Low
Endurance cycles	---	---	10^6	10^{14}	10^{12}

MRAM is a universal memory?

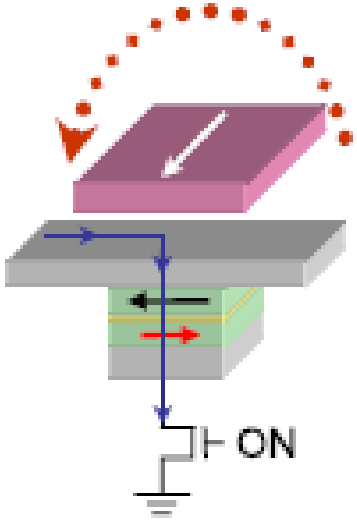
Various MRAM structures



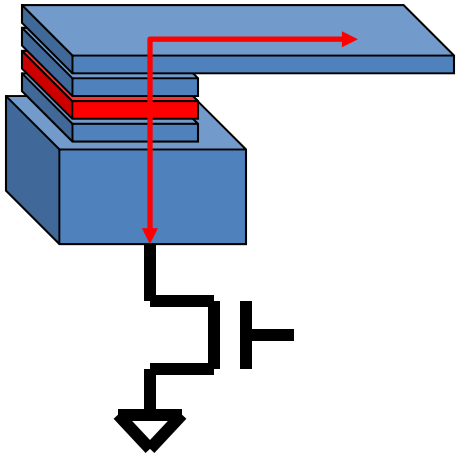
Conventional MRAM



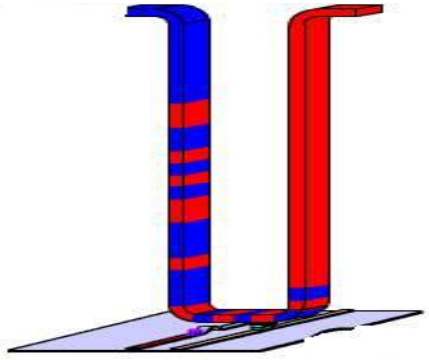
Toggle MRAM



TAS- MRAM

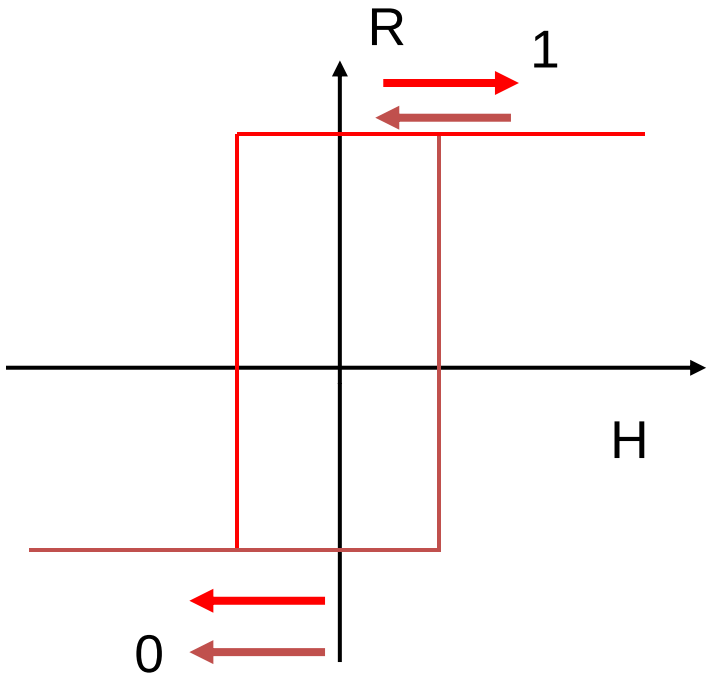


STT-MRAM (Our focus)

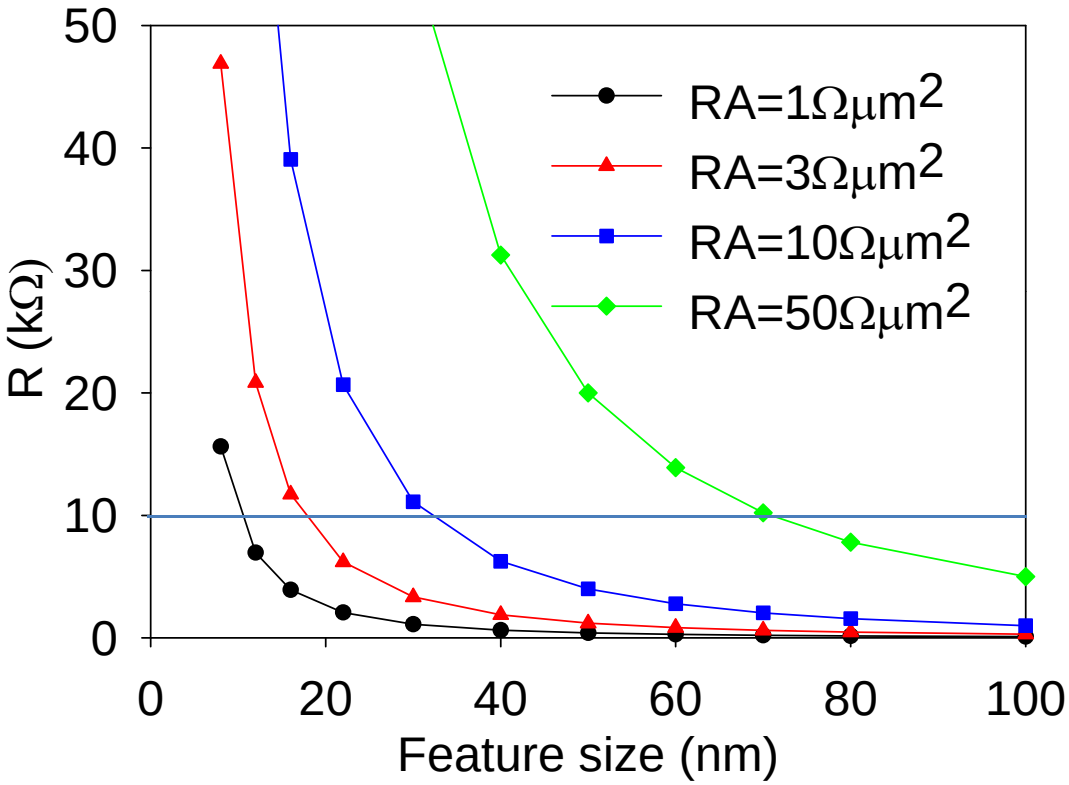


Racetrack memory

Scaling issues for reading



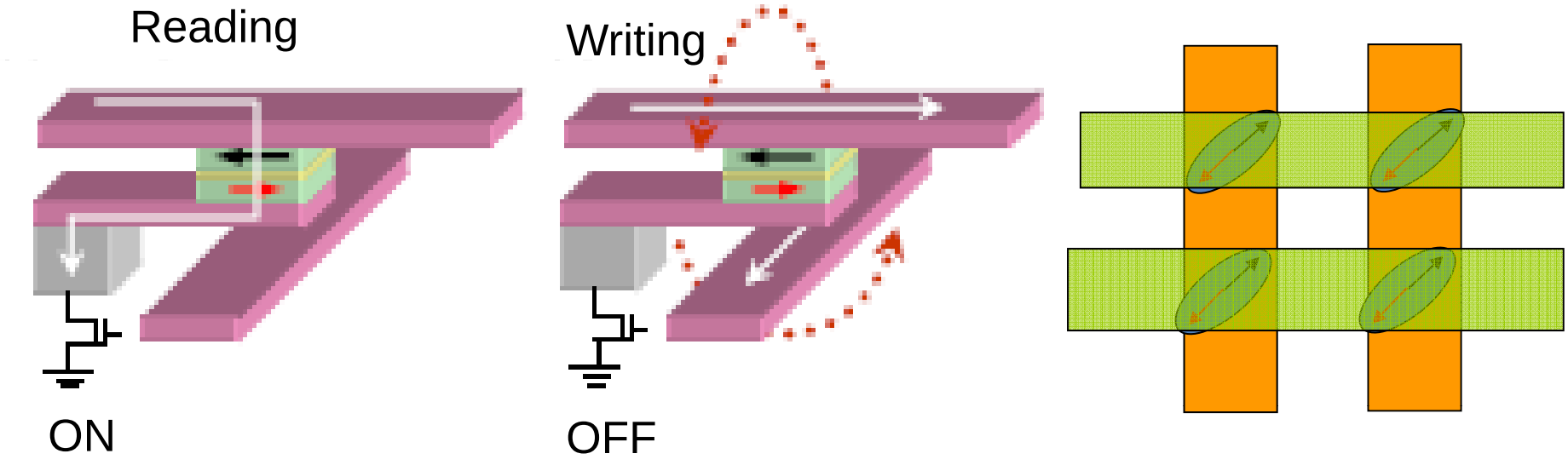
MR-H curve of a MTJ



Challenges

- Ultrathin barrier (~1nm for RA=3Ωμm2)
- R uniformity over wafer

Scaling issues for field writing



Conventional - MRAM

Toggle - MRAM

Issues for scaling

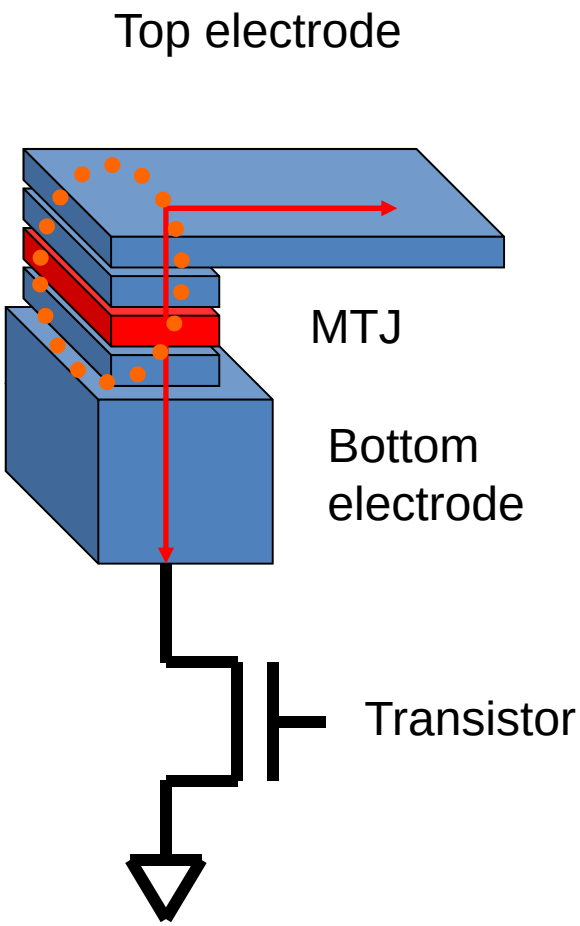
- High writing current, low density
- Large switching field distribution – sensitive to process
- Half selection issues- retention

Alternatives

Spin Torque Transfer (STT) –MRAM

Thermally Assisted Switching (TAS) -MRAM

Alternatives- STT-MRAM



•Advantages

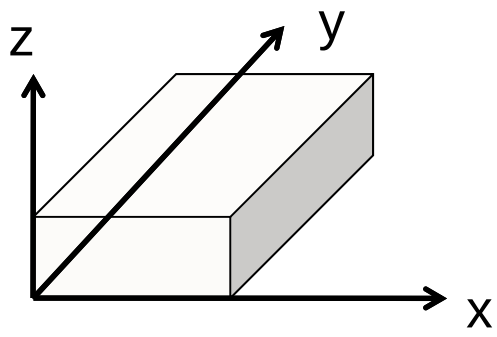
- •Simpler structure→ Lower cost
- •Smaller area→ Higher density
- •No half selection issue

What are the challenges?

STT-MRAM -Thermal stability and writeability

Low I_C for write endurance / CMOS size

$$I_c \propto \frac{M_s^2 V \alpha}{\eta} \sqrt{(N_{zz} - N_{xx}).(N_{zz} - N_{yy} + H_{ky}/M_s)}$$



Thermal stability $E_a = K_u V$

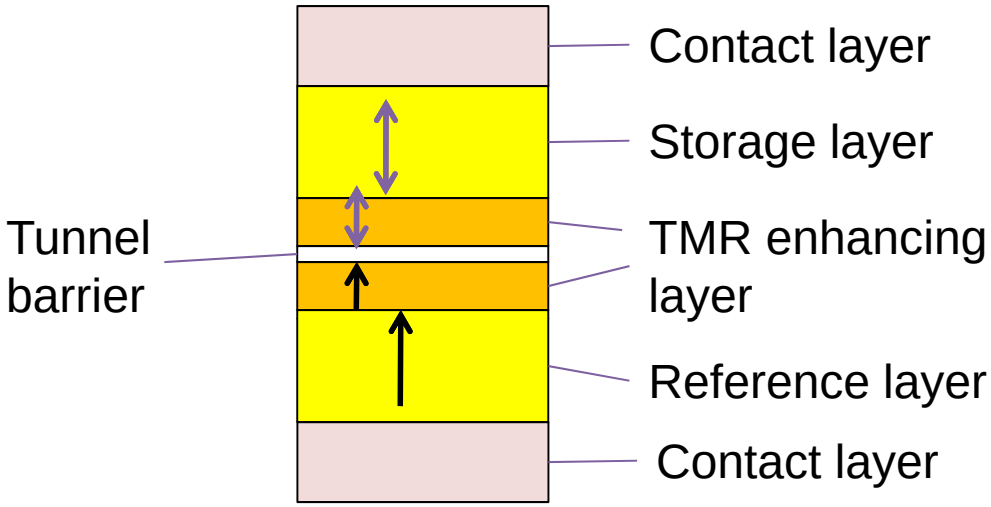
$$K_u V = \frac{1}{2} M_S^2 V (N_{xx} - N_{yy} + H_{ky}/M_s)$$

Where α=damping constant,η=STT efficiency
For in-plane anisotropy thin film, we have: $N_{zz} >> N_{xx}$, $N_{zz} >> N_{yy}$

$K_u V$: In-plane anisotropy, I_c: Out of plane anisotropy.

High aspect ratio is required to get high stability – low density

Perpendicular STT MRAM



$$I_c = \left(\frac{2e}{\hbar}\right)\left(\frac{2\alpha}{\eta}\right)\left(K_u V\right)$$

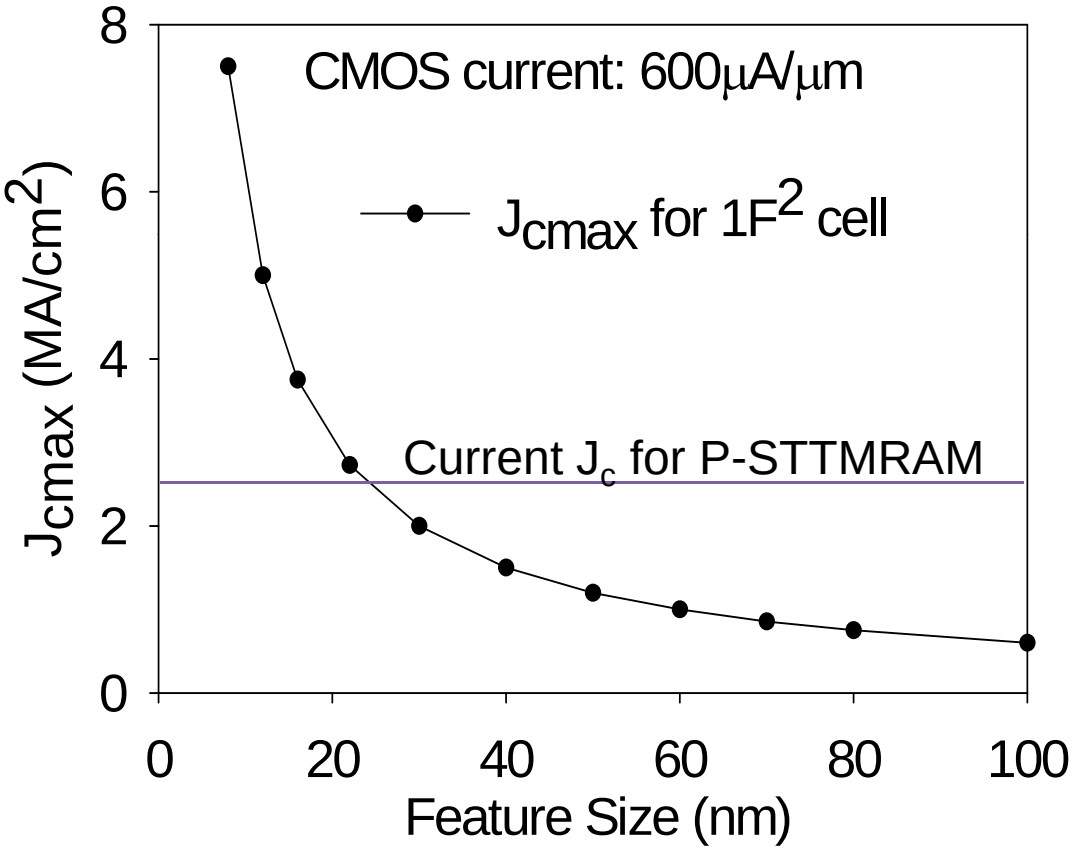
$$\frac{I_c}{E_a} = const \ .$$

Advantages

- Scalable
- Switching current is independent of shape
- High stability and high density
- Small cell to cell interaction

How far we can go? – Scaling limit

Current allowed by CMOS: I_T~600μA/μm
Writing current I_c should be smaller than I_T for 1T1MTJ



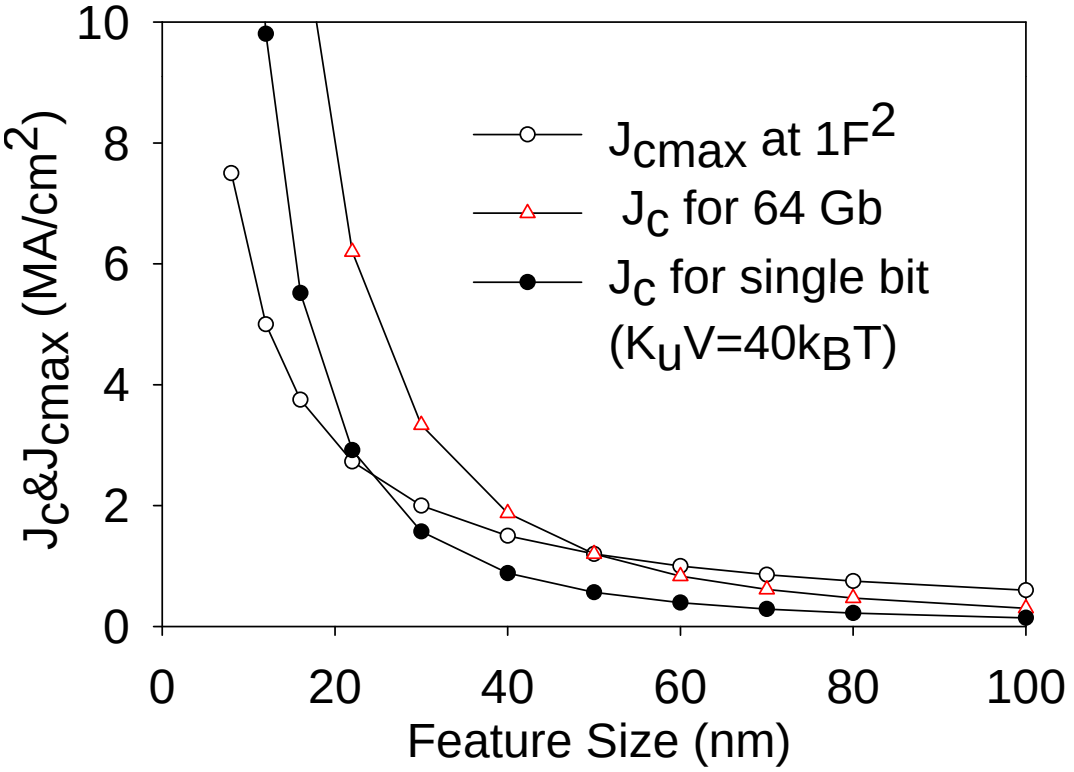
Will density be eventually limited by CMOS technology?

How far we can go? – Retention and writeability

For 64 Gb capacity, 10 year retention, $K_uV=85\ k_BT$

$$I_c = 2380 \times \frac{\alpha}{\eta}$$

For α ~0.01 and η~80%
I_c~30μA



Challenges

- I_c reduction without reducing K_uV


Thanks !!