Floating Body RAM (FBRAM) : Overview and Future Challenges

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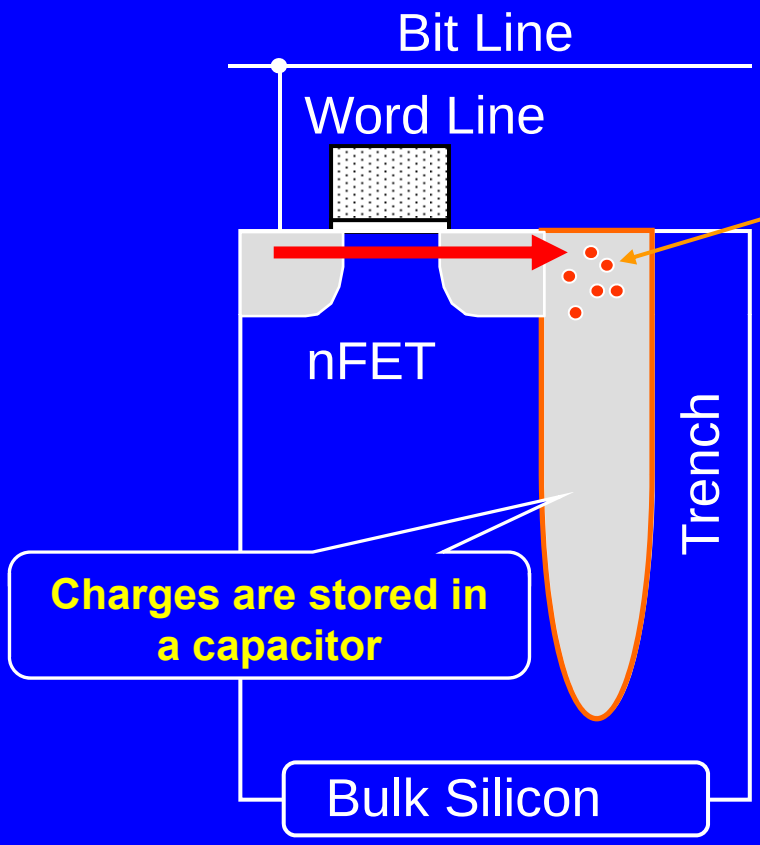
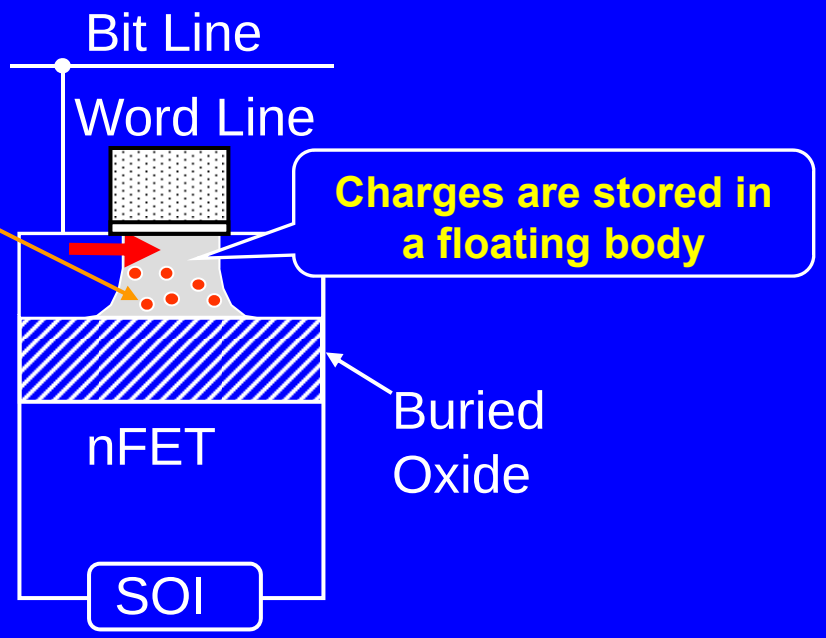
DRAM Cell vs FBC



1T-1C DRAM Cell

Charge



"1" : larger hole density (V_{th1})

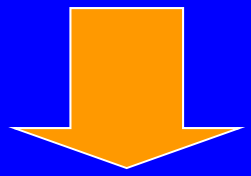
"0" : smaller hole density (V_{th0})

$V_{th1} < V_{th0}$

Floating Body Cell

Target of Floating Body RAM (FBRAM)

- **High performance RAM,**
  which can replace eSRAM.
- **Large Density RAM,**
  which can replace eDRAM.

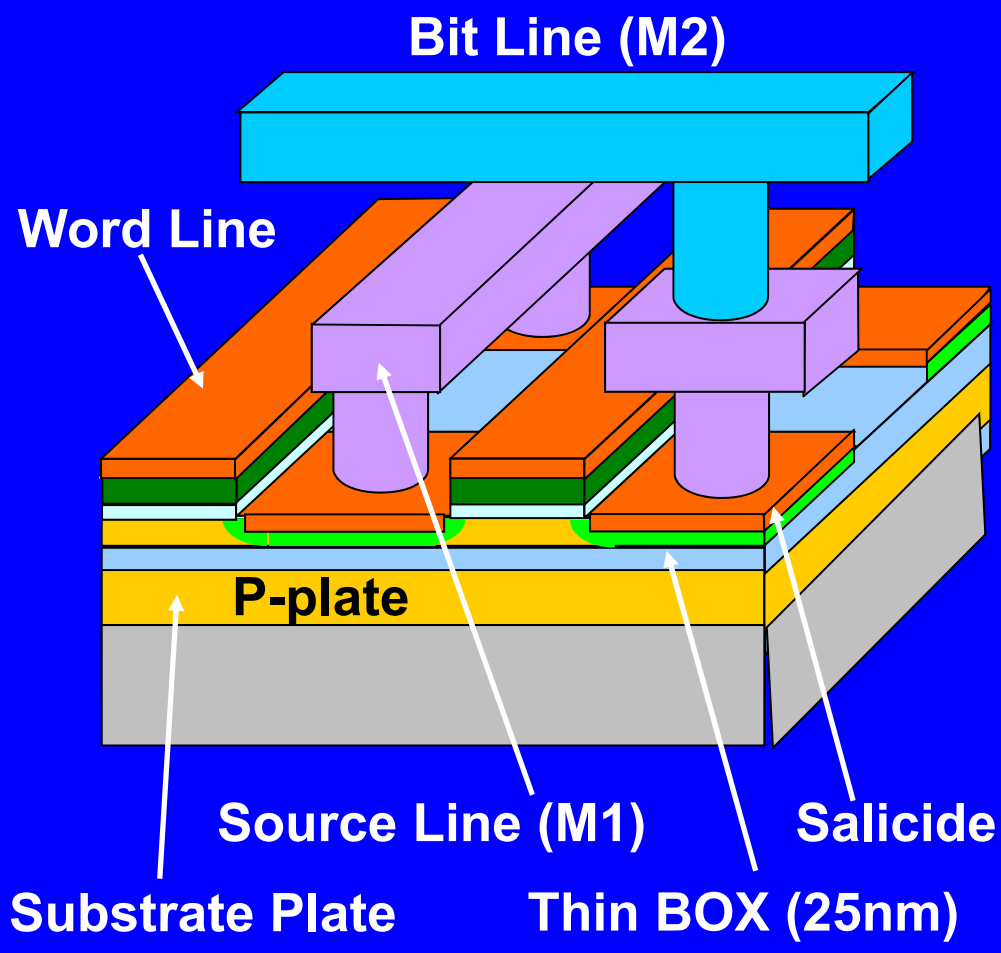


High performance/Large density RAM,
which can be used as an embedded memory
with Low Fabrication Cost.

Target of Floating Body RAM (FBRAM) ~Cont'd

	DRAM	eDRAM	FBRAM (1Cell/Bit)	FBRAM (2Cell/Bit)	SRAM
CellSize (F^2)	6 – 8	12 – 20	6	12	80
Process	CMOS + Capacitor	CMOS + Capacitor	CMOS		CMOS
tRC (ns)	20	5	20	3	1
Advantage	High Density	High Performance	Low Cost		High Performance
Retention @ median (s) @85C	>10	>1	>0.1		–
Issue to shrink	Capacitor Transistor	Capacitor Transistor	Transistor		Transistor
Scalability Limits	Storage Capacitance	Storage Capacitance	Hole Density		Signal Stability
Basis of memory	Charge Storage in Capacitor	Charge Storage in Capacitor	Charge Storage in Floaing Body		F-F

Overview of FBRAM development



FBRAM Technologies

- Cell Concept (ISSCC2002)
- Substrate Plate Cell (VL2004)
- FD Operation (IEDM2004)
- Salicide for Array Device (IEDM2004)
- 128Mb FBRAM (ISSCC2005)
  @ 90nm Tech.
- Well Design Optimized for Array & Supprot Device (IEDM2005)
- Cu Wiring used for SL and BL (IEDM2005)
- Scalability Estimation (IEDM2006)
- Single Cell Operation (IEDM2007)
- Autonomous Refresh (IEDM2008)

Issue for Scaling

- **Large Signal**
  - ✓ **Keep ΔVth ~ 0.40V**
- **Long Retention Time**
  - ✓ **Suppress Emax ~0.70MV/cm**
- **Array Functionality**
  - ✓ **Keep Signal-to-Noise Ratio (SNR)**

$$SNR = \Delta Vth / \sigma Vth > 18$$

Scalability of Partially-Depleted and Fully-Depleted FBC

$\Delta Vth \sim C_D / C_{ox} \times \Delta V_{Body}$

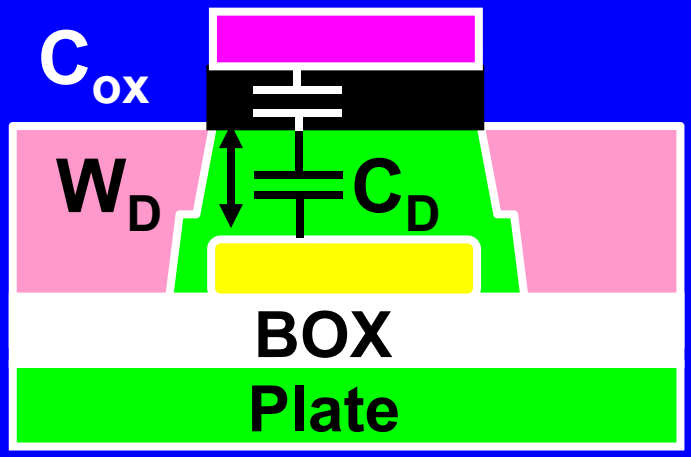
To keep ΔVth, C_D should be increased !

PD:

W_D reduction by high N_A

⇒ Degrade

V_T fluctuation, junction leakage

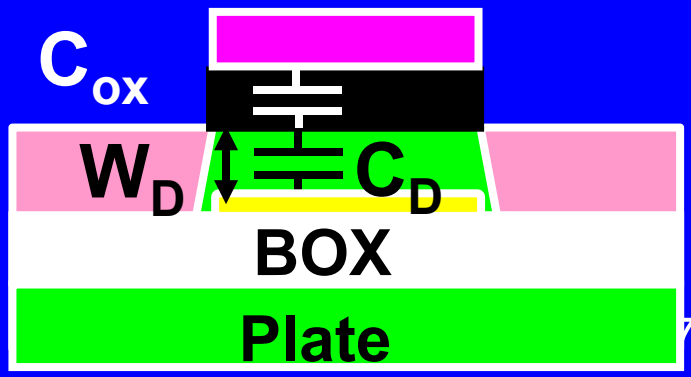


FD on thin BOX:

W_D reduction by Tsi reduction

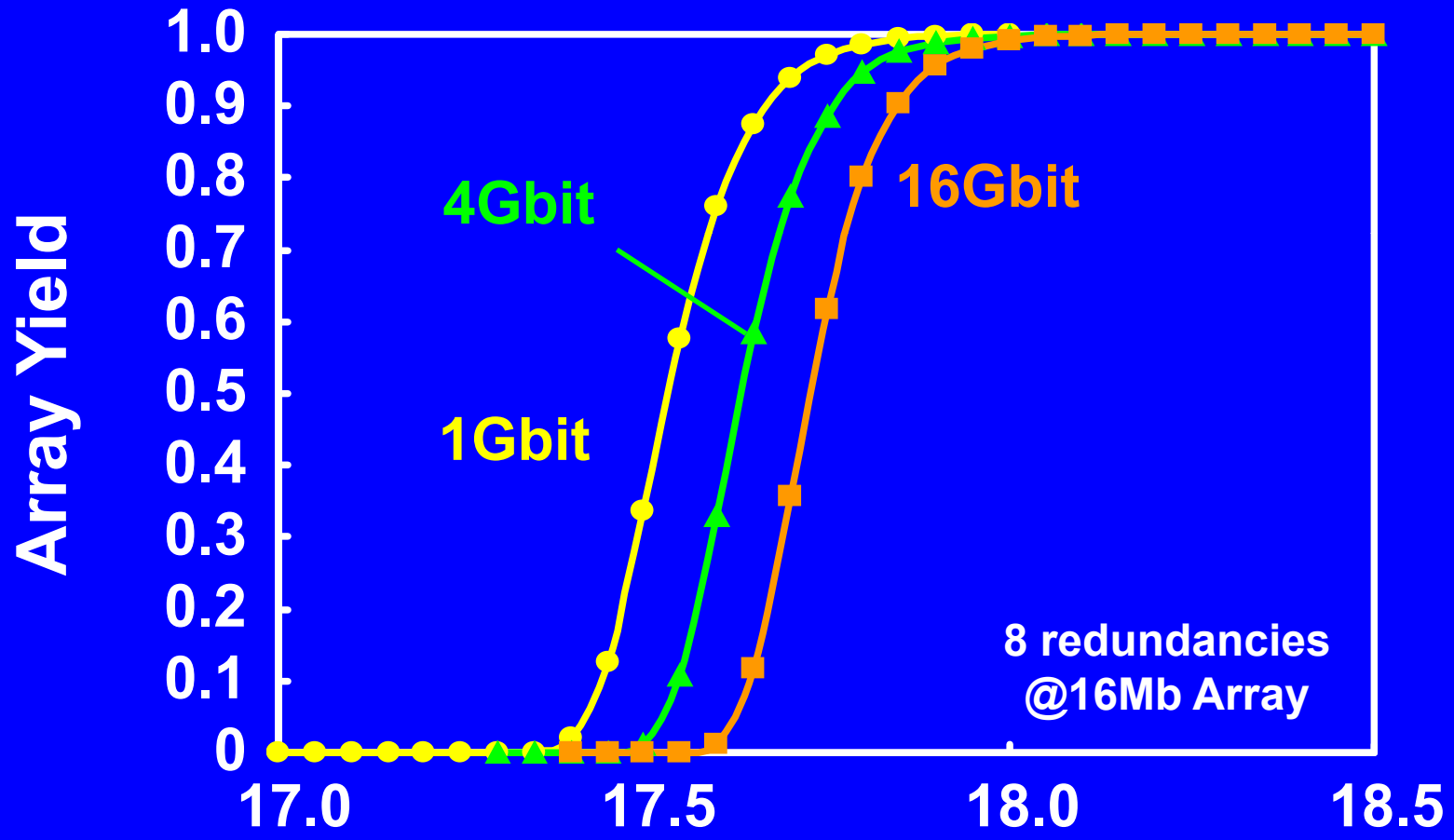
⇒ Does Not Degrade

V_T fluctuation, junction leakage

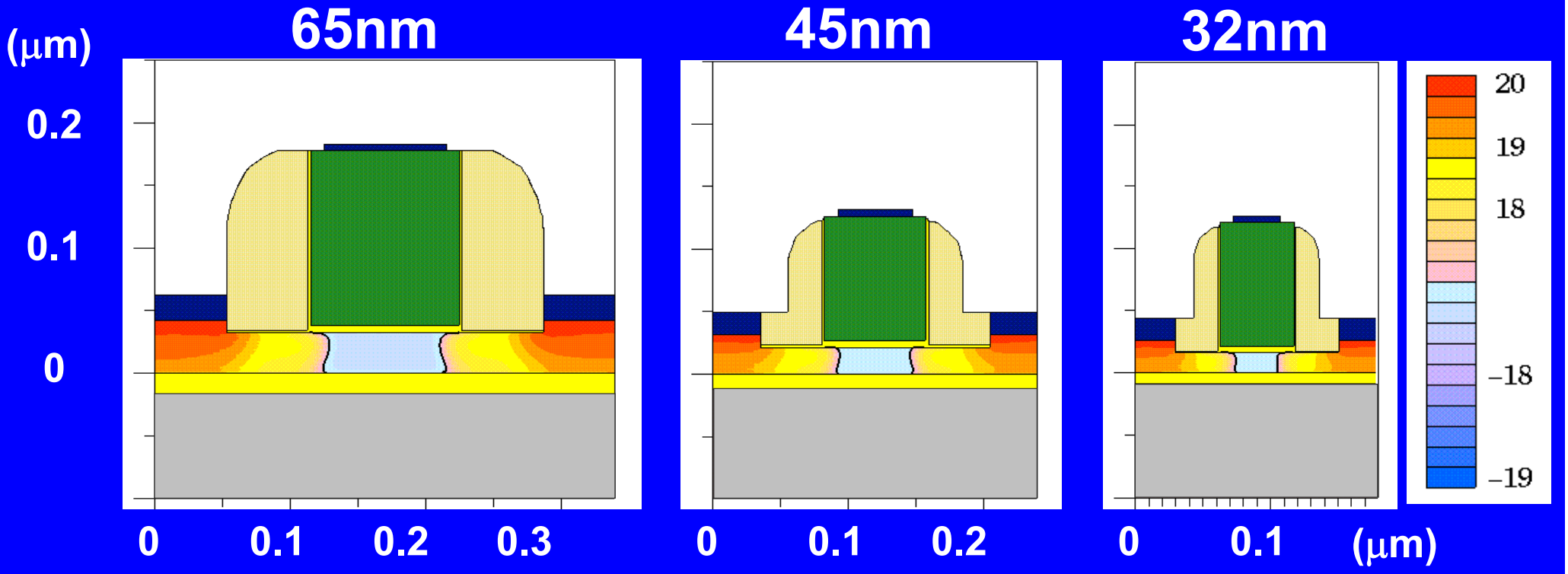


Memory Array Yield vs SNR

$SNR = \Delta V_{th}/\sigma_{Vth} = \Delta I_{cell}/\sigma_{Icell} = const. > 18$

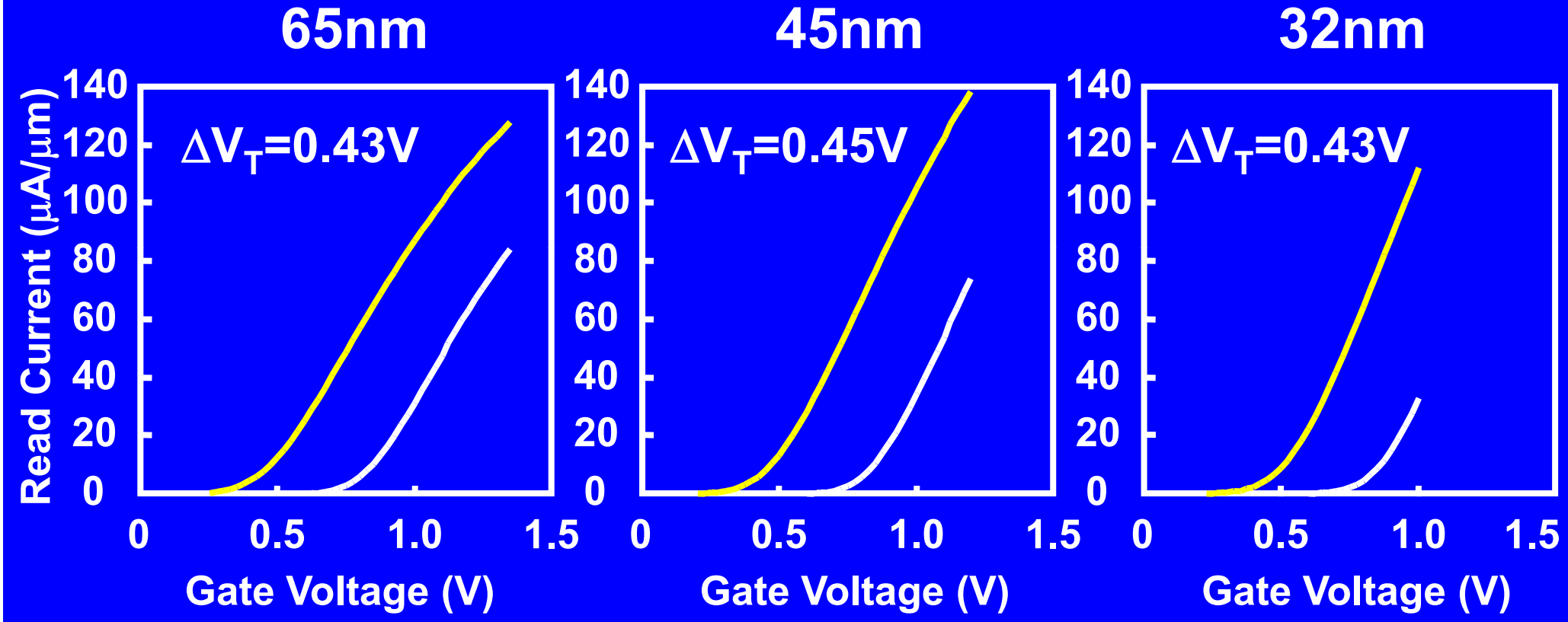


Structure of Scaled FD-FBC



65nm	45nm	32nm
Tsi=32nm	Tsi=21nm	Tsi=16nm
Tbox=17nm	Tbox=12.5nm	Tbox=9nm
Tox=5.6nm	Tox=5.2nm	Tox=4.8nm
Lg=110nm	Lg=75nm	Lg=55nm
Cell size=0.068μm^2	Cell size=0.0336μm^2	Cell size=0.02035μm^2

Id-Vg and Emax of Scaled FD-FBC

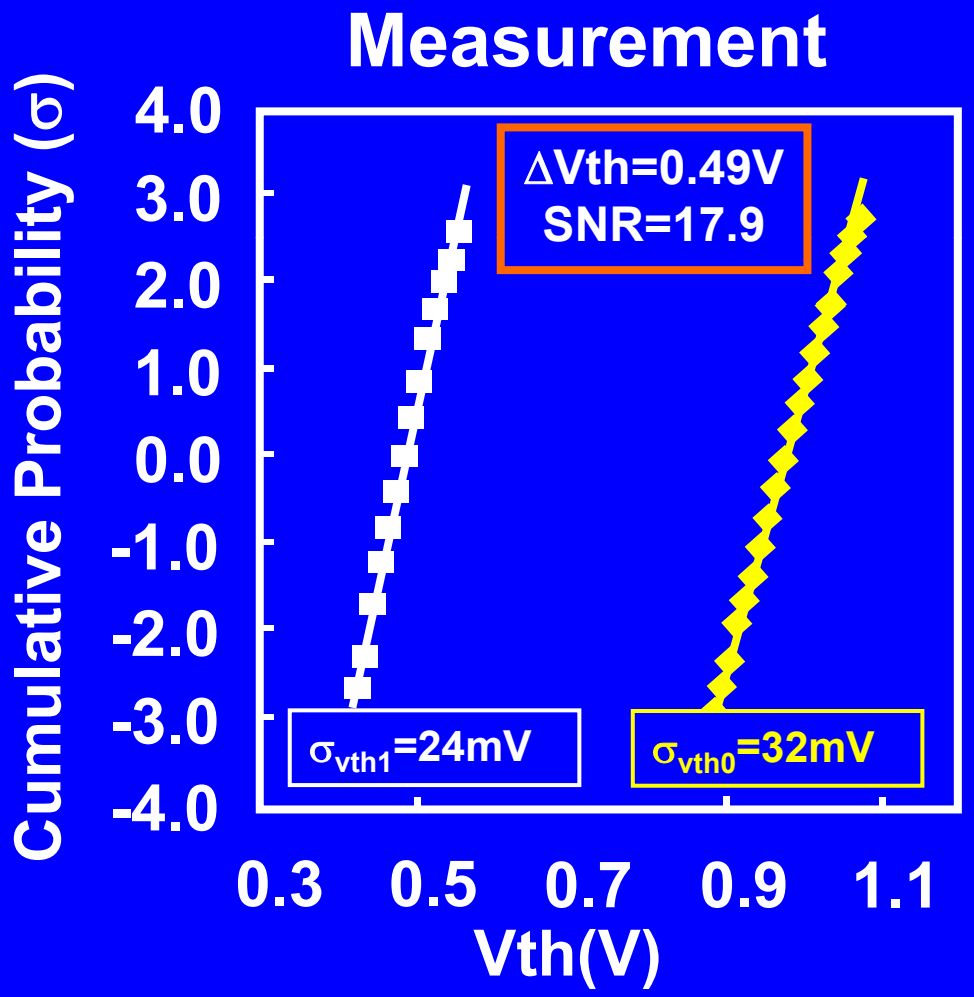


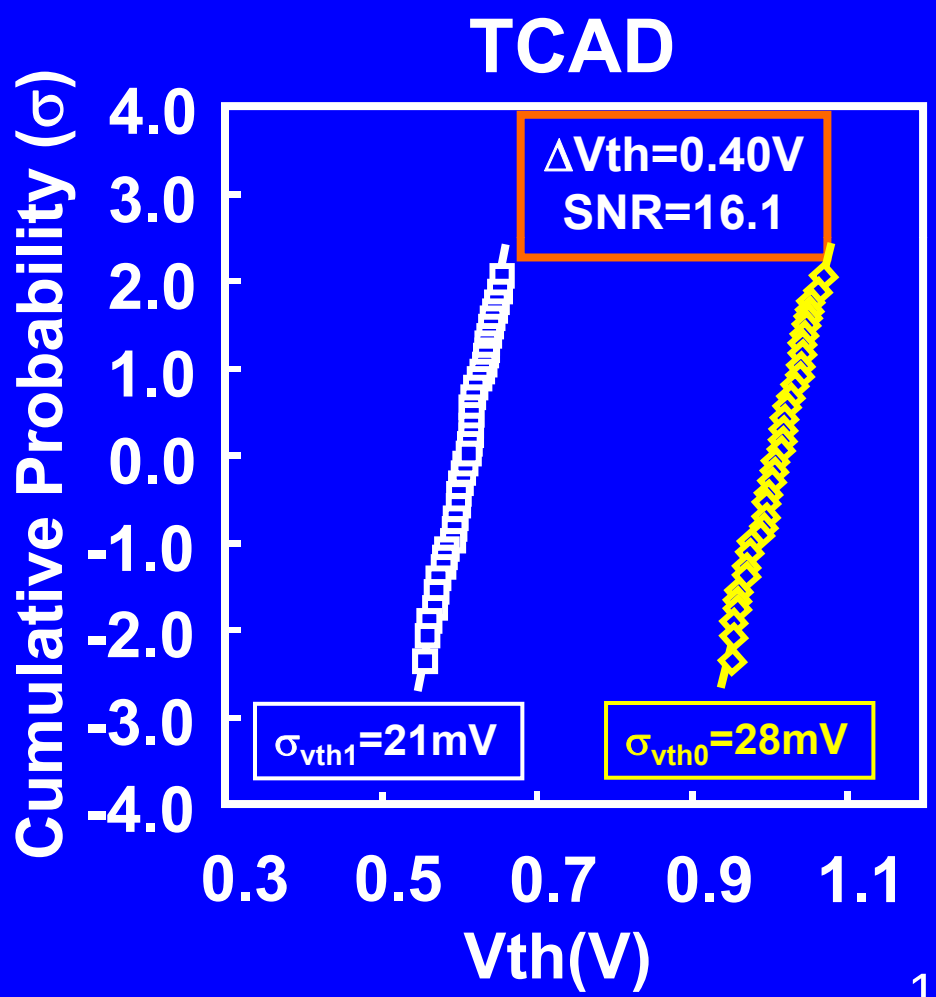
Emax of 0-cell =0.70MV/cm

Emax of 0-cell =0.70MV/cm

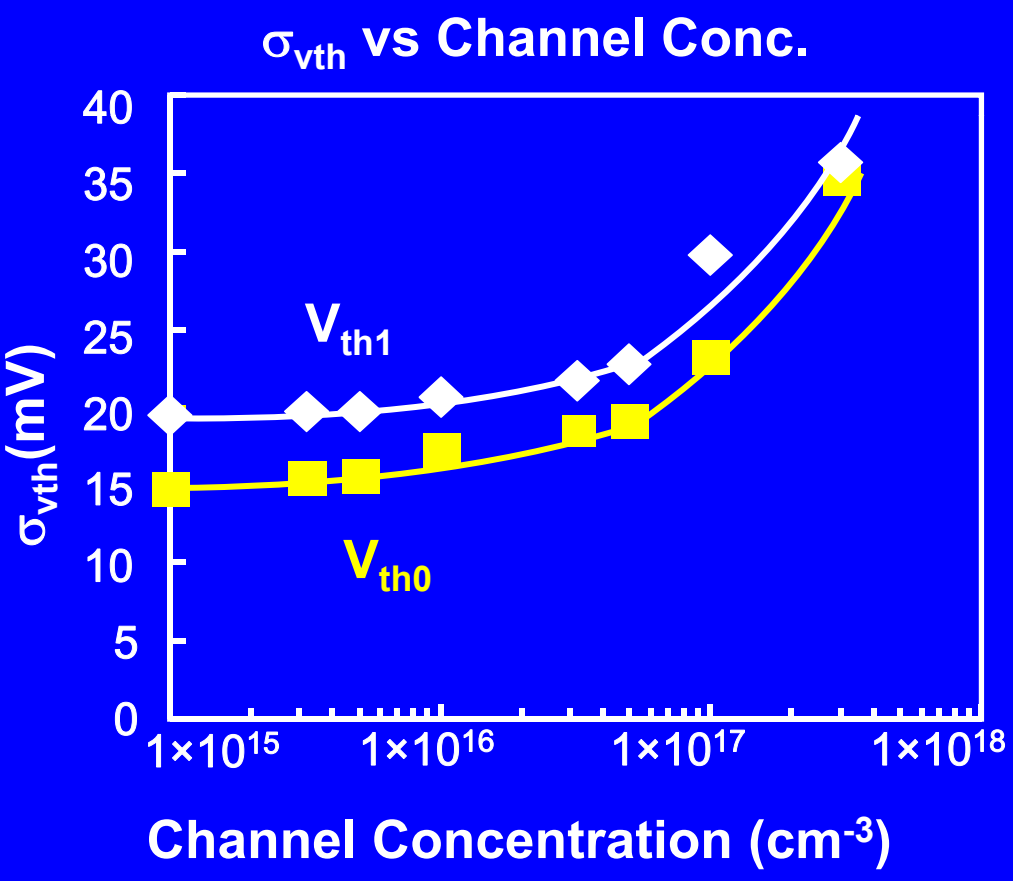
Emax of 0-cell =0.74MV/cm

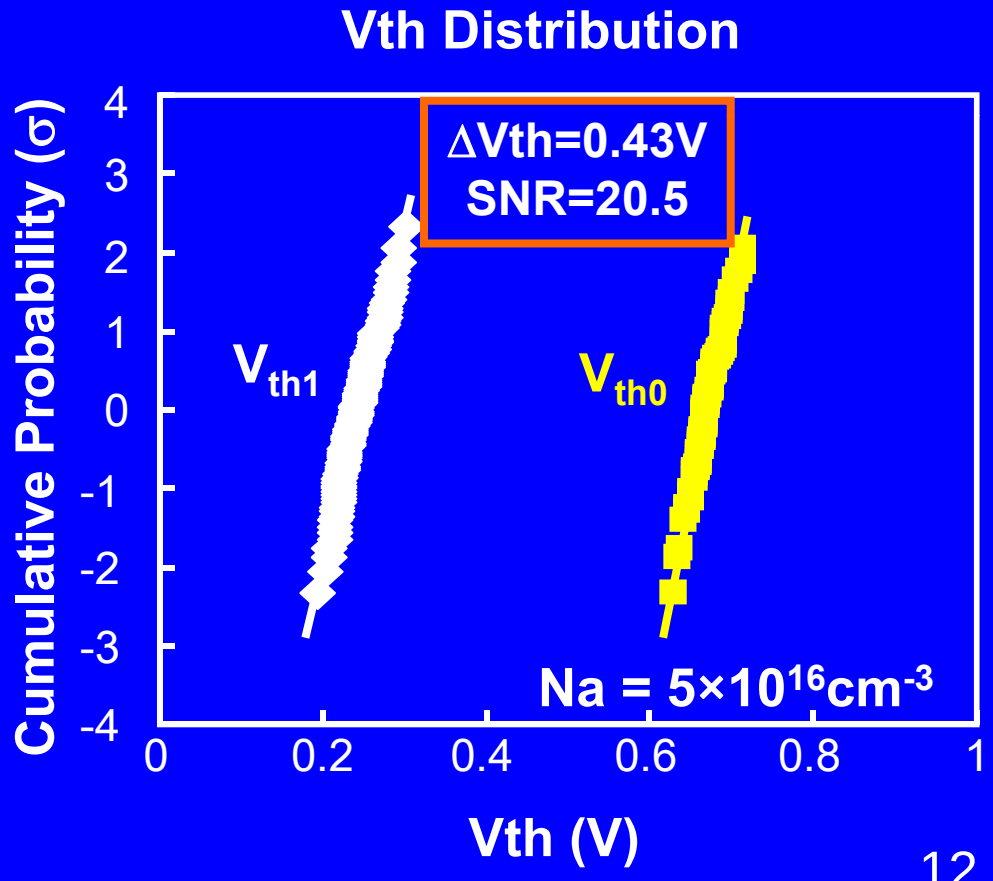
Vth Distribution & SNR @ 90nm Generation





TCAD Estimation of Vth Distribution & SNR @ 32nm Generation





Parameters of Scaled FD-FBC

	Generation	90nm	65nm	45nm	32nm
Structure	Cell Size (μm^2)	0.137	0.068	0.034	0.020
	Tsi (nm)	42	32	21	16
	Body Conc (cm^{-3})	3.E+17	2.E+17	1.E+17	5.E+16
	Tbox (nm)	25	17	12.5	9
	Lg (nm)	150	110	75	55
	Tox (nm)	6.0	5.6	5.2	4.8
Bias	Vwlh (V)	1.5	1.35	1.2	1.0
	Vwll (V)	−2.3	−2.0	−1.7	−1.45
	Vblh (V)	2.2	1.9	1.7	1.5
	Vbll (V)	−1.5	−1.2	−0.9	−0.7
	Vpl (V)	−3.0	−2.7	−2.4	−2.1
Results	Vth1 (V)	0.31	0.24	0.21	0.24
	Vth0 (V)	0.72	0.66	0.67	0.67
	ΔVth (V)	0.41	0.43	0.45	0.43
	Emax (MV/cm)	0.72	0.70	0.70	0.74
	SNR	18.3	17.9	17.9	20.5

Summary

FBRAM can be a candidate of future high-performance /large-density embedded memories with low fabrication cost.

FD-FBC is scalable down to 32nm node keeping signal margin (threshold voltage difference), retention time, and signal noise ratio (SNR) constant.