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MRAM : Materials and Devices

Current-induced Domain Wall Motion High-speed MRAM

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Outline

Introduction

- Positioning and direction of MRAM
- High speed MRAM cell

Domain wall motion cell for high speed MRAM

- Device structure and materials
- Writing properties and memory operation

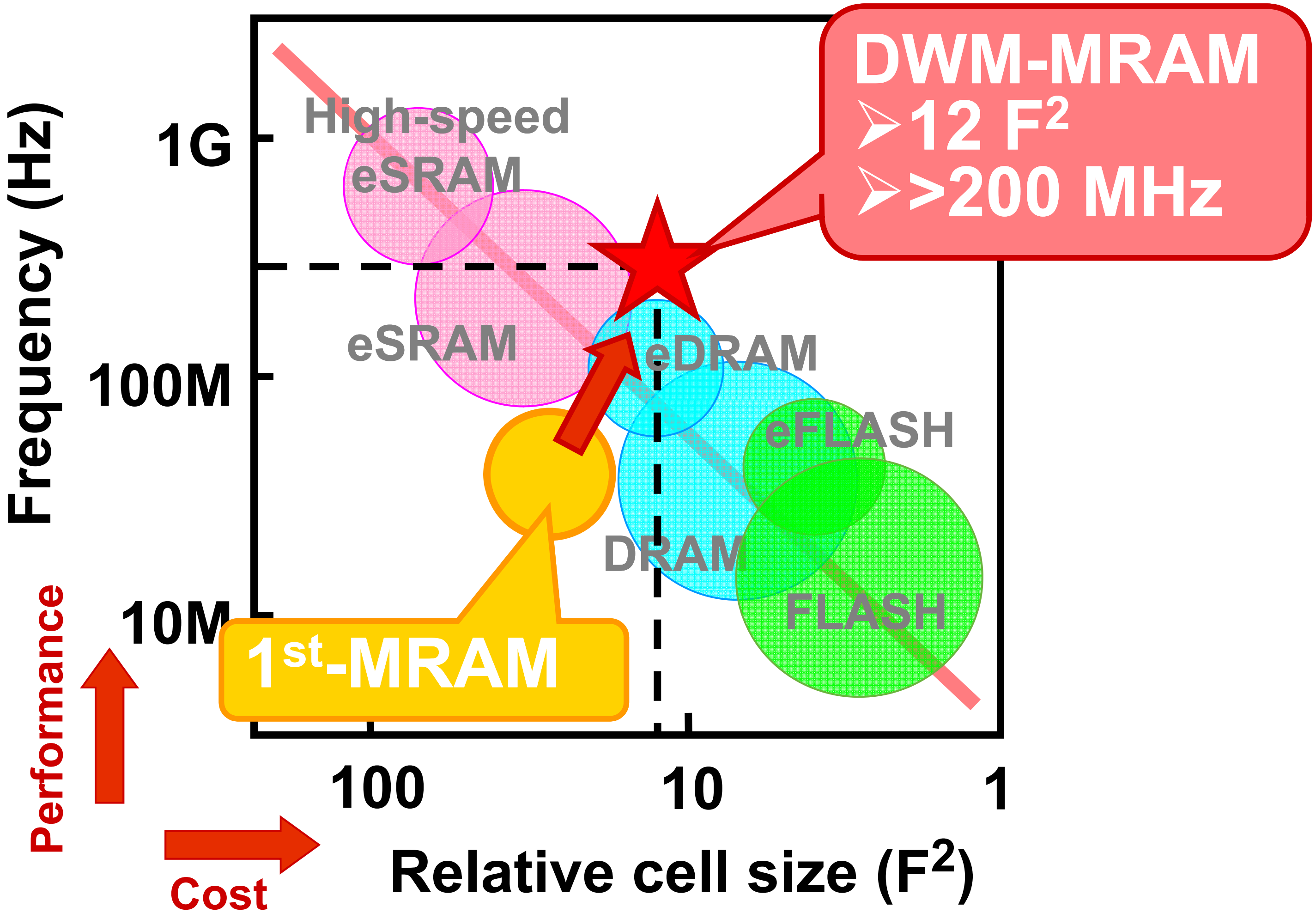
Summary

Comparison of novel and conventional memories

	MRAM	FeRAM	PRAM	FLASH	SRAM	DRAM
Mechanism	Magnetic Tunnel Junction	Ferro-electric	Phase change	Floating gate	Transistor	Capacitor
Non-volatile	○	○	○	○	×	×
Endurance	Unlimited ($>10^{15}$)	Limited ($<10^{13}$)	Limited ($<10^{9}$)	Limited ($<10^{6}$)	Unlimited ($>10^{15}$)	Unlimited ($>10^{15}$)
Access time	Very Fast (~10ns)	Fast (50~100ns)	Medium (>100ns)	Fast (read) Slow (write)	Very fast (~10ns)	Fast (~50ns)
Refresh	No	No	No	No	No	Yes
Cell size	Medium	Large	Small	Very Small	Large	Small
Low voltage	○	○	○	△	○	○
High temperature operation	○	×	×	△	○	△
Application	Work memory	Work memory?	Storage	Storage	Work memory	Work memory

- **MRAM has great potential for use as non-volatile working memory.**

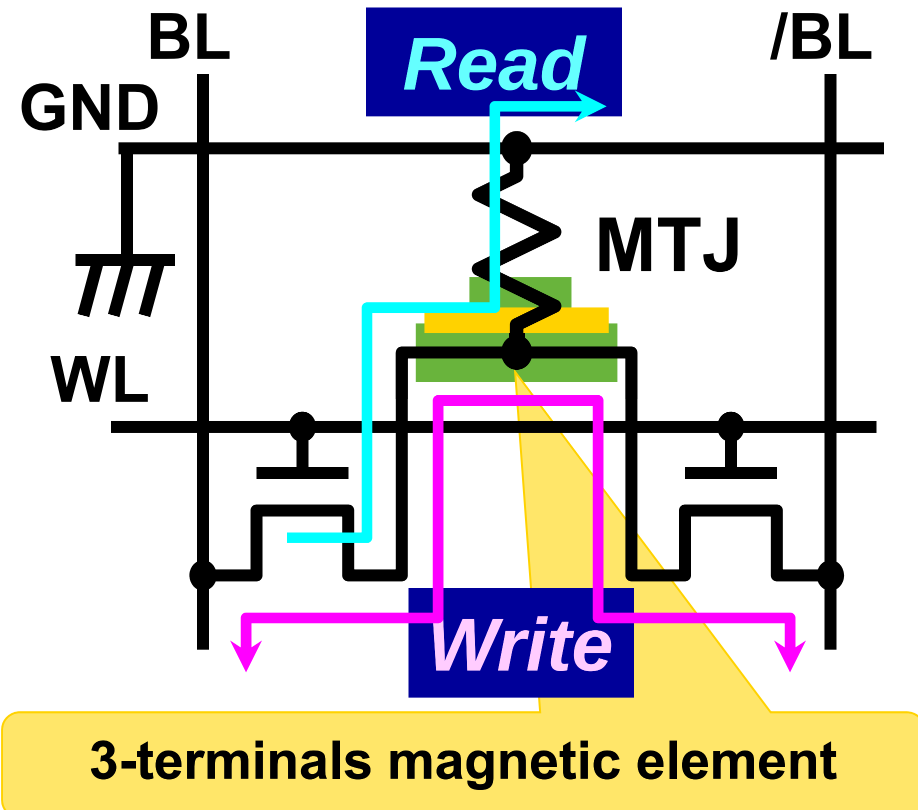
DWM-MRAM cell is located at …

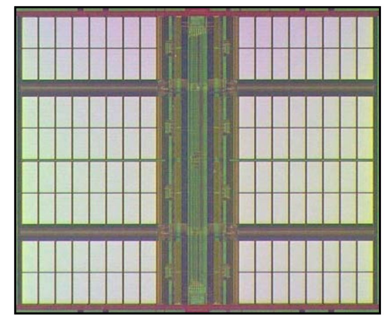


- 12F² & 200MHz cell has the features of eSRAM & eDRAM.
- Very useful for future high-speed embedded memory in SoC.

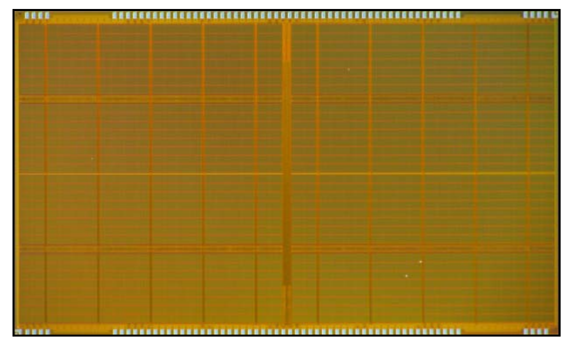
2Tr-1MTJ cell for high-speed MRAM operation

2Tr-1MTJ cell





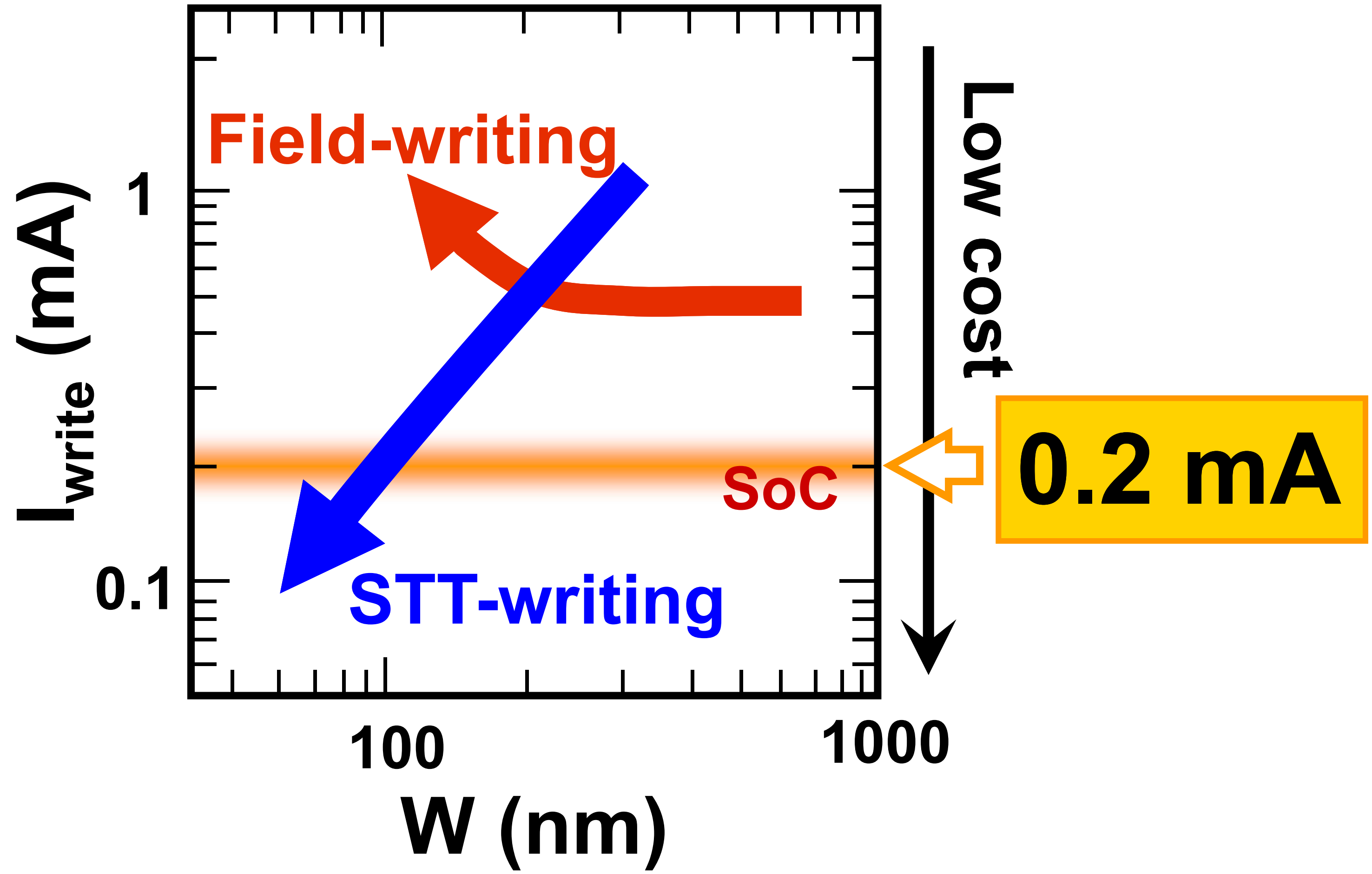
250 MHz (ASSCC 2007)



32 Mbit (ISSCC 2009)

- **No problem with either write disturbance or read one**
  ⇒ Great advantage for high-speed operation

Key issue : Reduction of write-current (I_{write})



- <0.2 mA ⇒ 2Tr-1MTJ cell has higher cost performance than conventional memories used in SoC.
- Spin-transfer torque switching is promising for lowering write-current.

Spin transfer torque switching

Conventional Spin transfer torque switching

- F.J.Albert et al., Appl. Phys. Lett., 77-23, 3809, 2000.

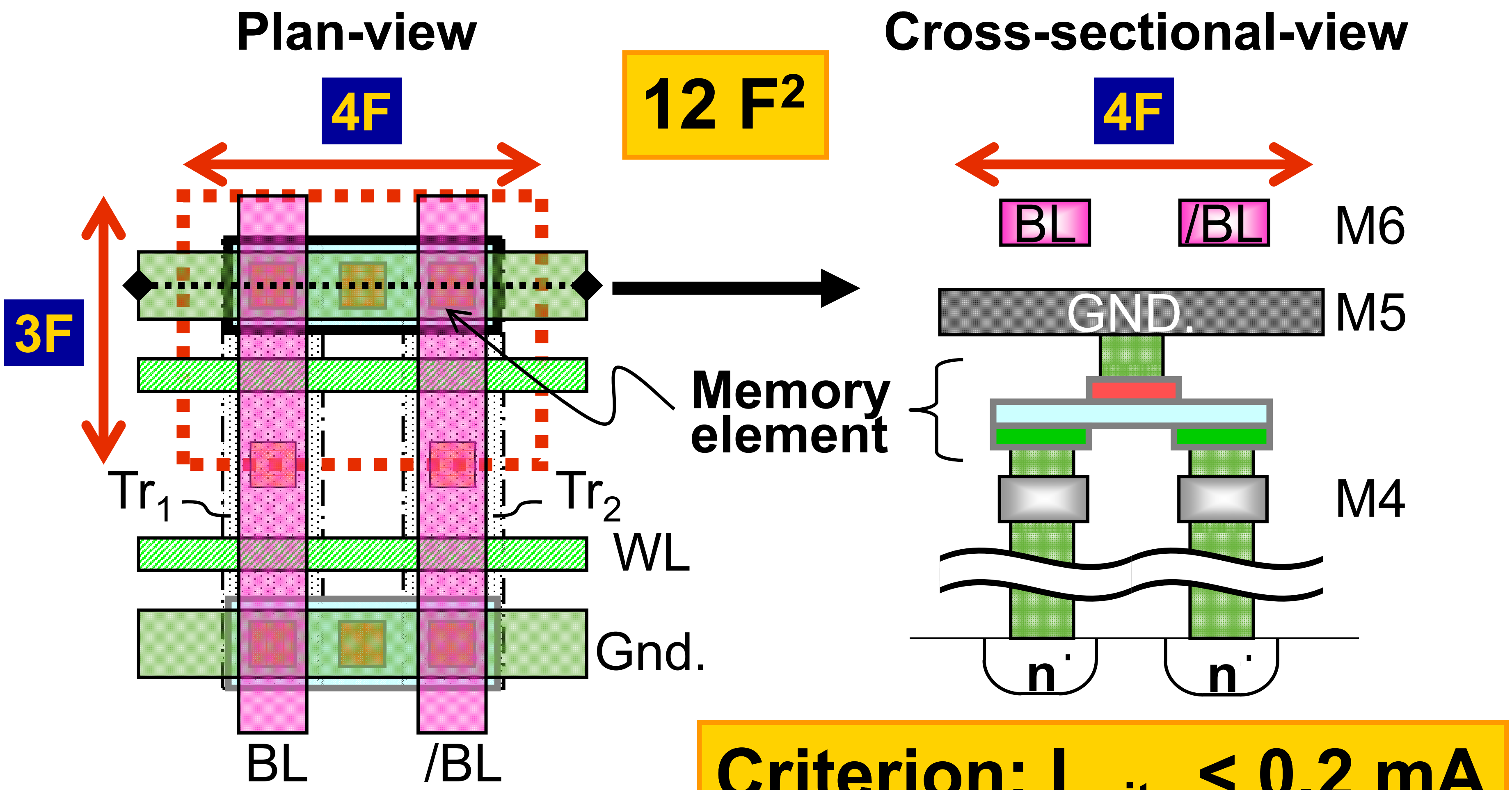
Current-induced domain wall motion (DWM)

- A.Yamaguchi et al., Phys. Rev. Lett. 92, 077205, 2004.
  - NiFe (in-plane)
- M. Yamanouchi et al., NATURE, 428, P.539, 2004.
  - GaMnAs (perpendicular)

Positive characteristics of DWM elements

- Suitable for 2Tr-1MTJ cell
- Scalable write-current & write-speed
- Sufficient thermal stability without write current increase
- Suppression for read disturbance & tunneling barrier damage in write process
- CMOS process compatibility

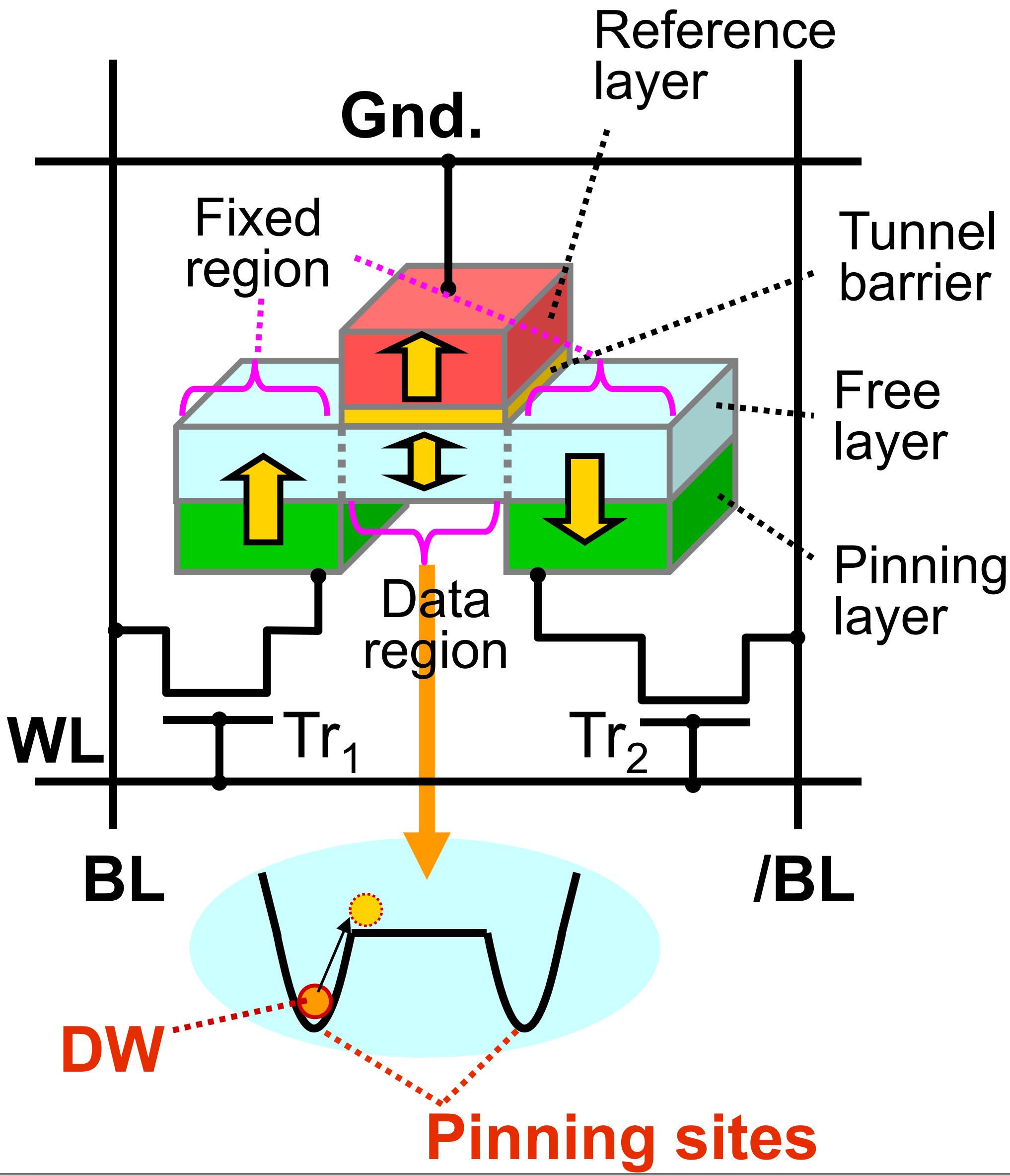
Minimum cell layout for 2Tr-1MTJ DWM cell

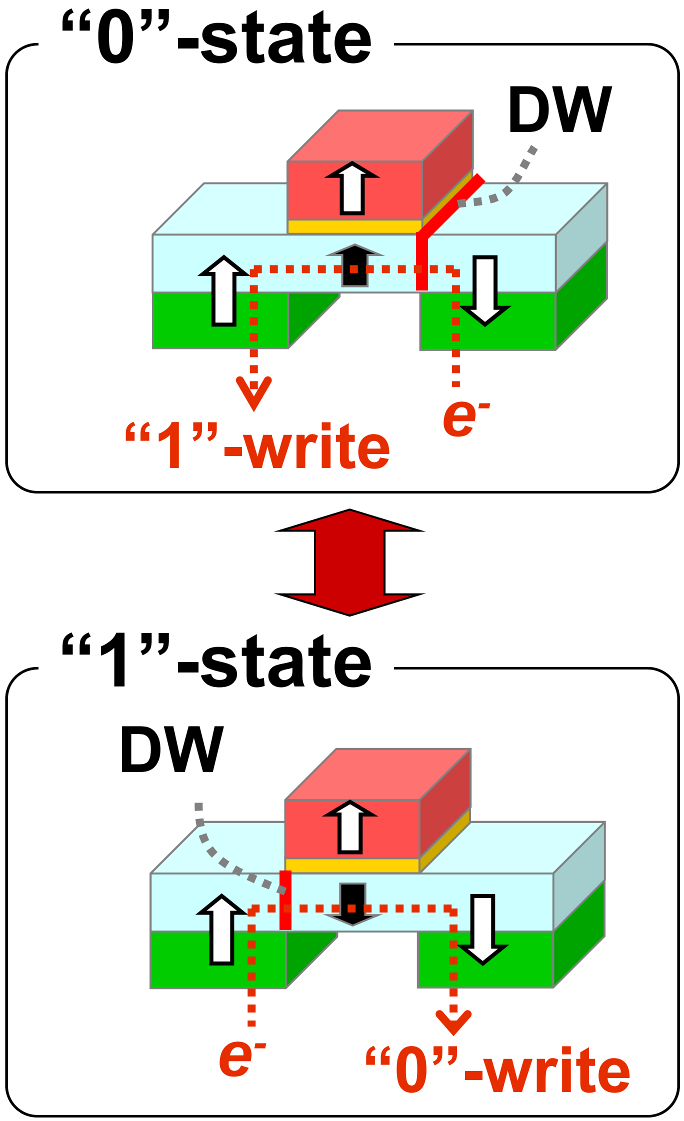


Criterion: I_{write} < 0.2 mA

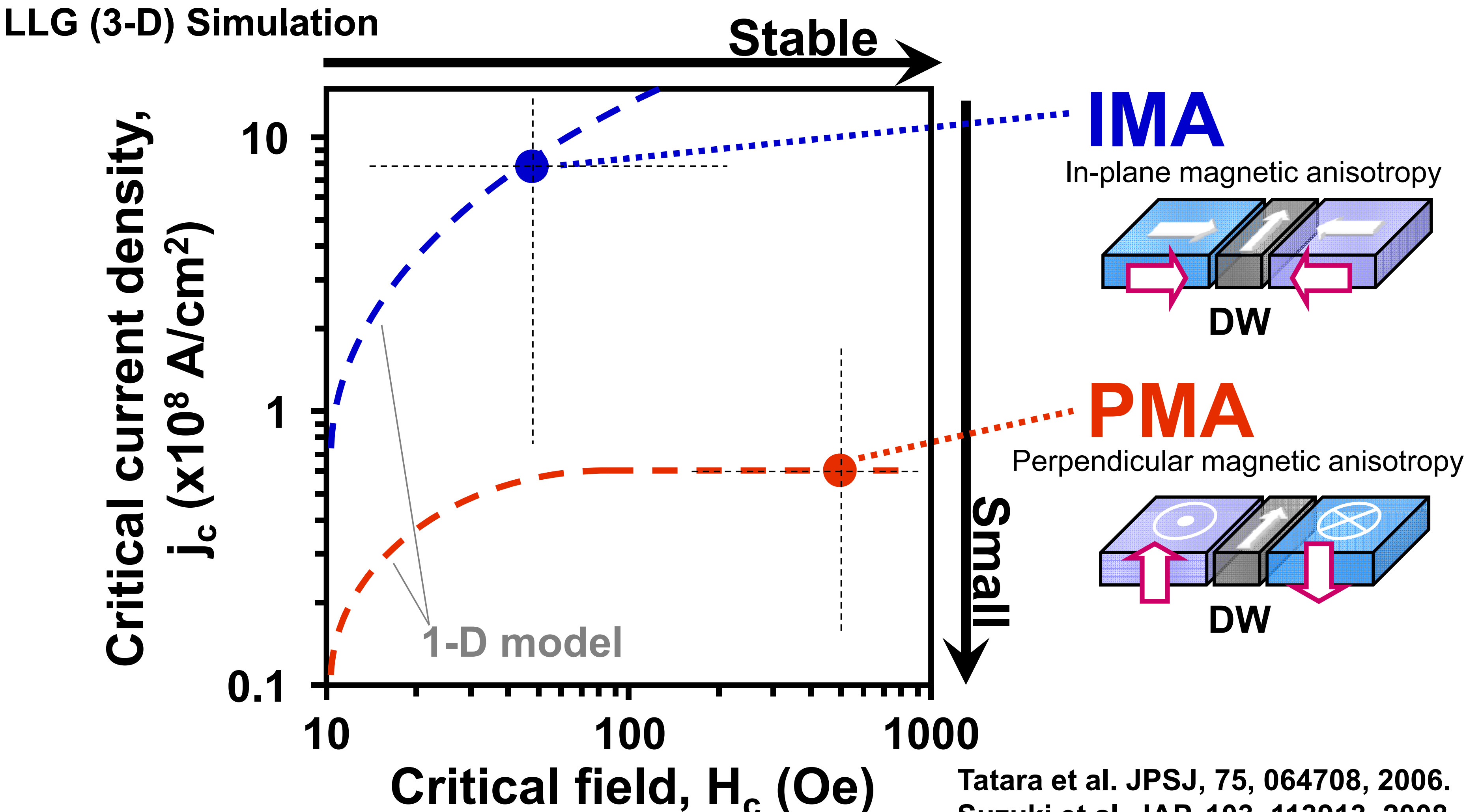
- **12F² ➔ 0.1 μm² @ 90-nm rule**
- **12F² is possible only when the write-current is < 0.2 mA**

Device structure for minimum cell layout





What kind of material should be chosen ?



Tatara et al. JPSJ, 75, 064708, 2006.
Suzuki et al. JAP, 103, 113913, 2008.

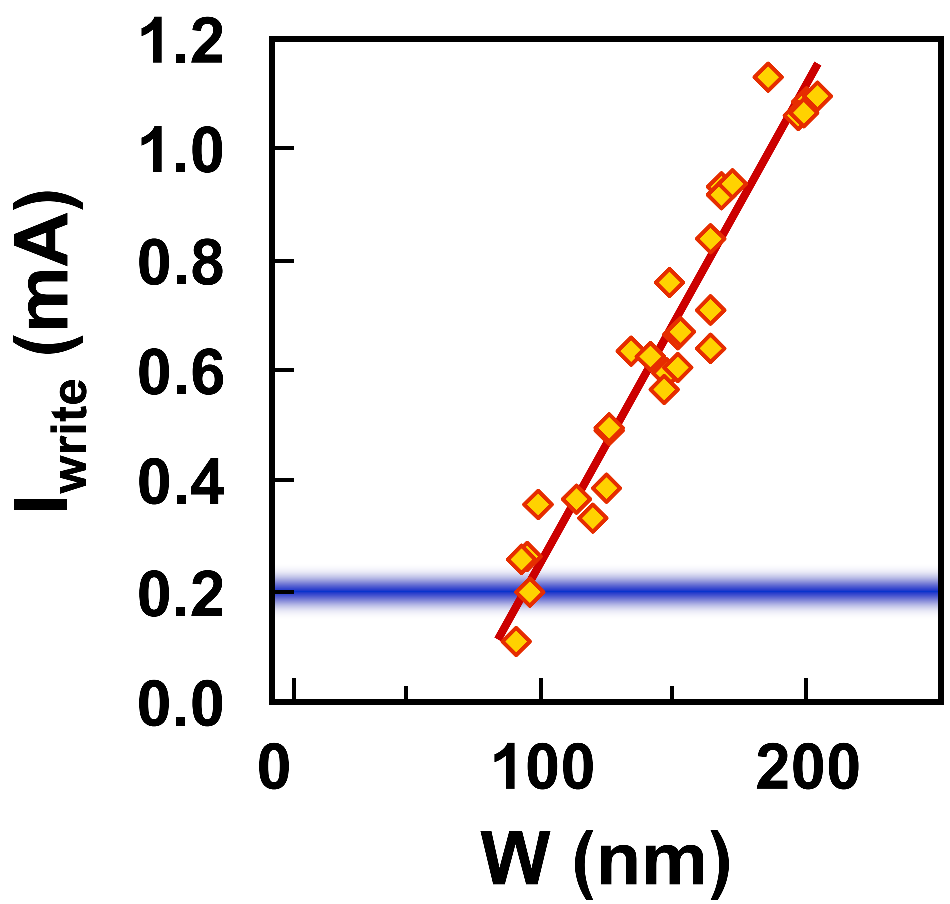
- **Using PMA, much smaller cell area with much better stability can be achieved.**

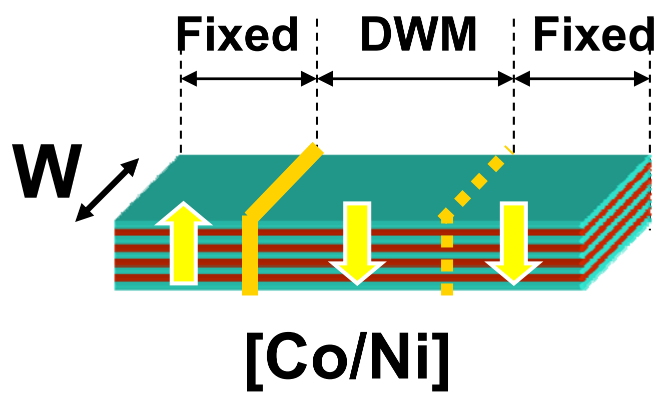
DWM materials

Material	Anisotropy	Temp. (K)	Minimum J_{th} (A/m^2)	Pinning field (Oe)	Velocity (m/sec.)
$[Co/Ni]_N$	Perpendicular	R.T.	0.3×10^{12}	200	60
$[Co/Pt]_N$	Perpendicular	R.T.	1.8×10^{12}	500	-
CoCrPt	Perpendicular	R.T.	1.0×10^{12}	500	-
GaMnAs	Perpendicular	100	8.0×10^{8}	40	22
NiFe	In-plane	R.T.	1.0×10^{12}	5	110

- **Co/Ni is the best material for DWM, because of its small J_{th} with large pinning field and high velocity.**

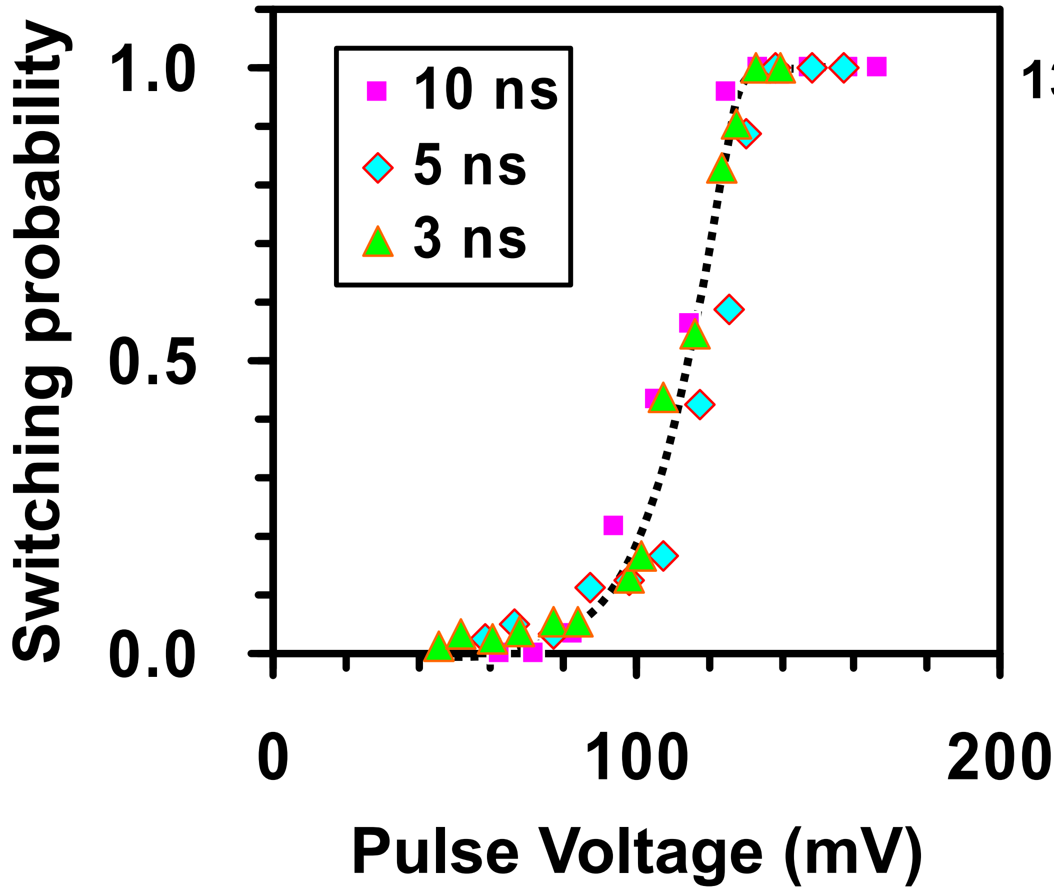
Write-current, I_{write}

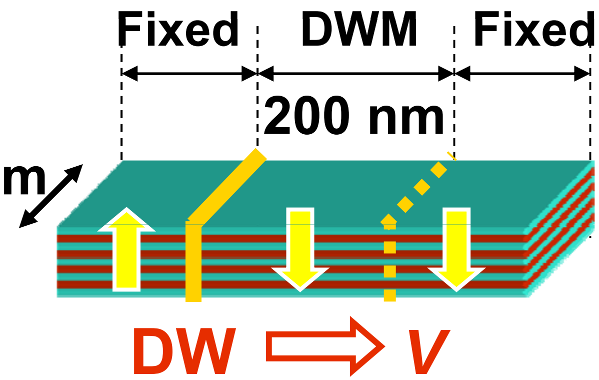




- At less than 100 nm width, the write-current becomes less than 0.2 mA. ⇒ The most important criterion is satisfied.

Write-time, t_{write}





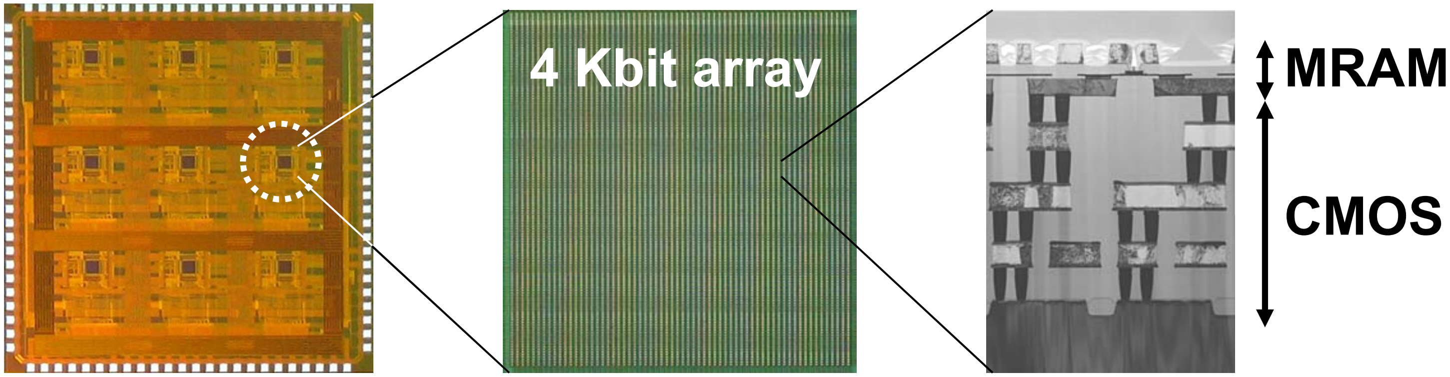
V_{DWM} > 50 m/s

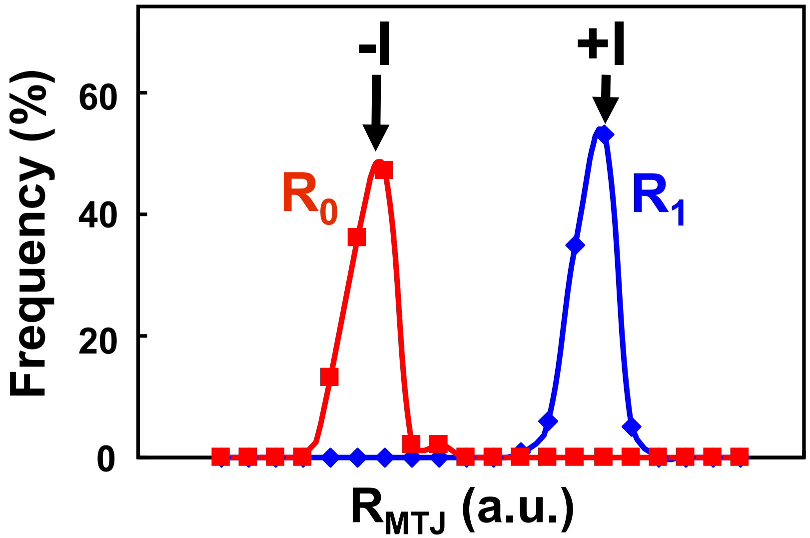
t_{write} < 2 ns
@ ℓ ~ 90 nm

>200 MHz

- More than 200 MHz operation is promising.

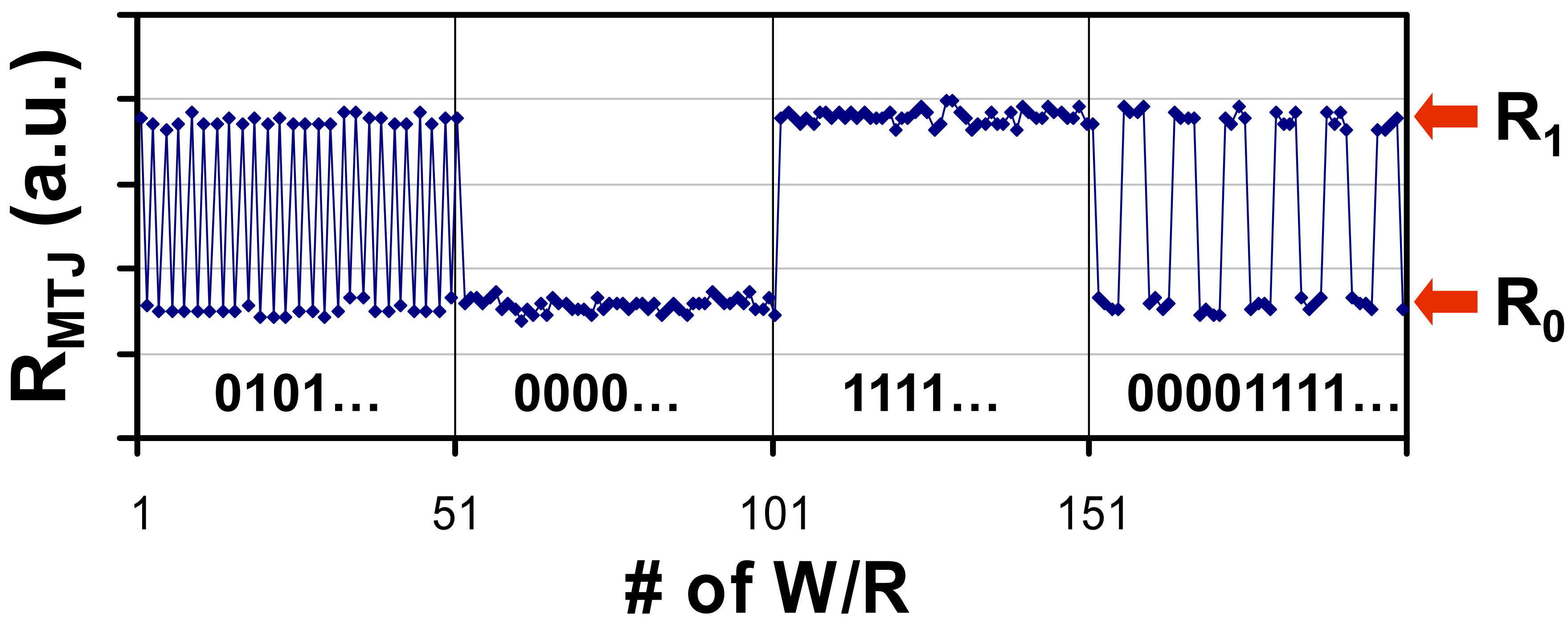
Memory operation : 4 Kbit array





- The two resistance states of the MTJ are clearly separated.
- The change of resistance is consistent with current direction.

Repeat test for write and read operation



- Good reproducible switching and overwrite properties are confirmed.

Summary

DWM MRAM with 2Tr-1MTJ high-speed cell

- 12 F^2 (0.1 μm^2 @ 90 nm rule), >200 MHz
- Scalable write-current & write-speed with sufficient thermal stability
- 4 kbit memory array operation has been demonstrated

Co/Ni multilayer film with perpendicular magnetic anisotropy is the answer for DWM MRAM

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Thank you