My (Optimistic) 3 Cents to Flash Scaling

Electrostatics, Resonant Tunneling and Planar Stacks

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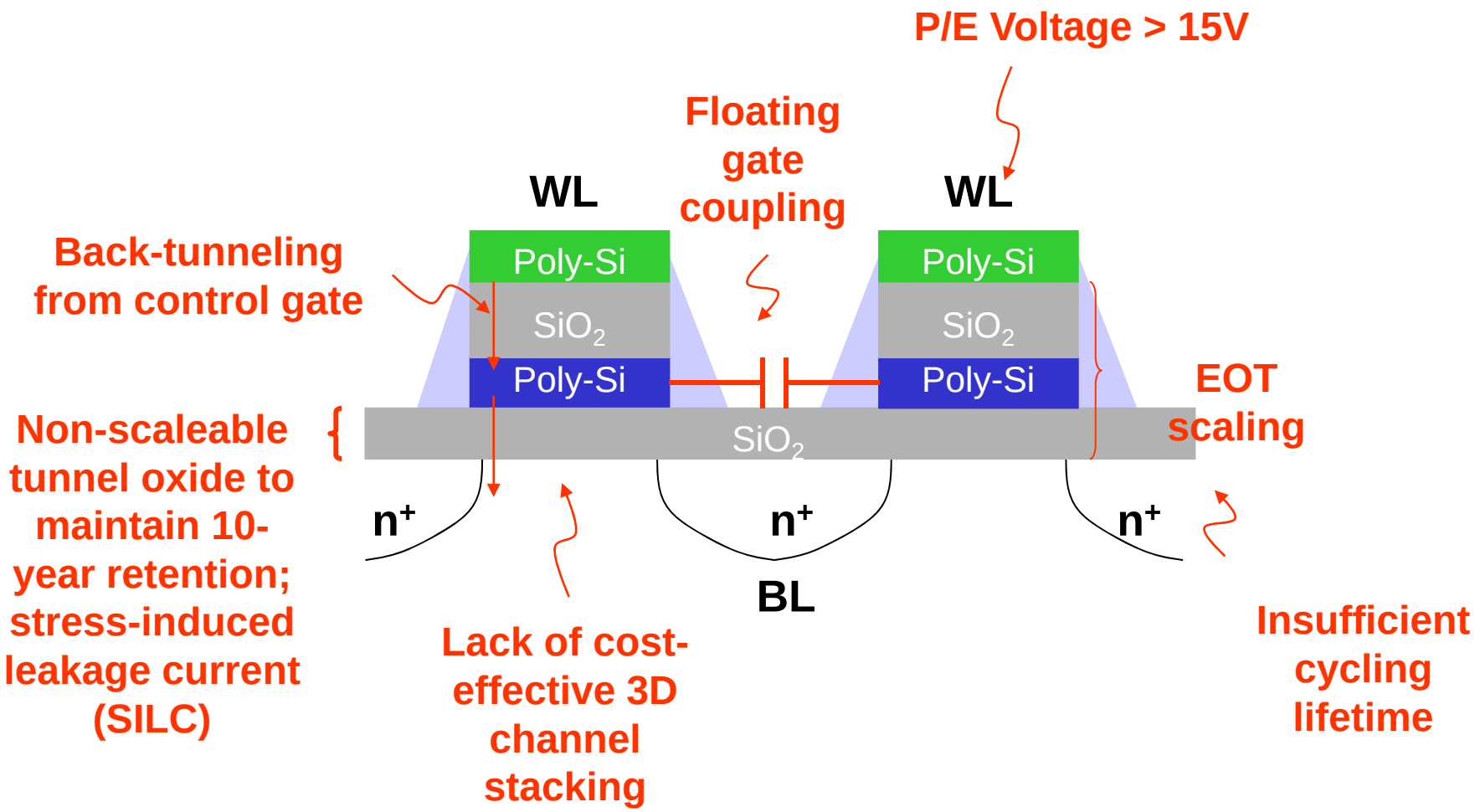
Flash Memory Scaling Challenges



Material Choices for Flash Memory

Charge Storage Medium

Continuous

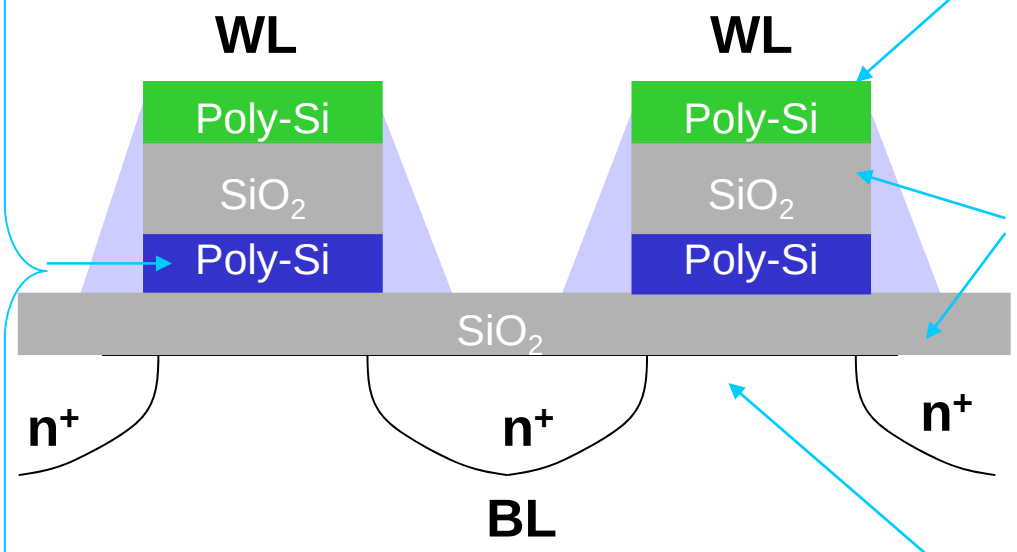
SONOS-type:

SiN, Al_2O_3, HfAlO, HfSiO, AlN, HfO_2, Ta_2O_5 *etc.*

NC Memory:

Si, Ge, SiGe, Au, Pt, Ag, Ni, $NiSi_2$, $TiSi_2$, W, Co, C_{60}, CNT *etc.*

Redox Molecules



Control Gate

TaN and other high WF metal

Tunnel & Control Oxide

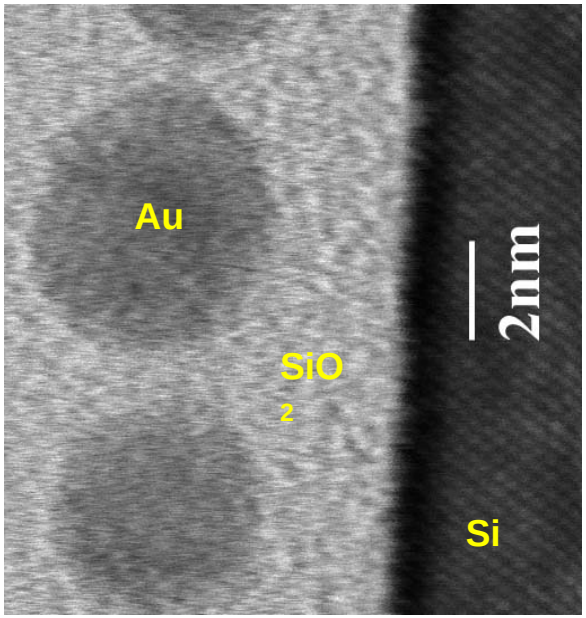
SiO_2, Al_2O_3, HfO_2, HfAlO, hybrid, pores, resonant, *etc.*

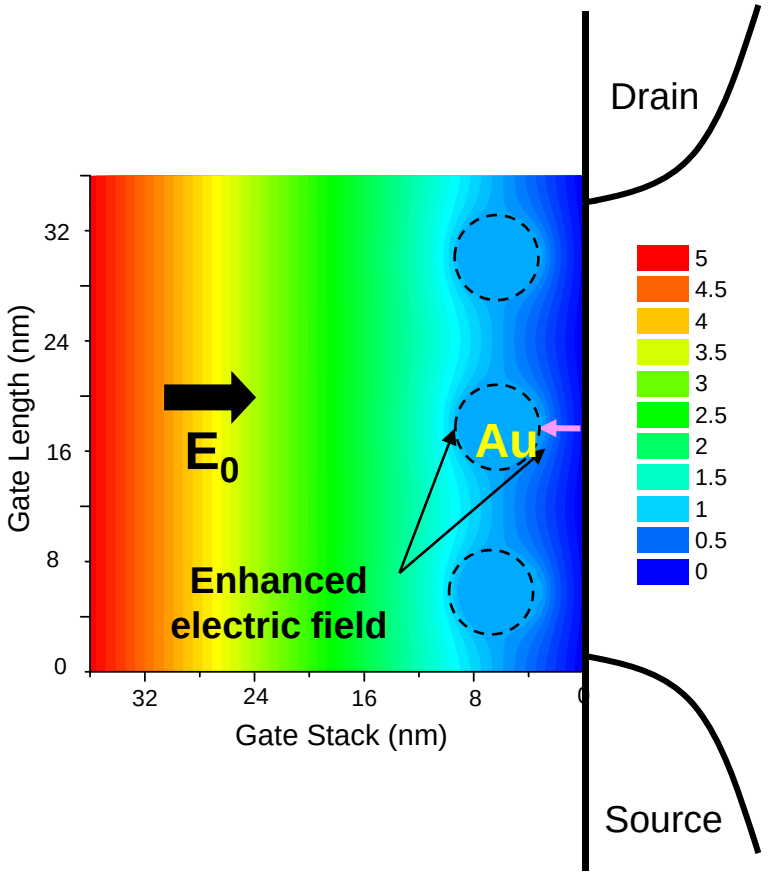
Sensing Channel

Bulk, SOI, Ge, TFT, NW, CNT

T. H. Hou, et al, MRS, March 2008

3D Electrostatics in the Nanoscale:
Use of metal, self-assembled 3D shape and pores



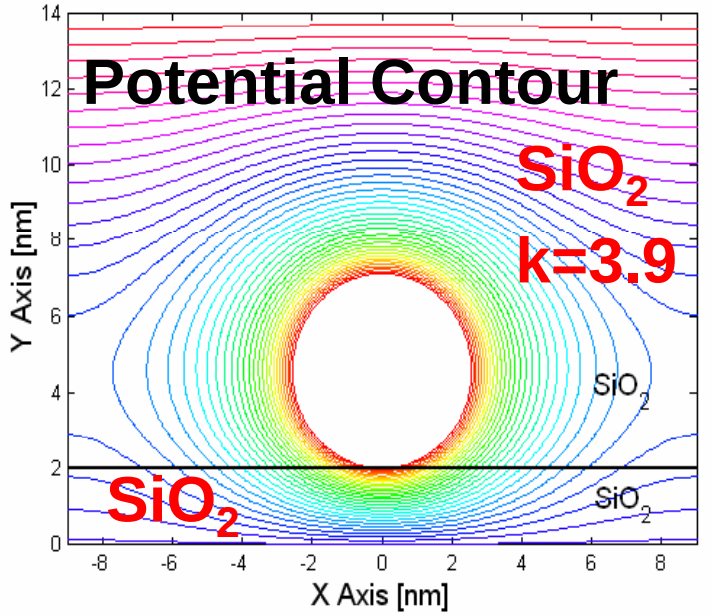


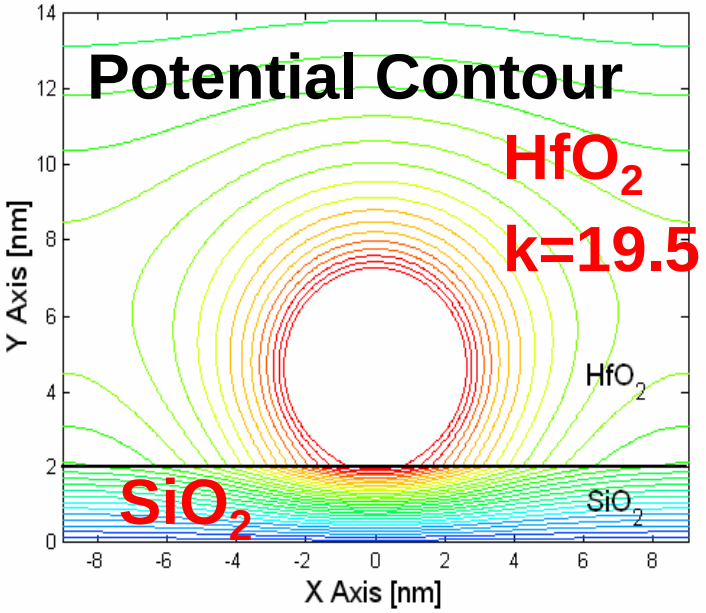
C. Lee, et al, *IEEE Elec. Dev. Lett*. 26 (2005) 879.

Material and Geometry in Nanoscale

Metal NC vs. Semi NC

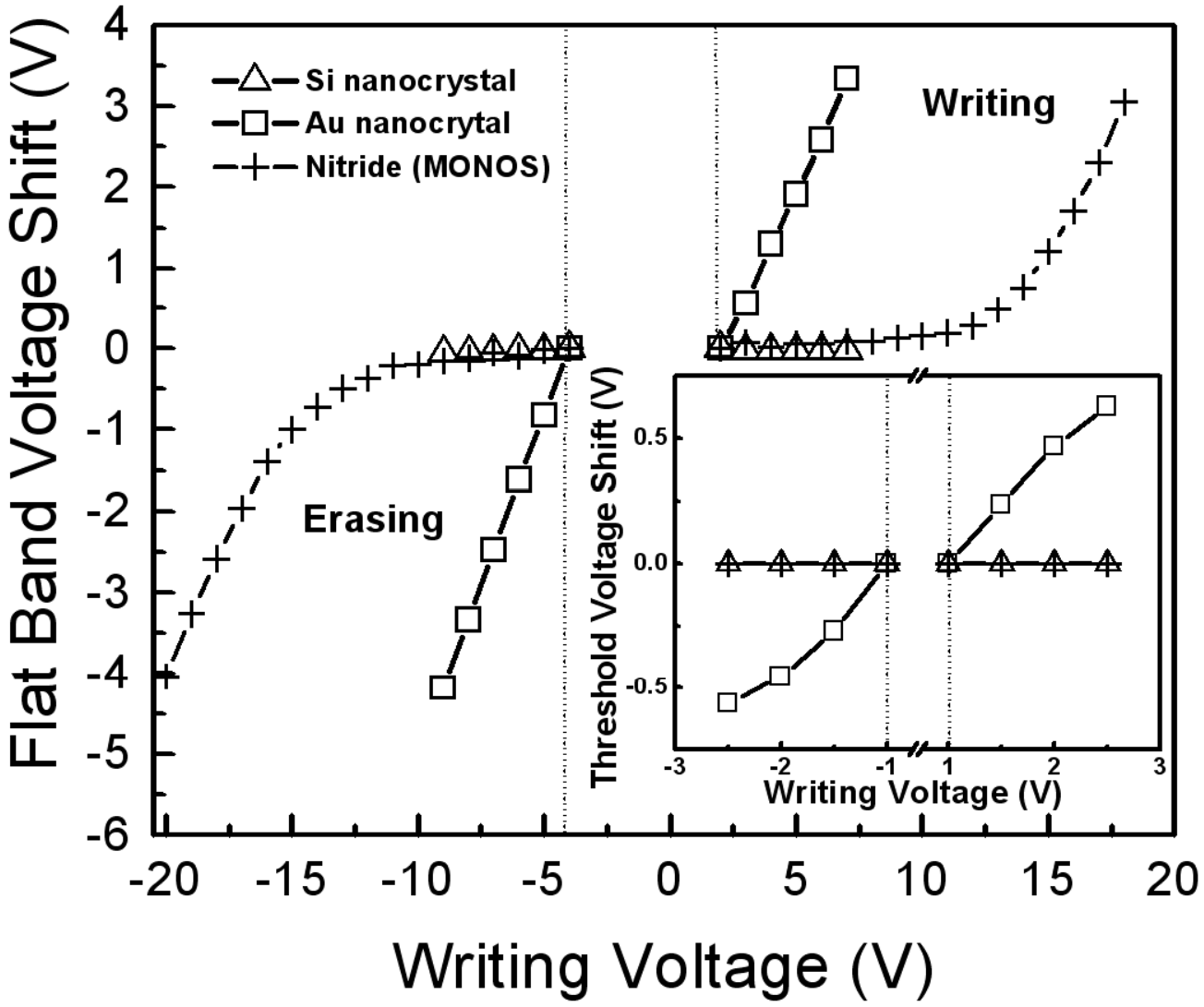
- Discrete storage (nanocrystals or traps), should be the highest k to have electric fields point toward it.
- If the dielectric has higher k, then electric field diverge away.
- The tunnel oxide needs to have lower k than control oxide for channel-injection operations.
- 3D electrostatics is a must inclusion for the device design.





T-H. Hou, *et al, IEEE Trans. Elec. Dev*. 3095 (2006).

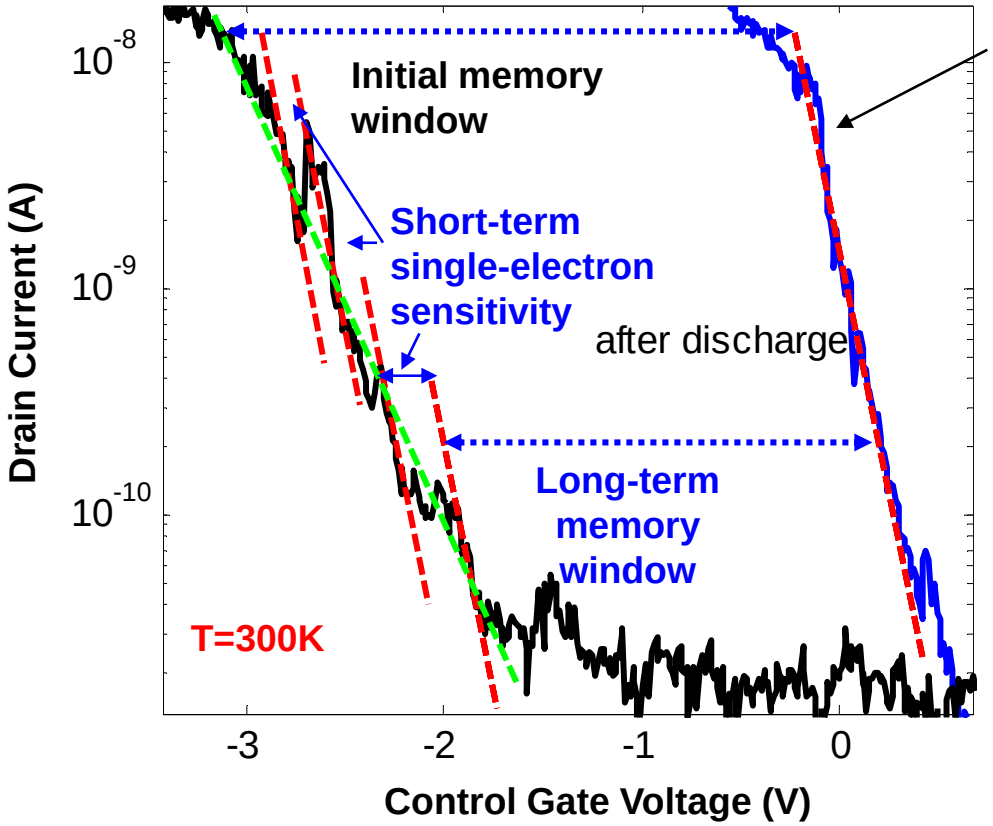
3D Electrostatics: Low-Voltage Operations

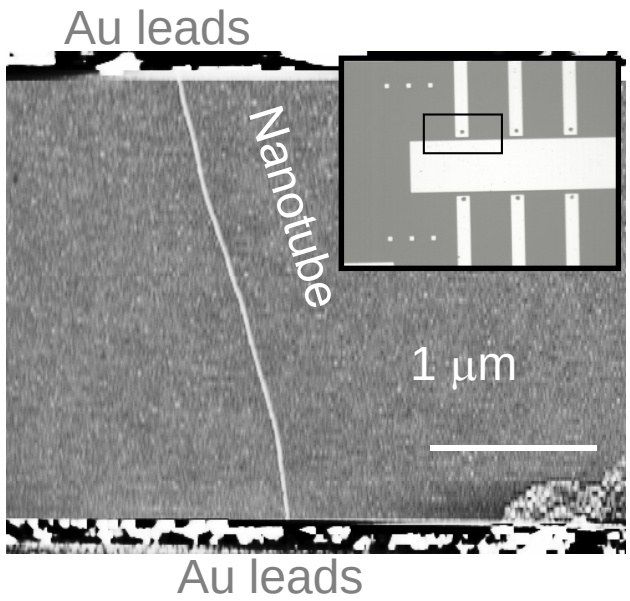


- Same tunnel and control oxide
- Devices NOT optimized
- Just to show electrostatic behavior

C. Lee, et al, *IEEE Elec. Dev. Lett.*, 26, 879 (2005).

Optimal Electrostatics for Flash Memory



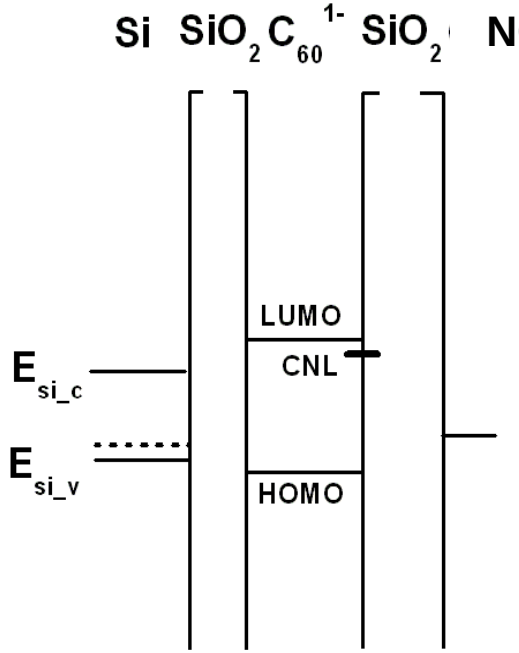


$$\frac{V_{memory}}{V_{P/E}} \geq 60\%$$

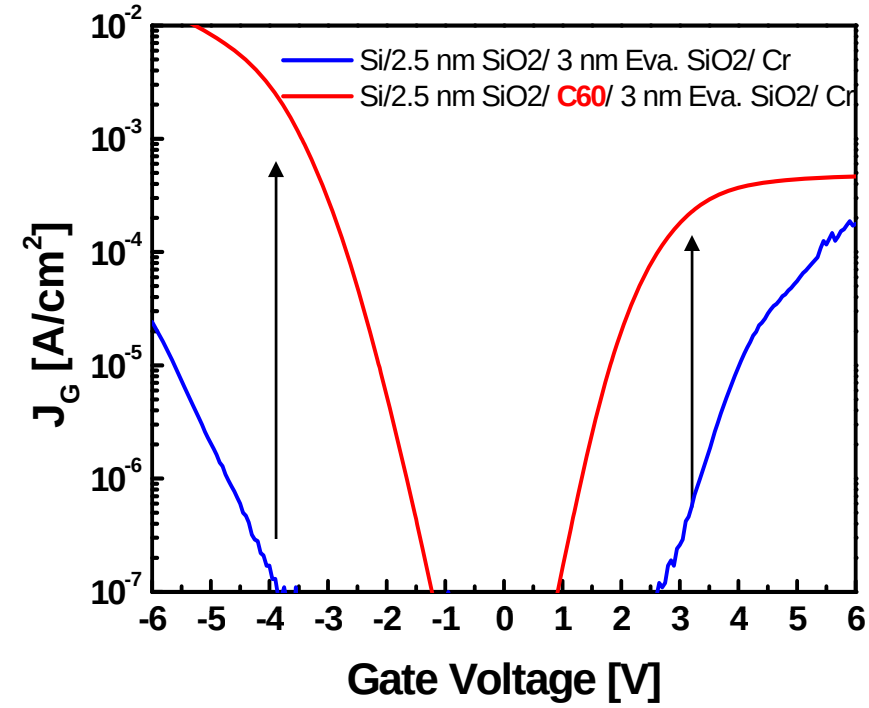
- **Dimension**: Control gate > control oxide > storage > channel > tunnel oxide *(Carbon nanotubes not manufacturable yet…)*
- **Dielectric constant:** Storage > dielectric > channel

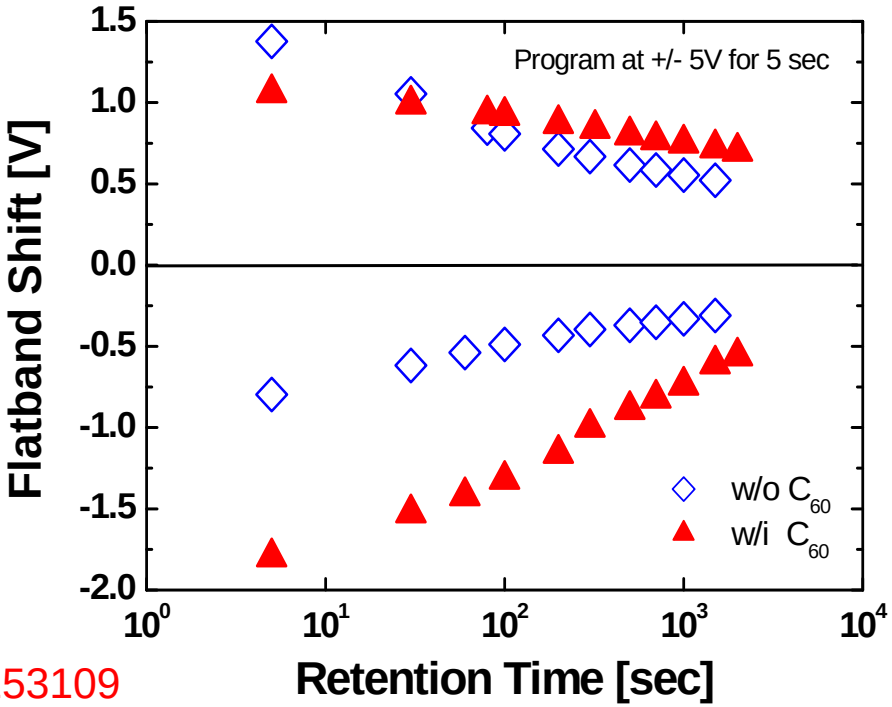
U. Ganguly, *et al, Appl. Phys.* 87 (2005) 043108

Molecule-Enabled Resonant Tunneling Barrier



Resonant tunneling through C_{60} significantly increase $t_{retention}/t_{P/E}$

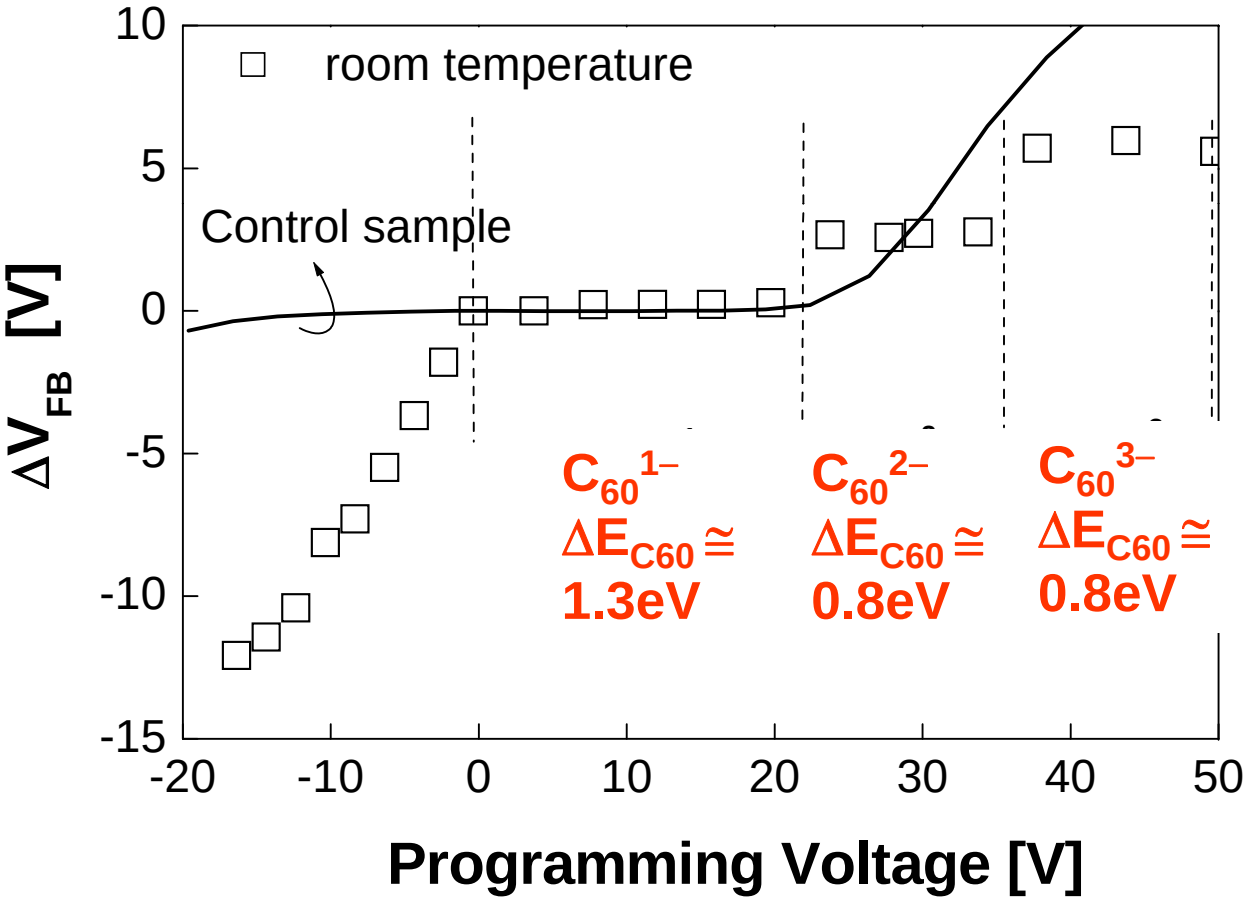


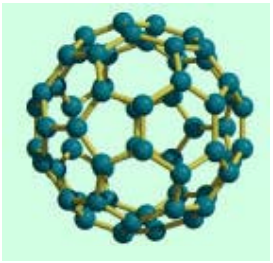


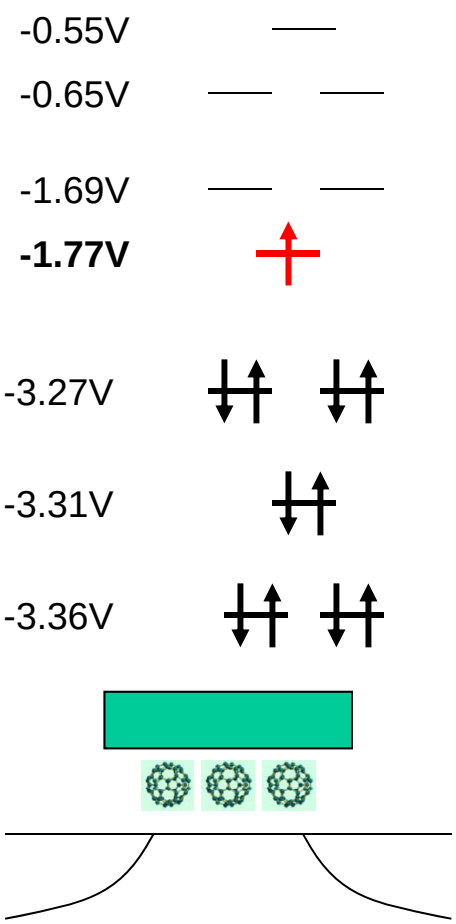
T.-H. Hou, et al, *Appl. Phys. Lett.*, 92 (2008), 153109

Redox States of C_{60} in Gate Stack

- **CMOS flash memory to operate the charge state of a molecule (≅ 1nm)**

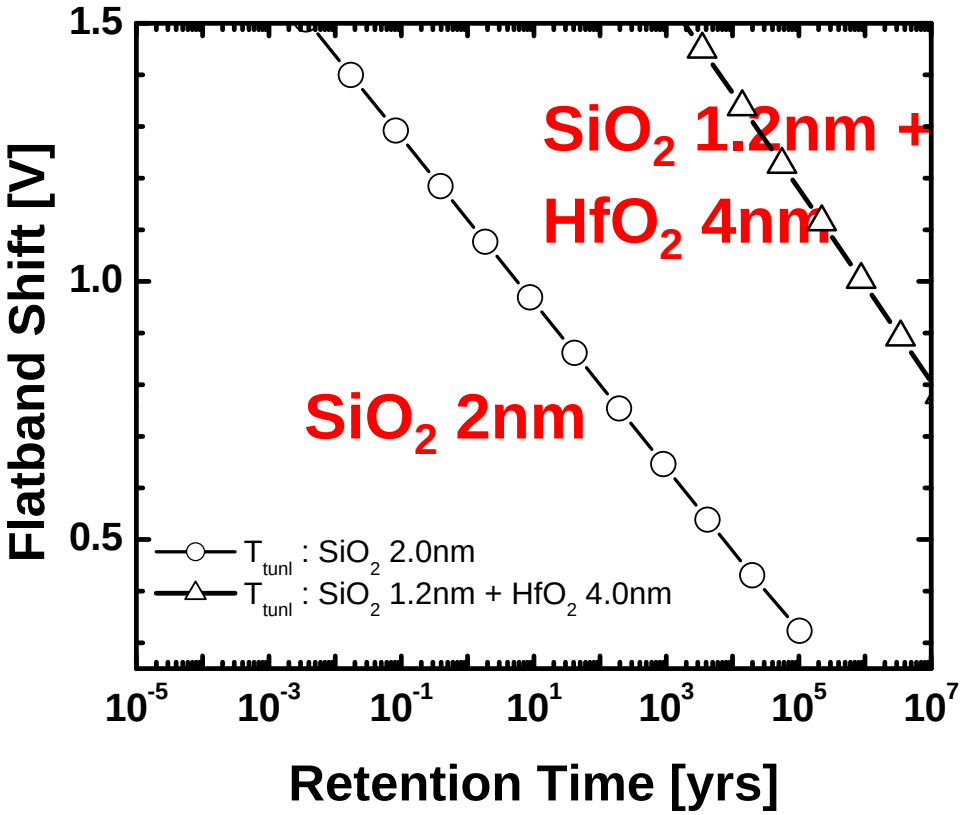


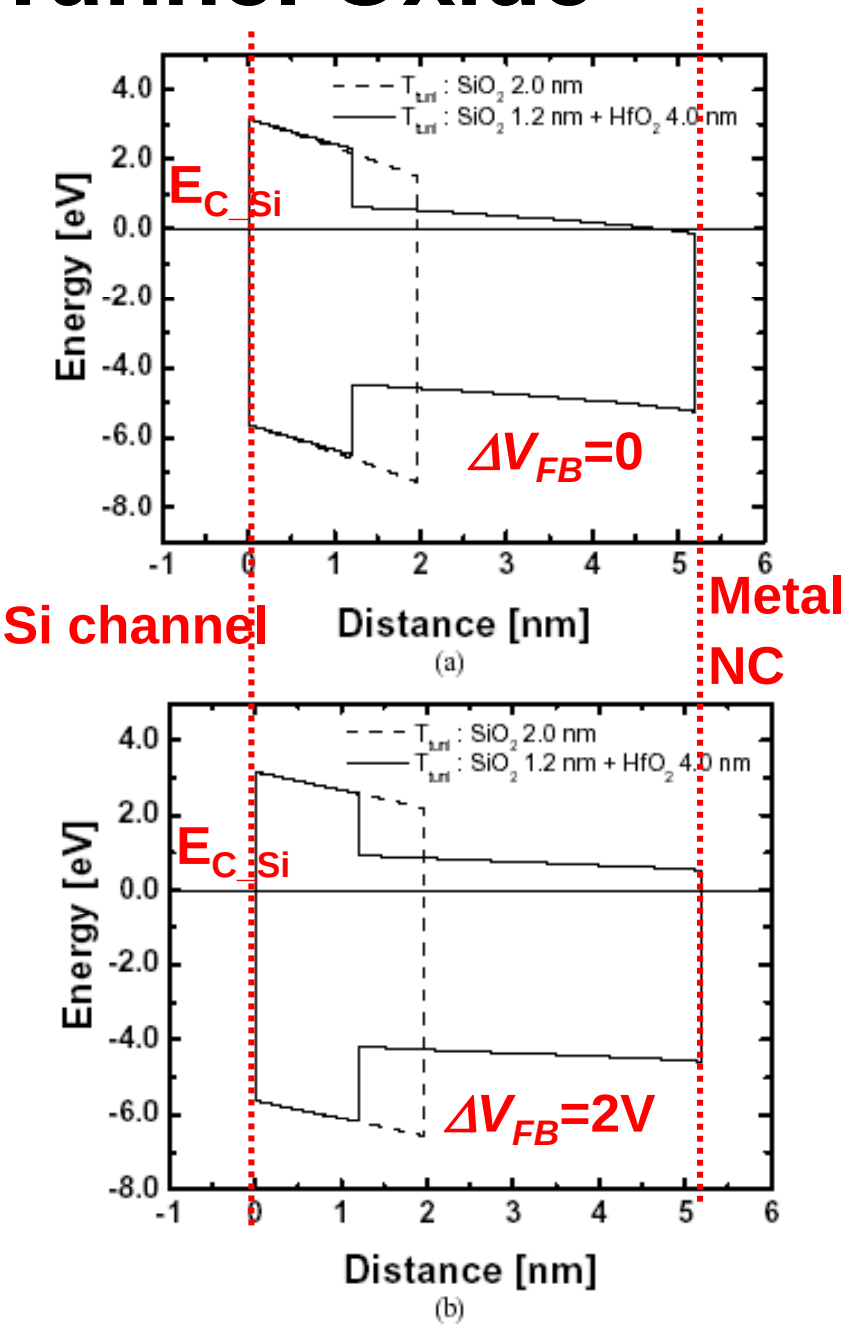




T-H. Hou, *et al, Appl. Phys. Lett*. 89 (2006) 253113

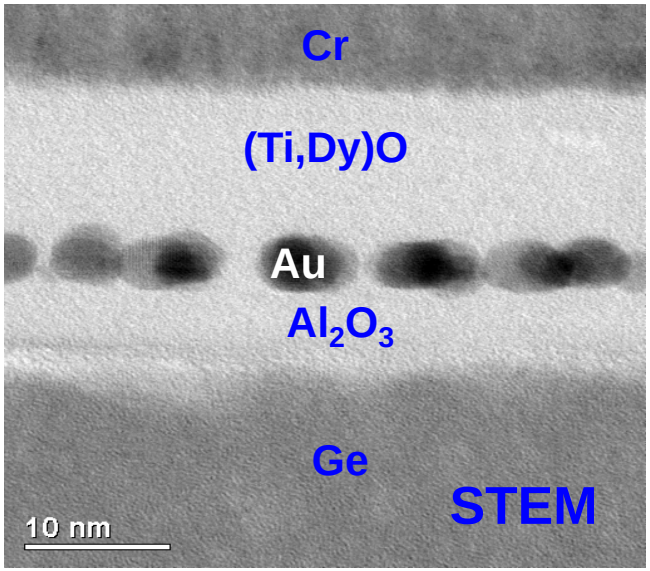
Heterogeneous Tunnel Oxide

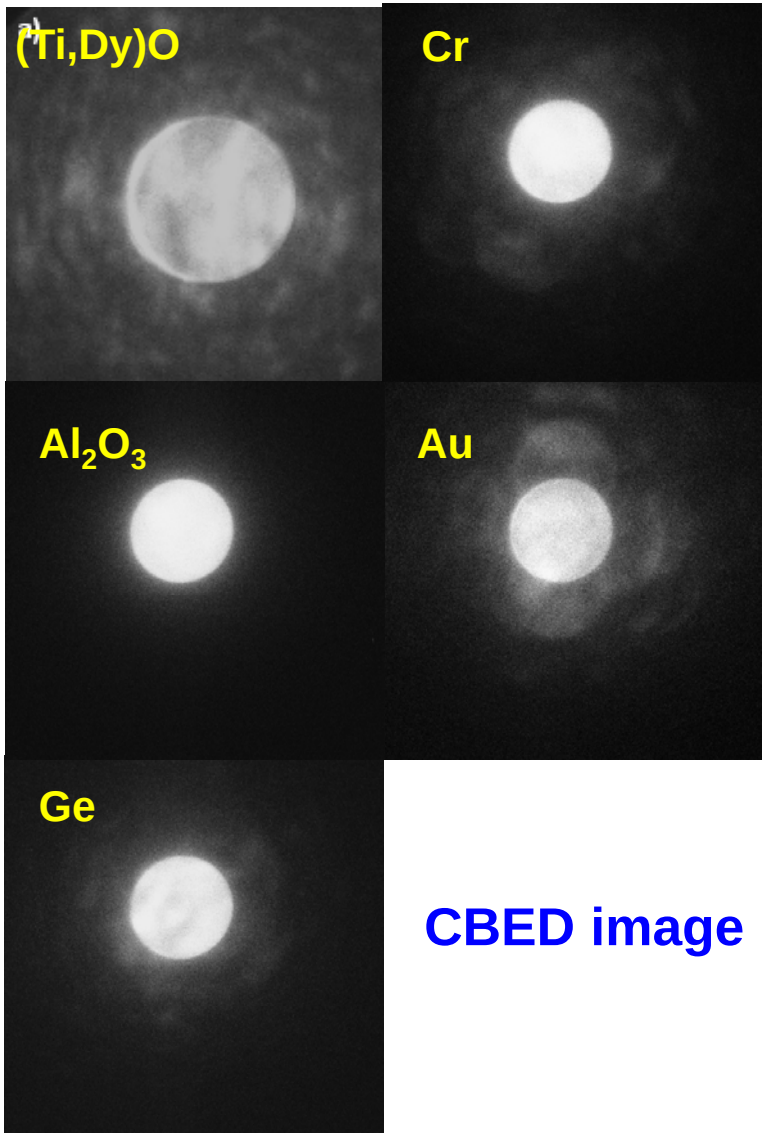




- Bi-layer tunnel oxide works well for metal NC.
- F-N tunneling during P/E and direct tunneling during retention.

3D Stacks of UTB Ge TFT Flash





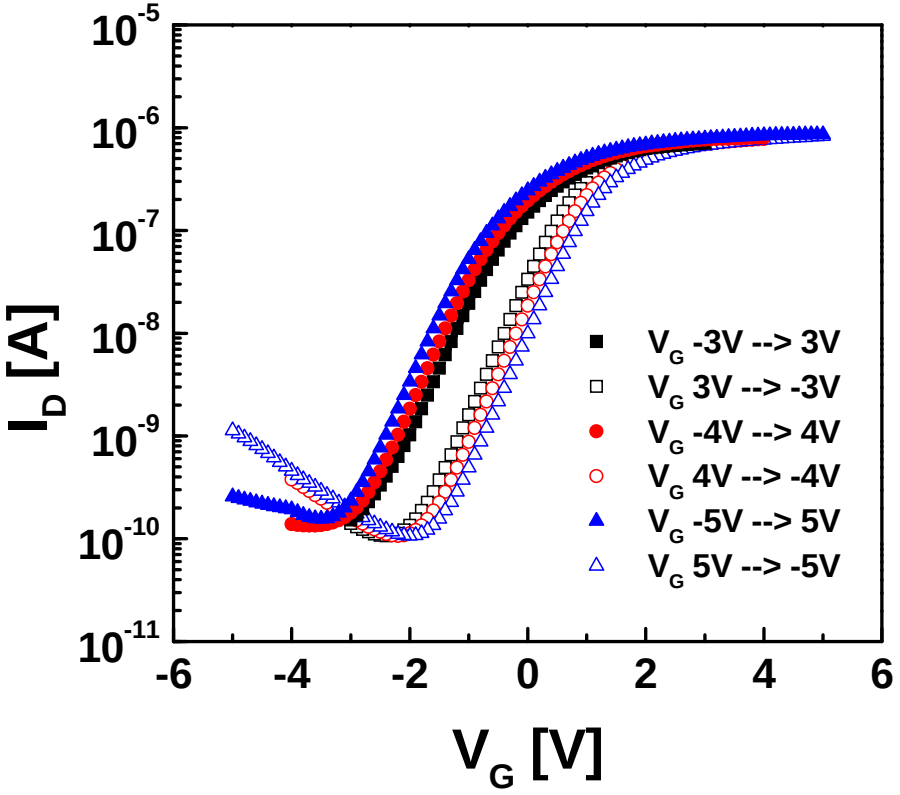
Bulk thermal SiO_2 substrate
CMP 13nm in-situ doped Ge
ALD Al_2O_3 tunnel oxide
Self Assebled Au NC
ALD (Ti,Dy)O control oxide

CBED image

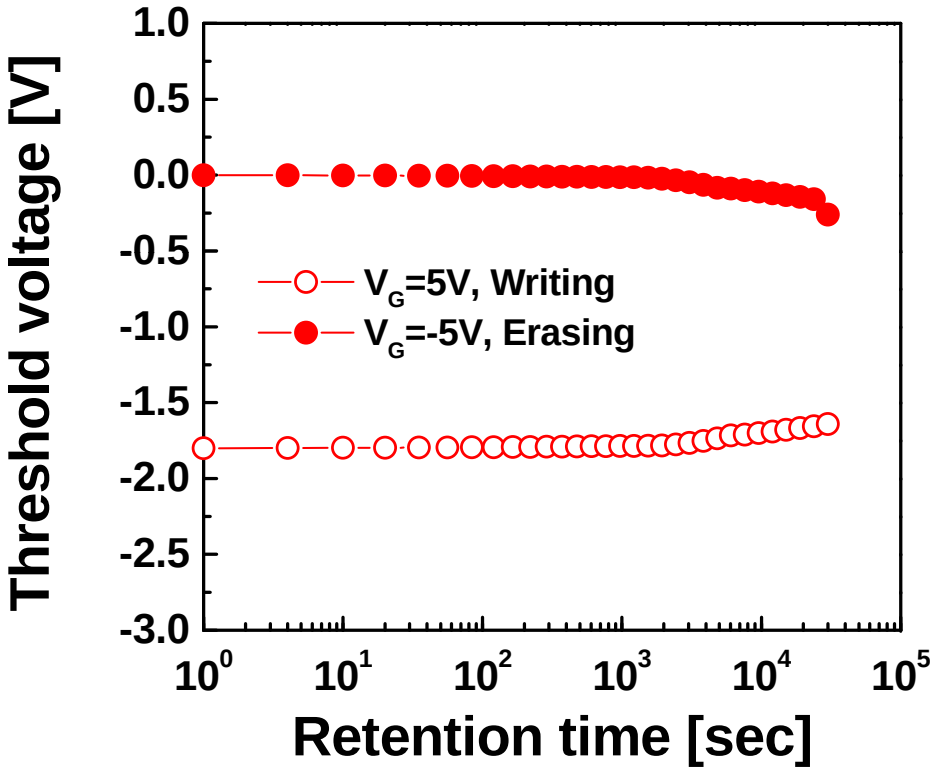
J. Lee, et al, MRS 2009 (tbp).

3D Stacks of UTB Ge TFT Flash

– Low voltage design: ±5V and 3μA I_{ON}



P/E Memory Window



Retention Characteristics

Summary

- 3 possible principles to further enable voltage and density scaling
  - Electrostatics from self-assembled materials (nanocrystals, pores, etc.)
  - Specifically designed tunnel barriers (resonant tunneling, molecular orbitals, etc.)
  - Planar 3D stacks of UTB CMP Ge channels
- There is still much room at the bottom even for flash memory.
- If physically possible and material-wise feasible, engineers can always make it work.