Foundry Perspective on Embedded Memory

Panel VI: Needs and Models for Collaborative Research

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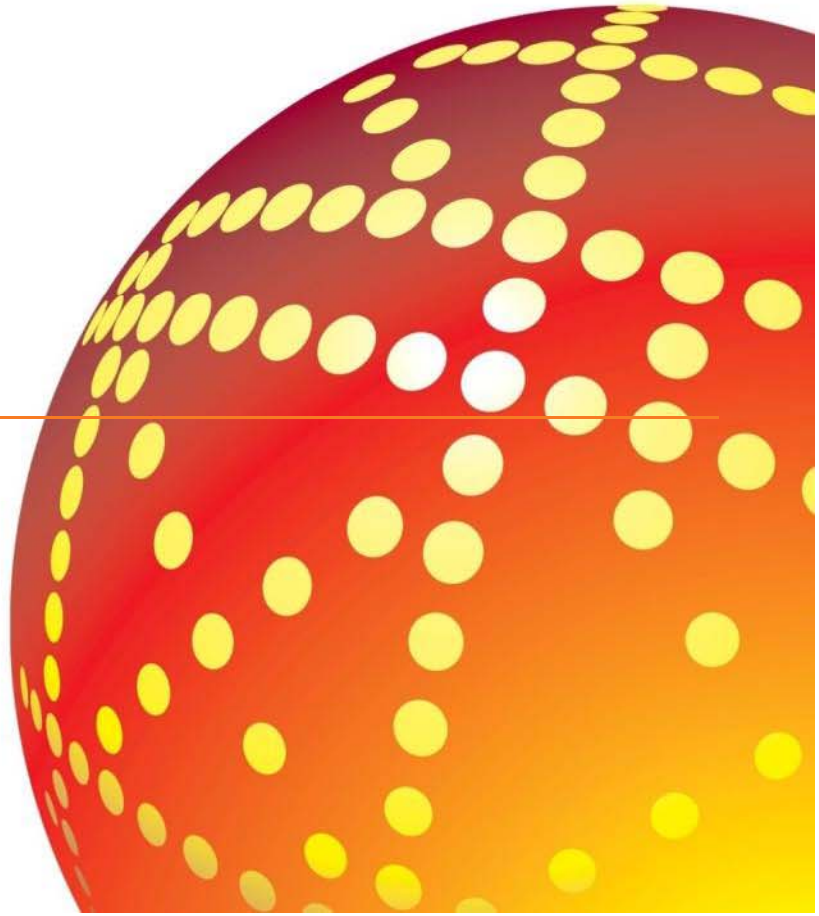
GLOBALFOUNDRIES



October 21, 2009

Memory Options

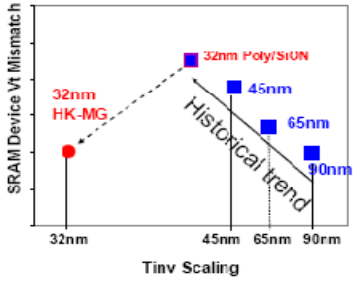
- Memory can be delivered in three forms:

1. MCM
2. 3D integration
3. Embedded

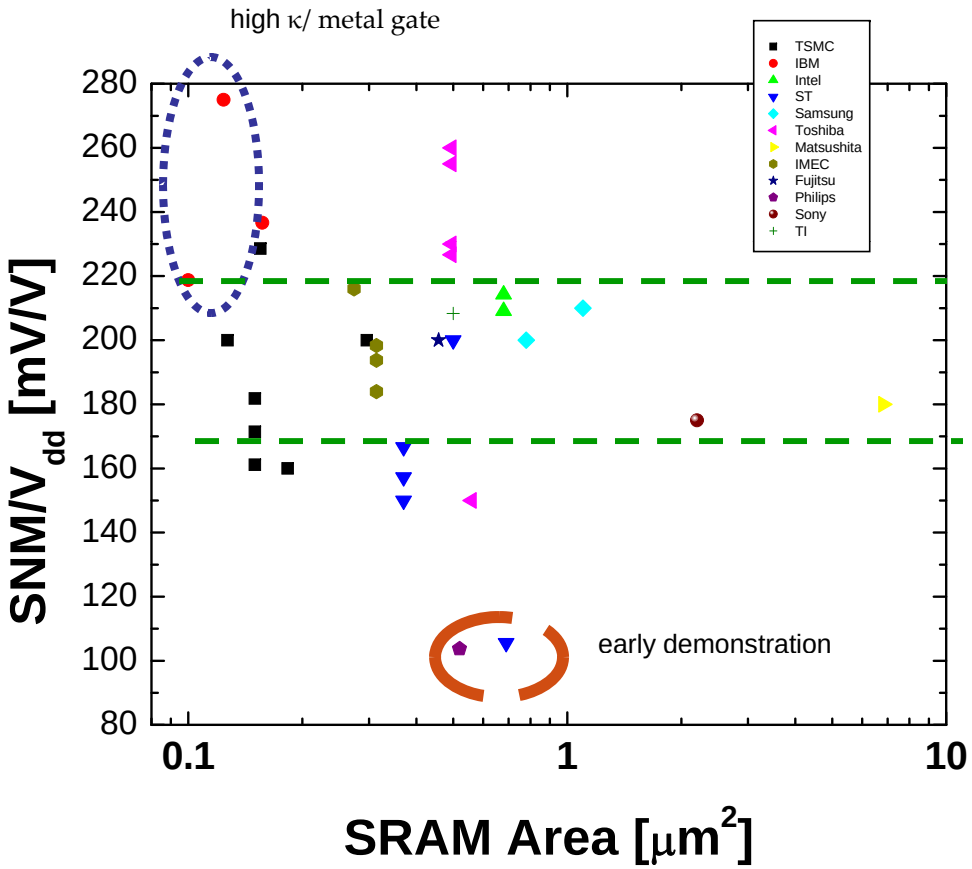
- Performance, cost, and form factor must be considered.
- Embedded memory:

1. SRAM
2. DRAM
3. Non-volatile

SRAM Trends

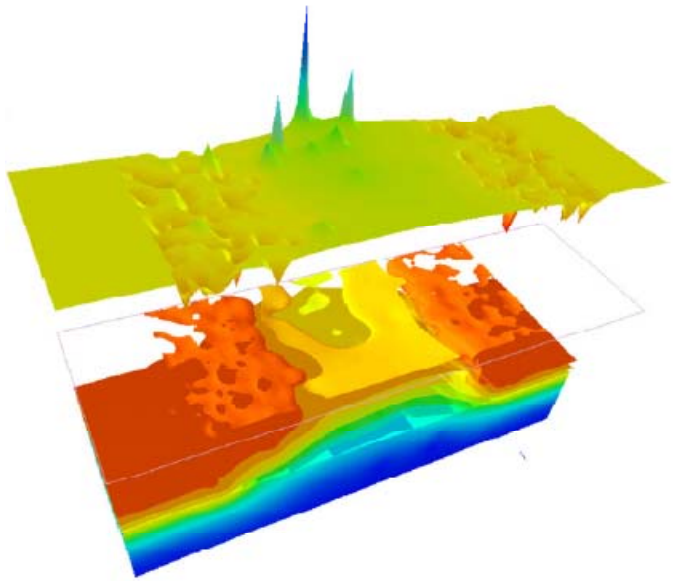


H.S.Yang et al, IEDM 2008



SRAM Long-term Challenges

1. Stability of SRAM cell. At which node will random dopant fluctuations require fully depleted devices?
2. RTN in small area. How perfect a dielectric can we make?

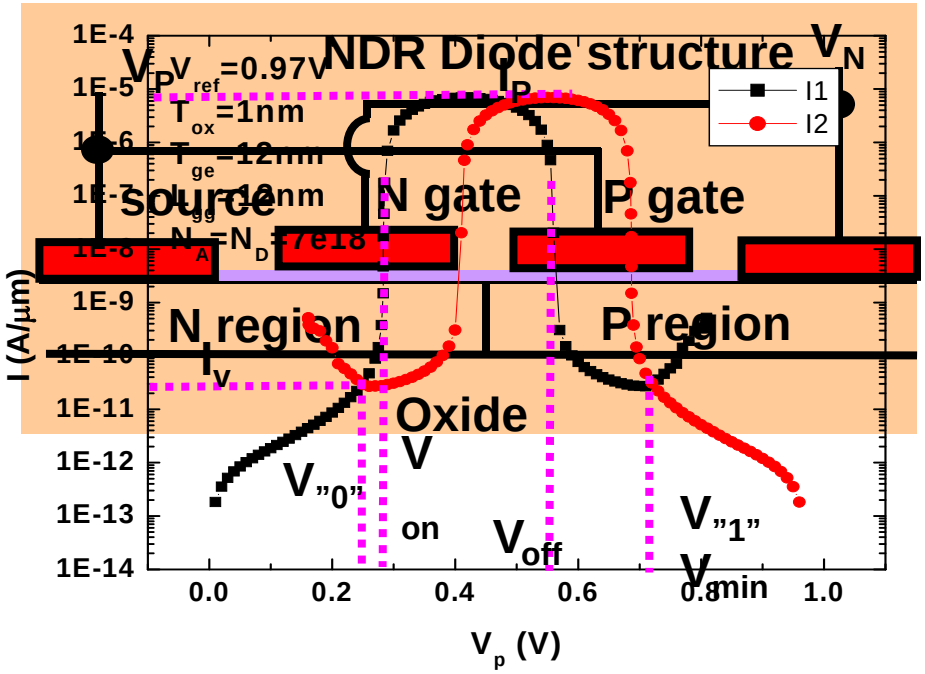


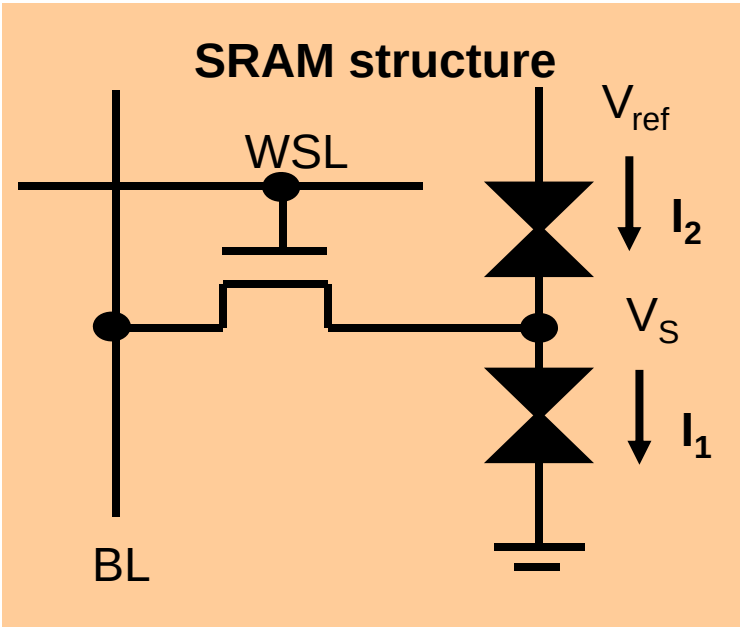
M.F. Bukhori et al, *Micr.Rel.*,**48**, p.1549

	6T	8T	4T	5T
Description	POR	Separate read/write path to improve cell stability	Data feedback with body bias of the pull down Tr.	Single ended bitline
Cell size (32nm)	0.157	0.2	0.11	0.133
Relative cell size	1	+ 28%	- 30%	- 15%

SRAM Based on Tunneling Devices

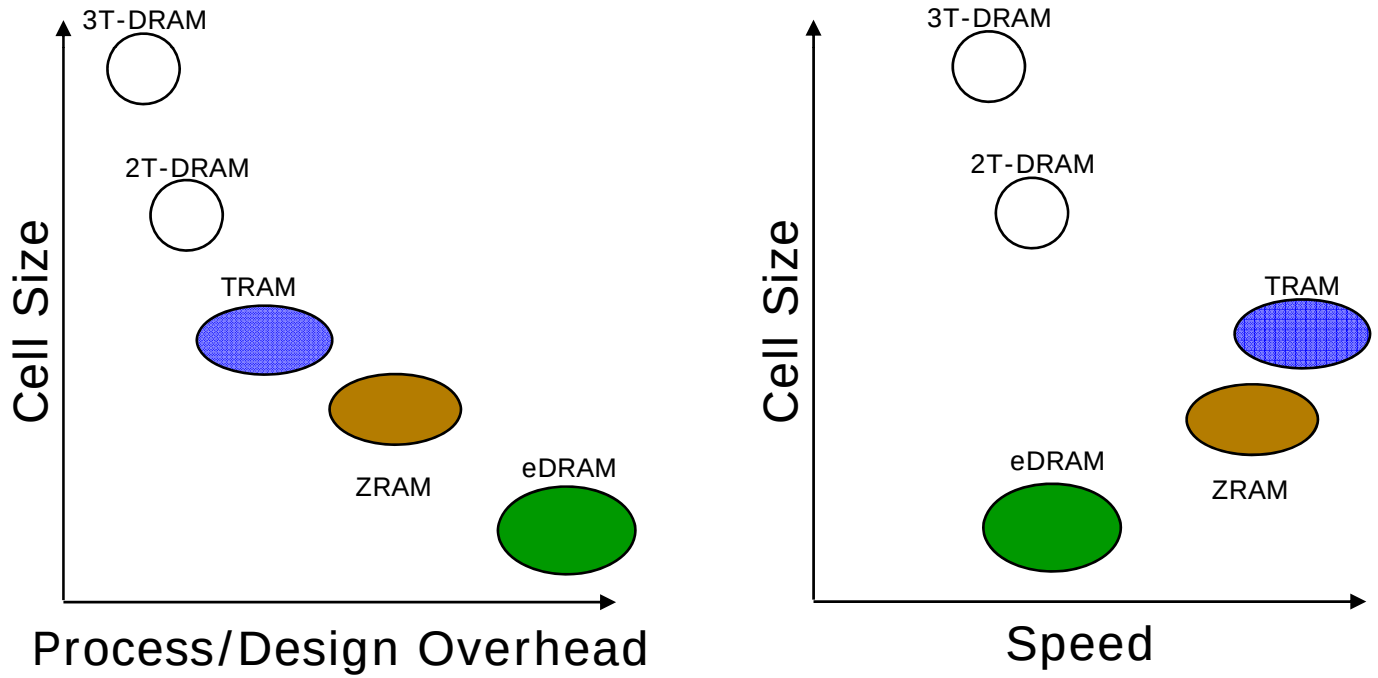
- SRAMs based on tunneling devices (various types of Goto cell) offer area savings.
- Valley current of the NDR device is critical to achieve low power operation.





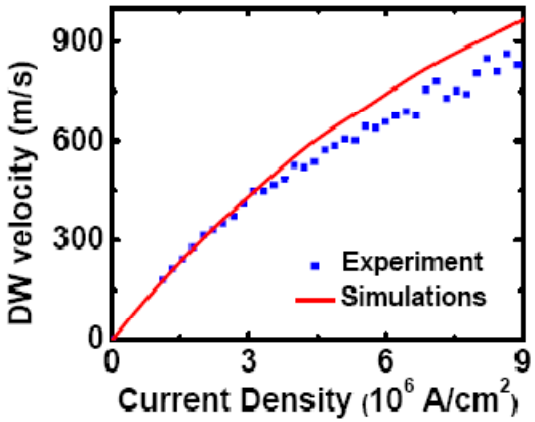
DRAM Solutions

- High performance DRAM solutions are limited by cost.
- Research on novel dynamic memory is important.



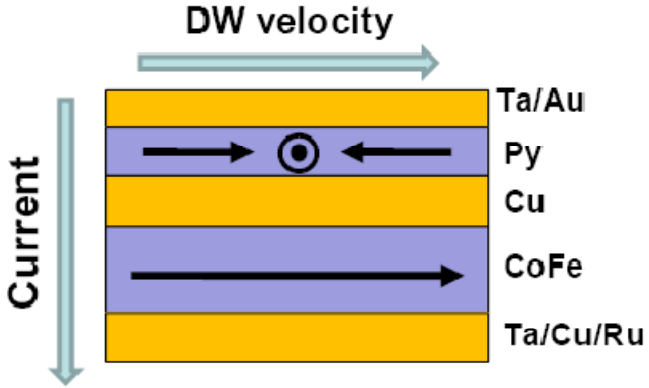
Embedded Non-volatile Memory

- Embedded flash is used for smaller memory sizes. Due to its large overhead operating voltages have to be reduced. Candidates are nanocrystal and SONOS memory.
- STT memory is an excellent candidate for embedded memory since its power scales inversely with geometrical scaling. Penta layer STT and perpendicular magnetization devices offer significant improvement and provide further research guidance.



Boone et al, arXiv 2009

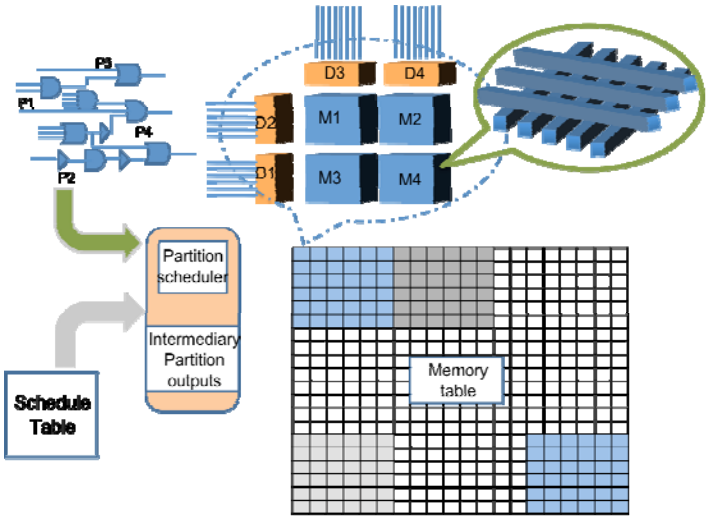
By using current flowing perpendicular to the ferromagnet domain wall velocity can be increased at smaller current densities.



Novel Architectures

Memory Based Architecture for Computing (MBARC) requires large amount of memory. (*Paul, S., Bhunia, S., "MBARC: A scalable memory based reconfigurable computing framework for nanoscale devices", ASPDAC '08)*

Logic truth table is stored in ultra-dense memory.



- LUTs and configuration written to memories during programming
- Controller programmed during synthesis
- Intermediate results are stored in local memory
- Overall computation completes when sequence of look ups finishes

Field-Programmable Gate