NV-Memory Elements with Gate-All-Around Transistors

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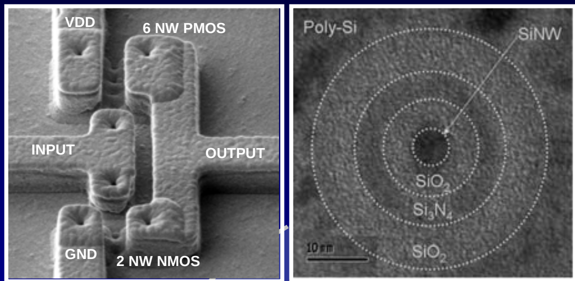
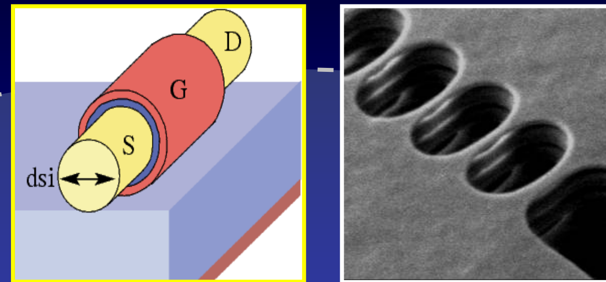
Outline

- **Motivation**
  - Si-Nanowire/-Pillar Platform – Application
  - Channel Control, Density, Performance
- **Integration Feasibility**
- **Examples of NV-Memory Devices**

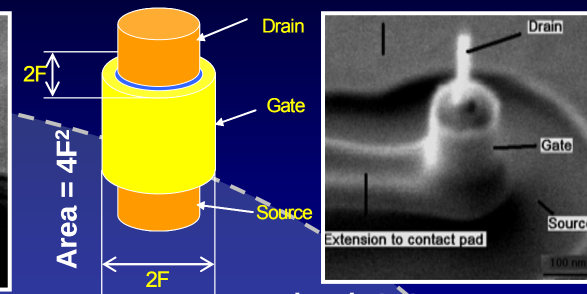
Nanowire/Pillar Technology Platform & Applications



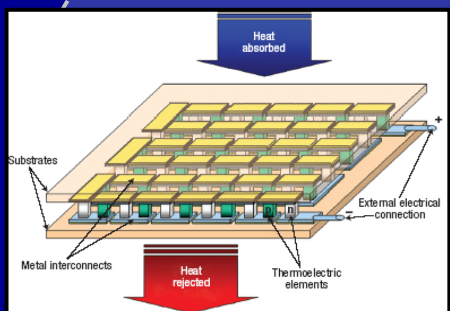
Low-Power Logic & High-Density NVM



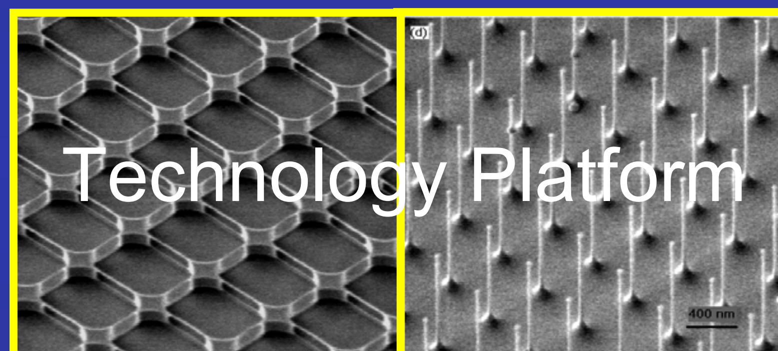
CMOS Devices Beyond 22nm

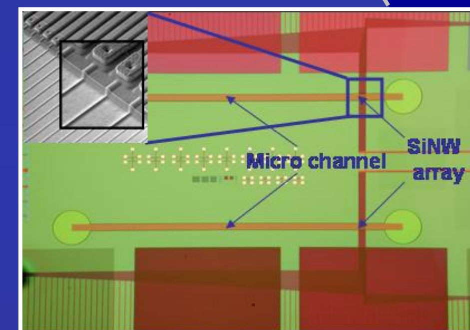


Vertical SGT, A new paradigm

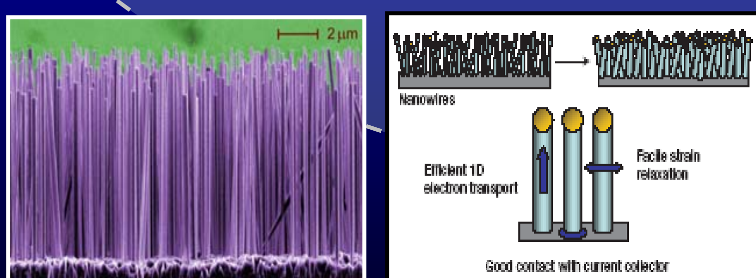


μ–Chip-NW-TEG, TEC

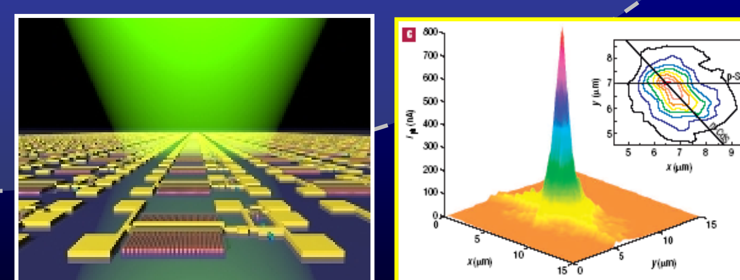




Biosensor Array with μ-fluidic channels



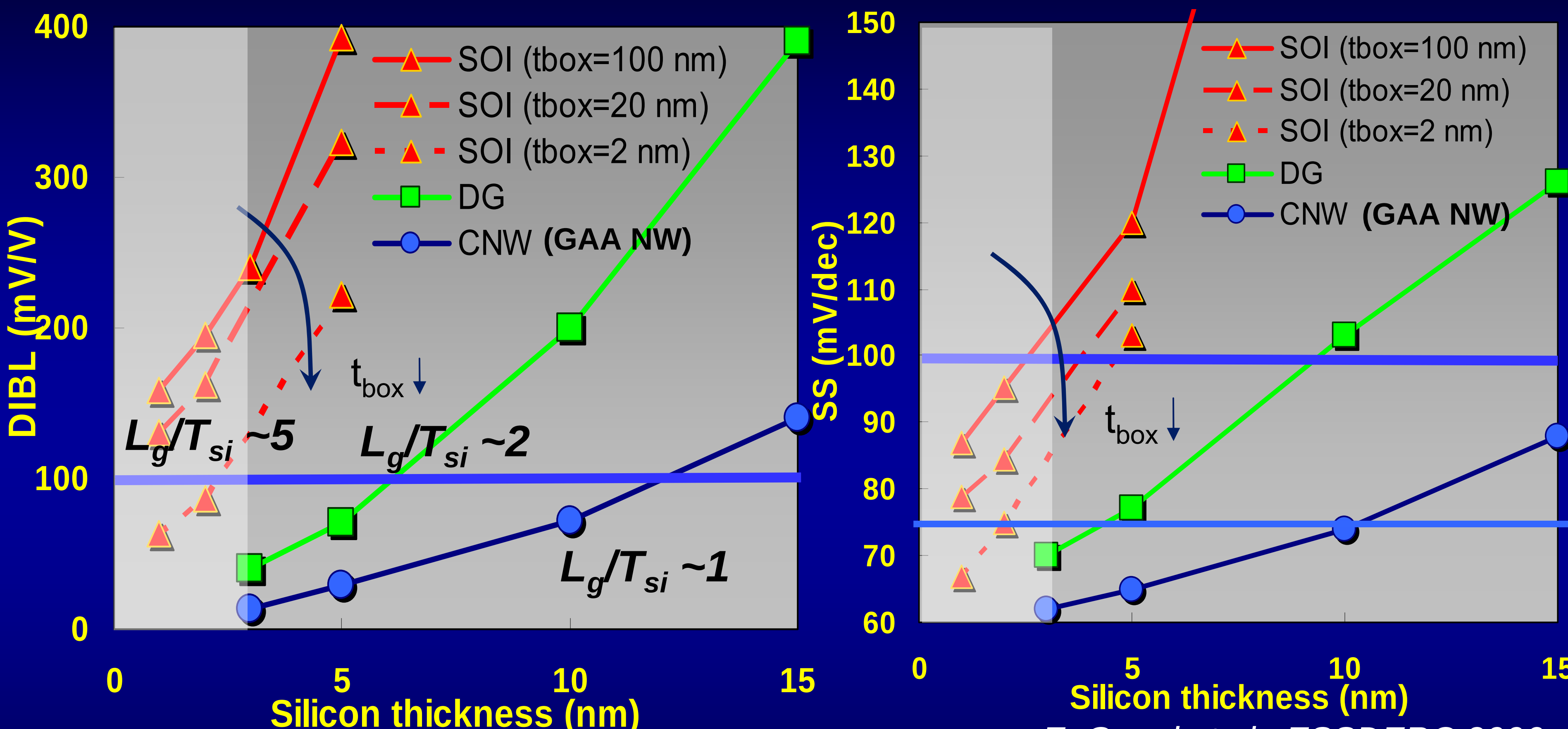
Integrated Energy Harvesting & Storage



Integrated OEIC Sensor Array

Gate-All-Around: a Candidate for Sub-22 nm Nodes

Electrostatics Analysis at L_G = 10 nm (EOT= 2 nm)

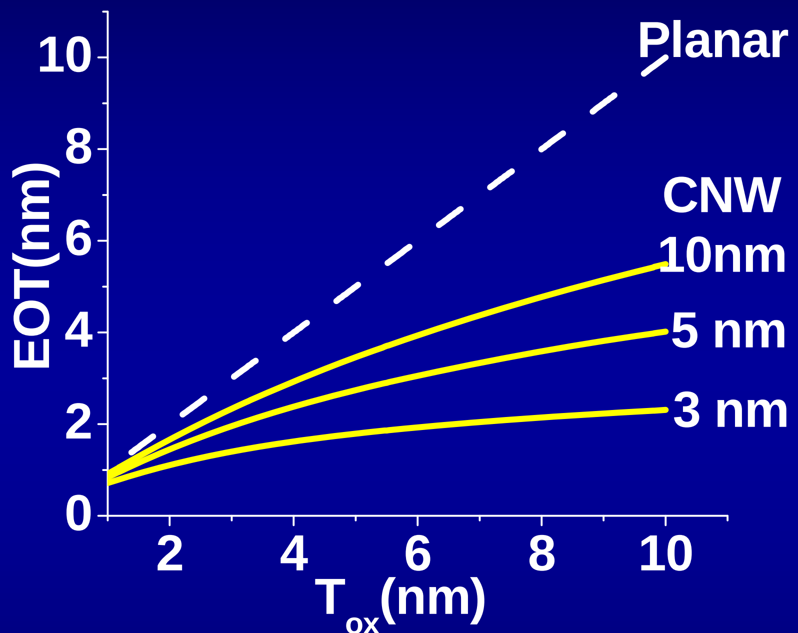


E. Gnani et al.; ESSDERC 2006

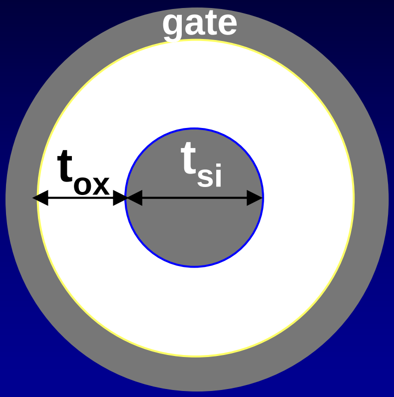
Only GAA nanowire fulfills the requirement of gate electrostatics with the condition that channel dimension ≤ L_G (L_G/T_{Si} ~1).

➔ *Devices can be scaled to sub-10 nm technology nodes!*

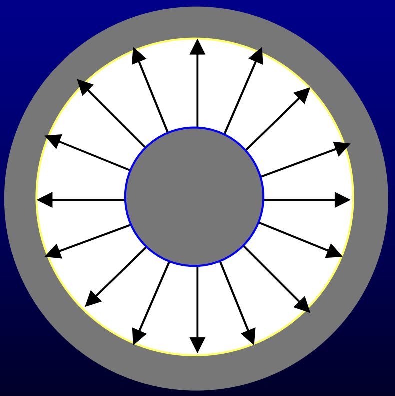
Effective Scaling of Gate Dielectric



$$C_{ox}(planar) = \frac{\varepsilon_{ox}}{t_{ox}},$$

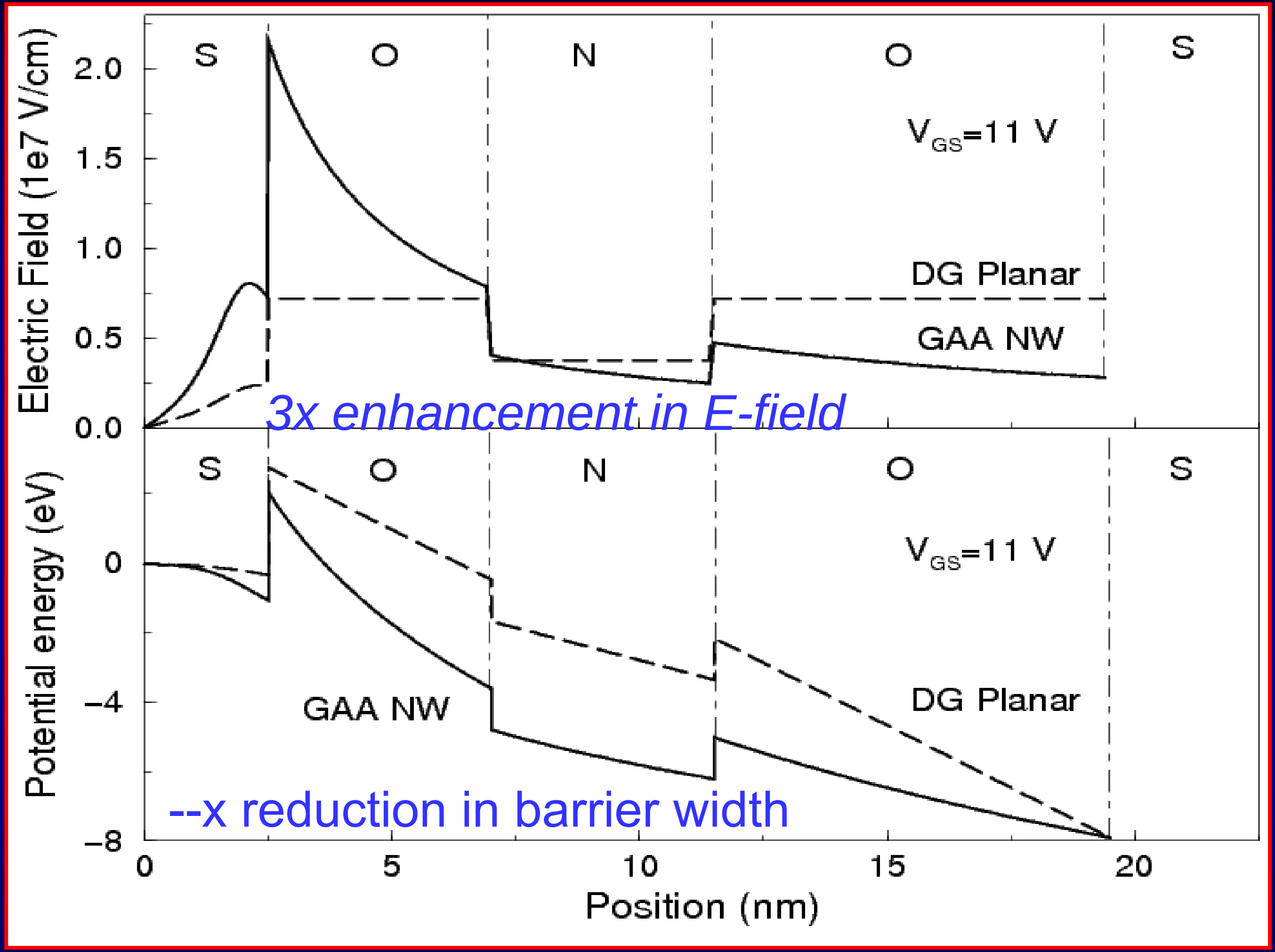


$$C_{ox}(GAA) = \frac{\varepsilon_{ox}}{\frac{t_{si}}{2}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}$$



- $T_{ox|Electrical}$ can be $<T_{ox|Physical}$;
- Reduction in EOT is possible by thinning the Si-body dimension.

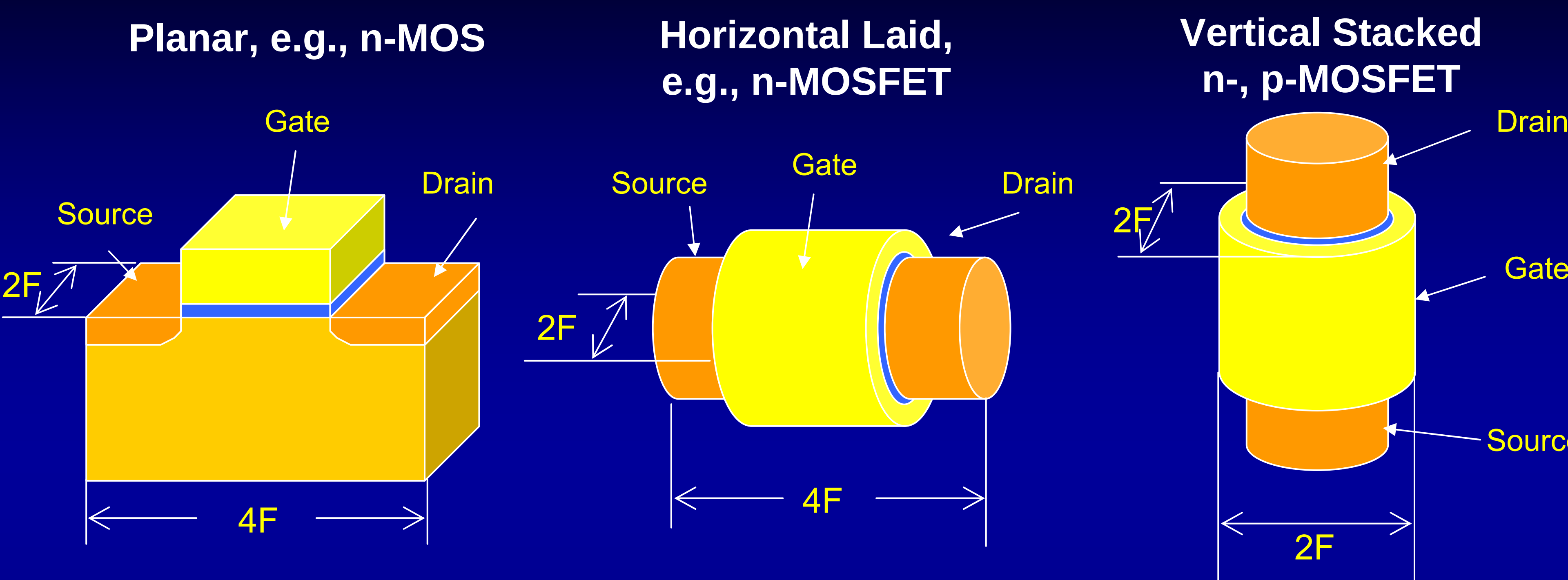
High E-Field in Tunnel Layer



(Collaboration: UOB)

Field Enhancement is achieved with Nano-Structure

More Fundamental Limitation and Implication



Area = $8F^2$ | **Area = $8F^2$** | **Area = $4F^2$**

F: Feature size

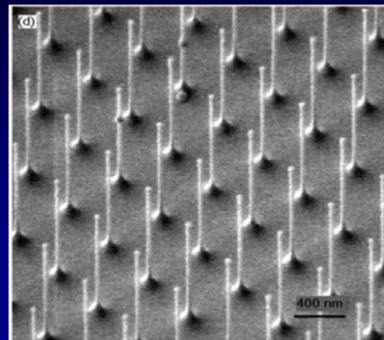
FUNDAMENTAL BENEFIT with VERTICAL SCHEME:

- Device area: Shrunk by ~50% from Planar

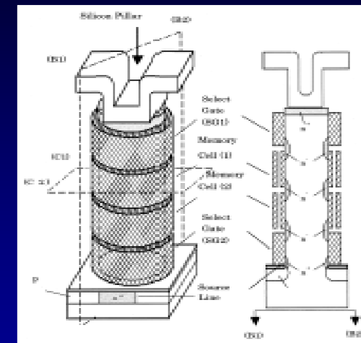
If consider n- and p-MOSFET together for circuit,

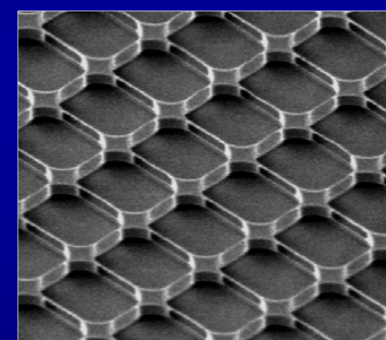
- Circuit area: Shrunk by >70%
- Speed: Improve by ~6.1x faster
- Power: Reduce by ~3.3x lower

High-Performance & High-Density NVM



[Vertically Stacked Cells]



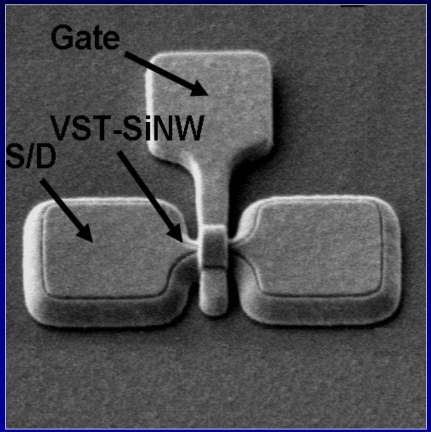


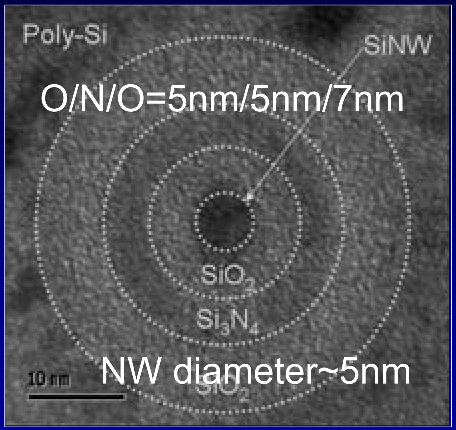
[Gate-All-Around; nm-scale wire]

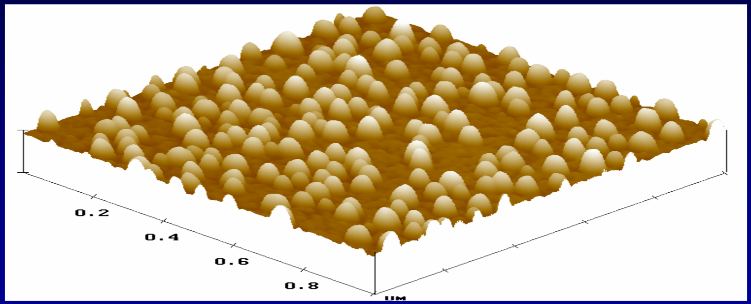
Vertical Multi-Cell Integration on

Performance via Nano-Structure

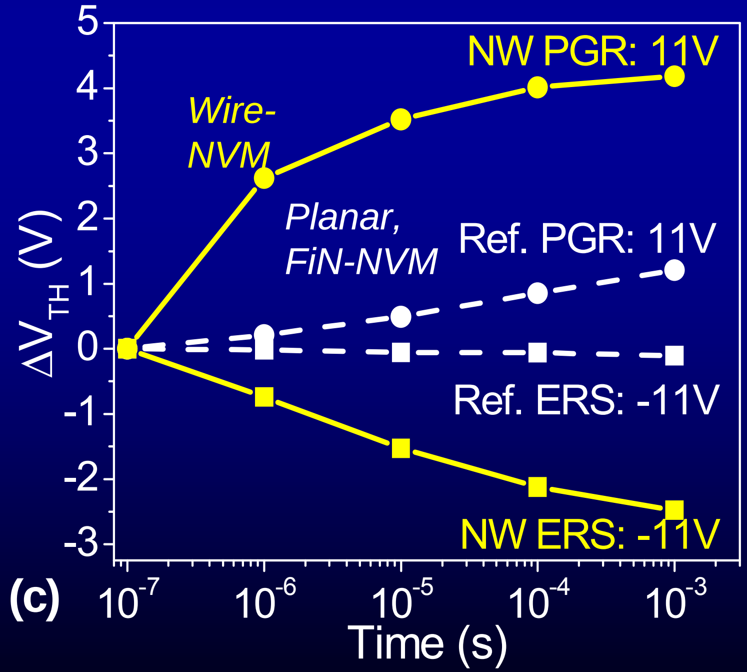
NV-Memory Device Performance (Horizontal)

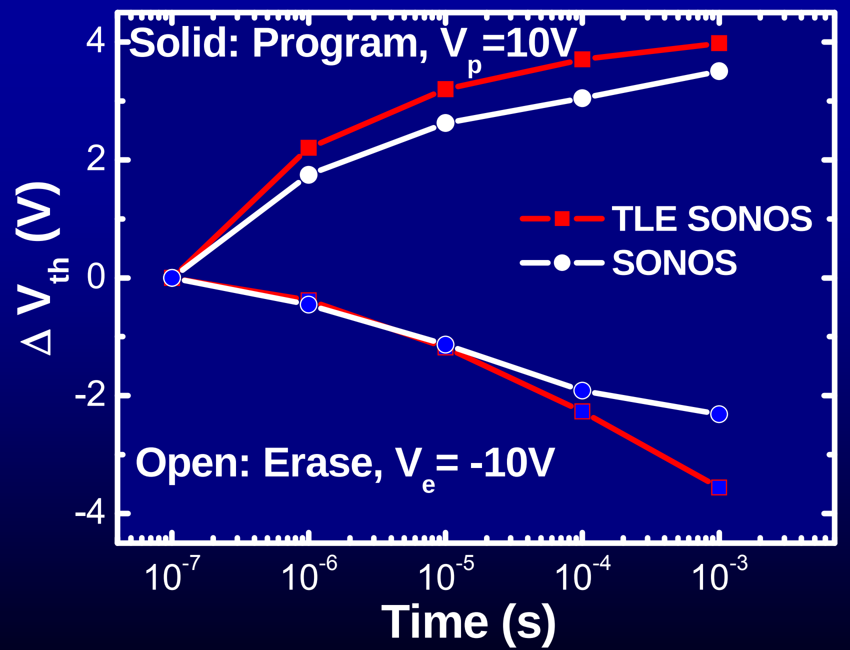




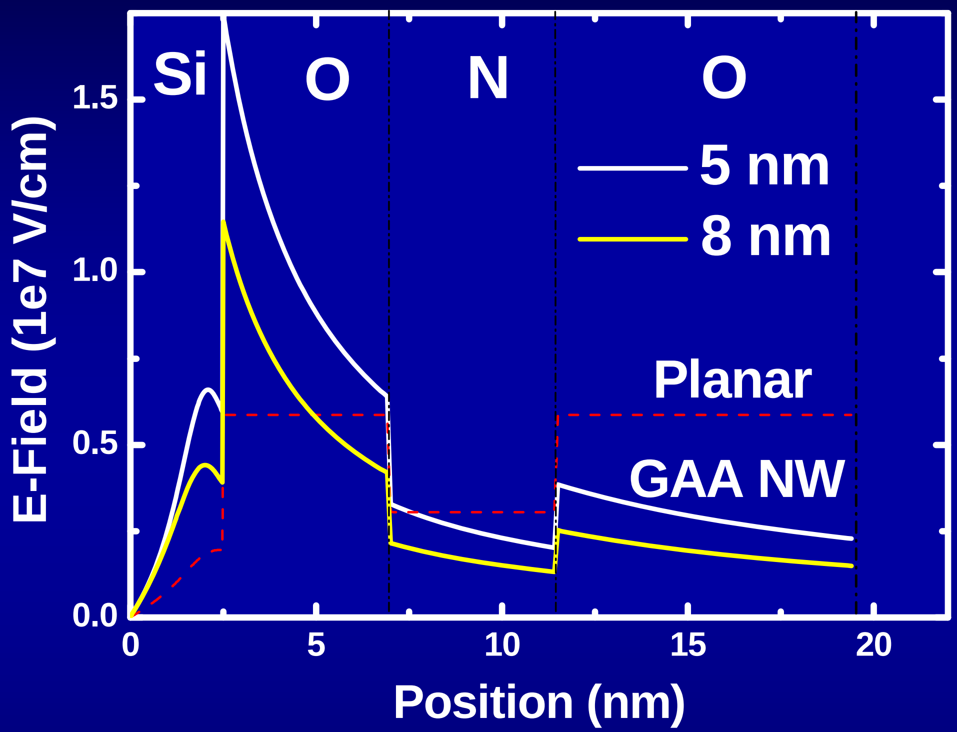


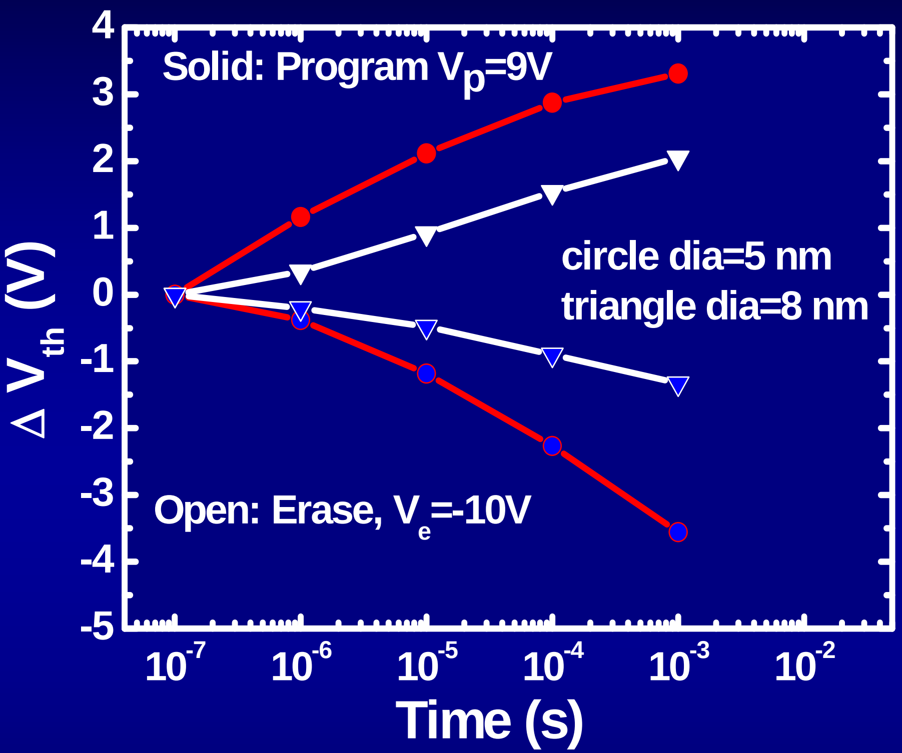
Si-Nano-Crystals on Si_3N_4: 7.5×10^9 cm^{-2}





Wire Diameter Impact

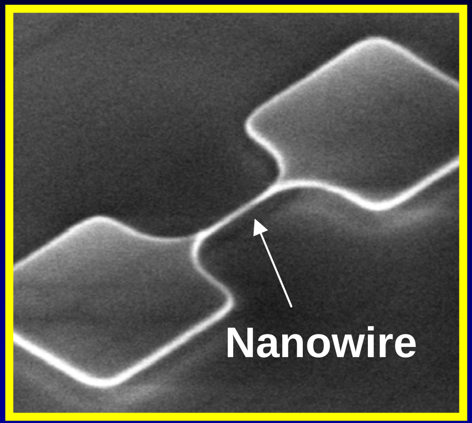


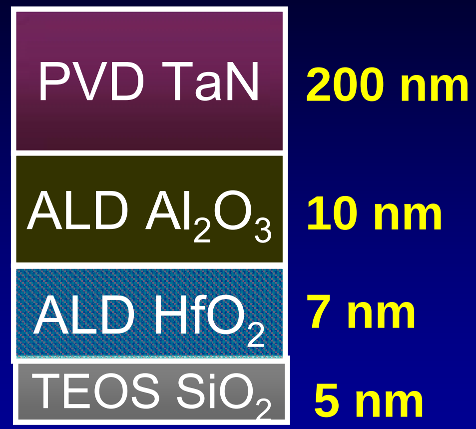


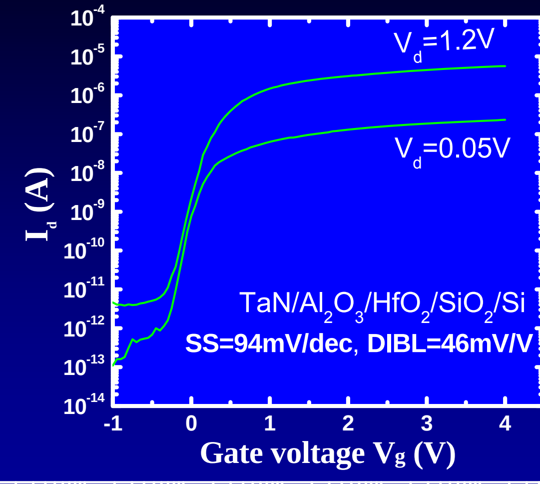
(Collaboration: UOB)

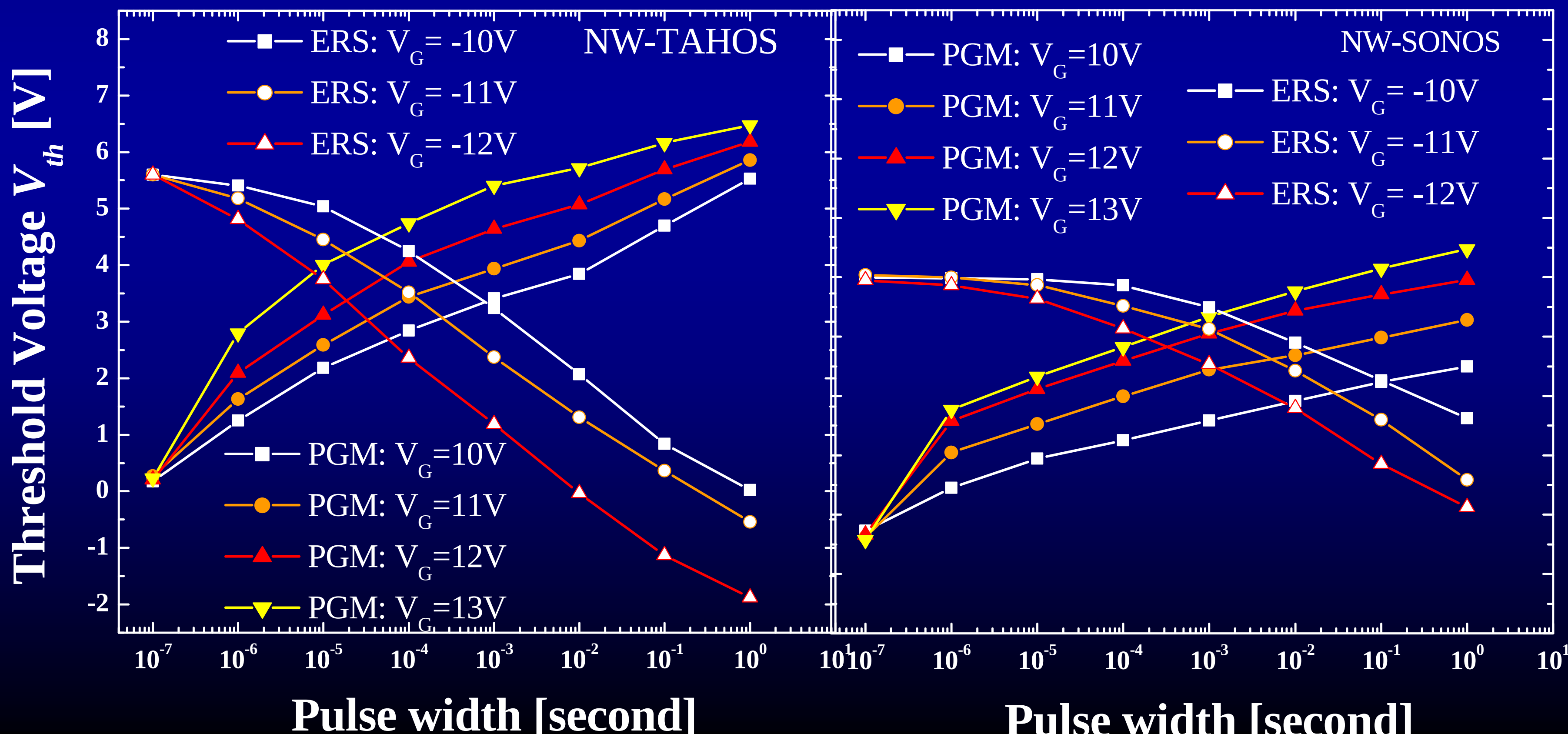
Field can be simply increased with narrower-diameter to Improve the P/E performance

Impact of High-κ Storage



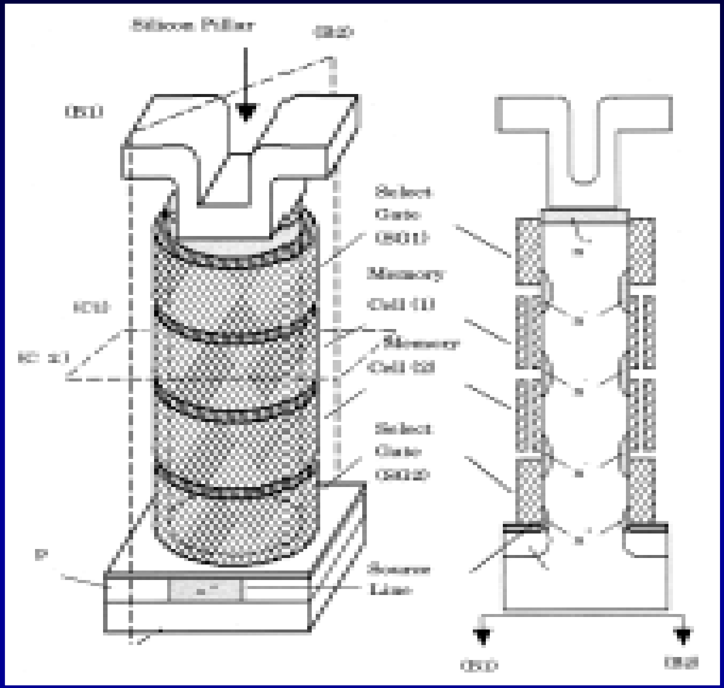


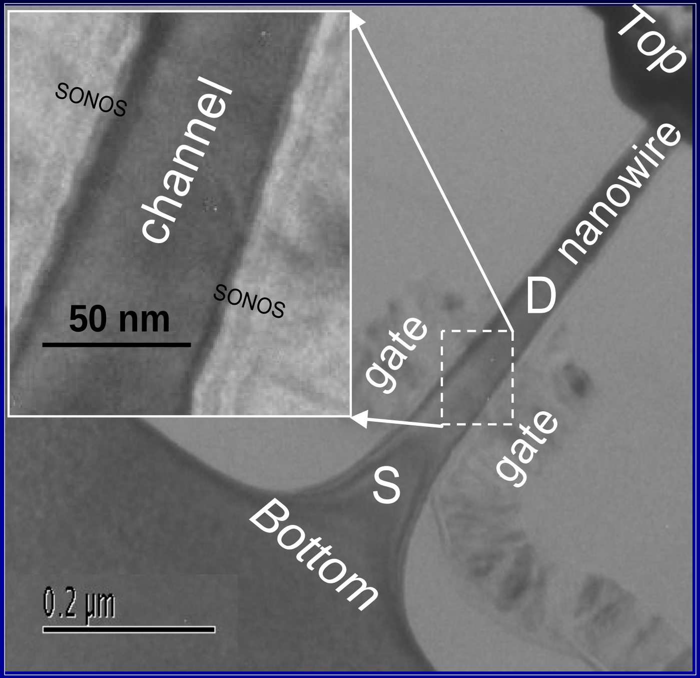




Vertical Pillar based SONOS NVM

[Tohoku Univ./TED '05]





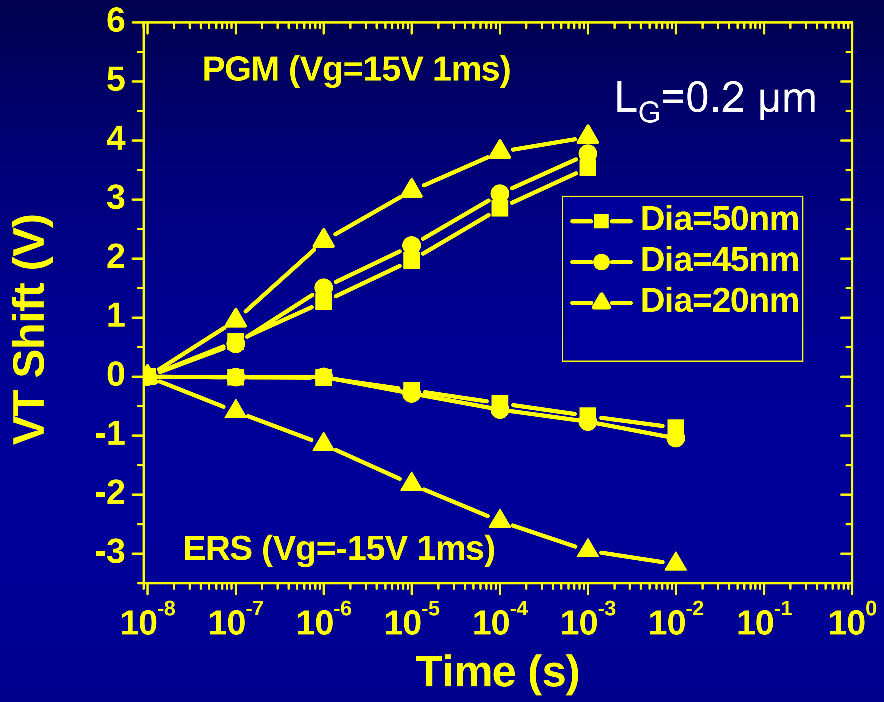
Objective:

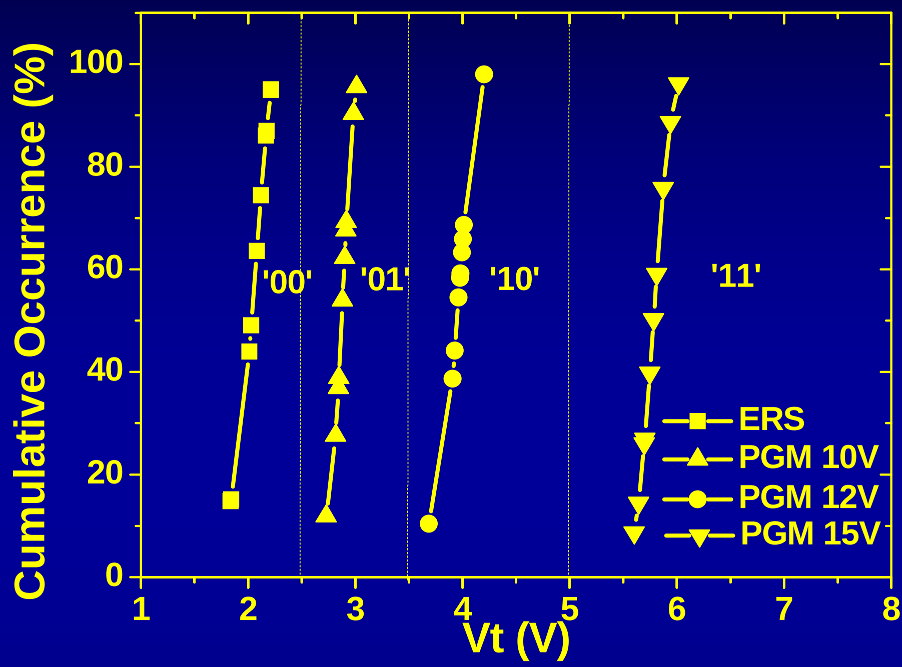
- Develop scalable high-density and high performance memory devices

Approaches:

- Multi-cells implementation on single Pillar Vertically
- P/E field-enhancement via Surrounded Gate on nano-pillar

Multi-bit Programmable SONOS NVM on Pillar





- P/E speed Improvement with reduced diameter (50 → 20nm),
- Well distributed Programming V_t: 2-bit storage/Cell Possible,
- Good retention and Endurance.