Physics of Double and Single Barrier Tunneling and Their Impacts on Semiconductor Memories

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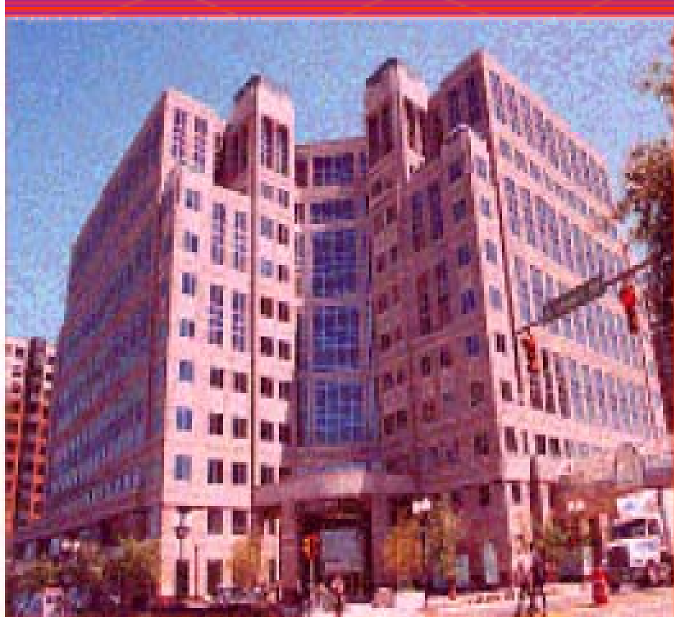
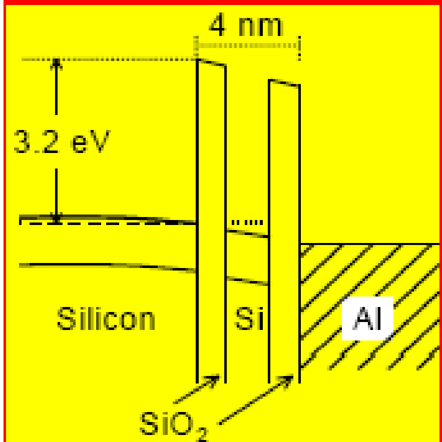
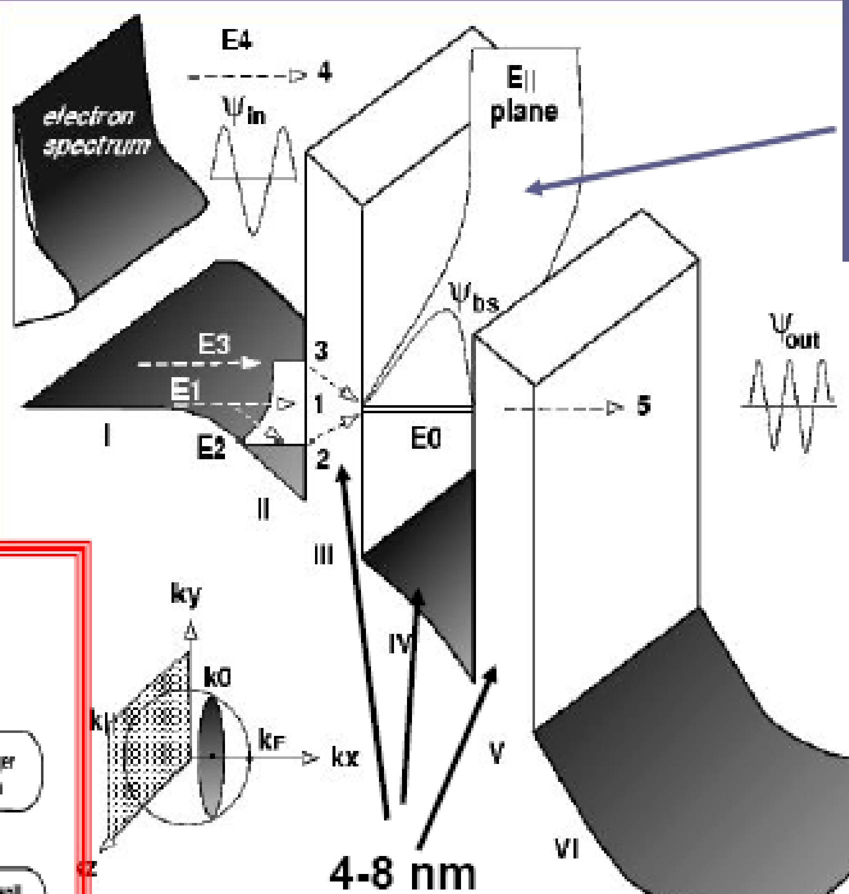


TOPIC #I

Bey... -a Compatible & Viable Solution:

Physics behind DB Quantum Tunneling





Time-independent effective mass Schrodinger Equation

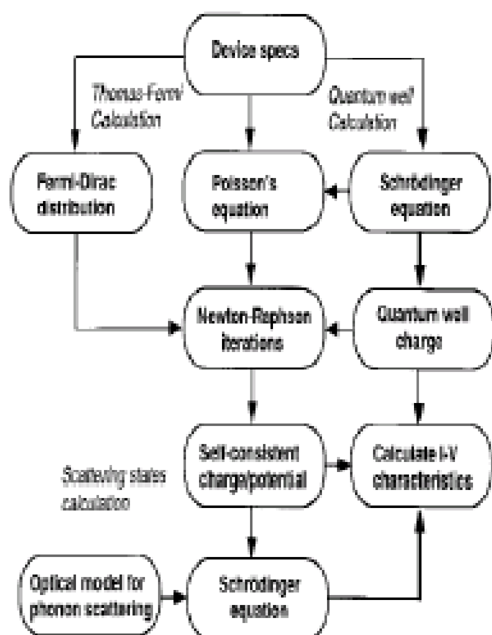
$$\left[-\frac{\hbar^2}{2}\nabla\left(\frac{1}{m^*}\nabla\right)+V(\vec{r})\right]\psi_n(\vec{r}) = \left[E(\vec{k})-E_n(0)\right]\psi_n(\vec{r})$$

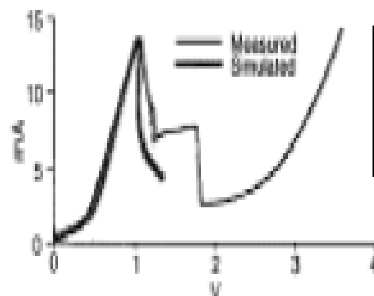
Device Current Density:

$$J_{tot} = -q\hbar\sum_k W(k)\cdot \mathrm{Im}\left[\psi_k^*(x)\frac{1}{m^*(x)}\frac{\partial\psi_k(x)}{\partial x}\right]\Delta k$$

$$J_{tot} = \frac{q m^* k_B T}{2\pi^2\hbar^3}\int_{E_c}^{\infty} T(E_x)\cdot \log\left[\frac{1+\exp\left(\frac{E_F-E_x}{k_B T}\right)}{1+\exp\left(\frac{E_F-E_x-qV_A}{k_B T}\right)}\right]dE_x$$

$$T(E) = \frac{\left(\frac{\Gamma}{2}\right)^2}{\left[E-(E_r-eV/2)\right]^2+\left(\frac{\Gamma}{2}\right)^2}$$





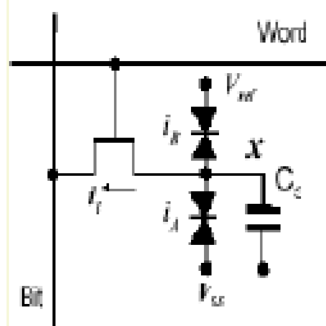
Recipe Contest for Si-based RTDs / TDs

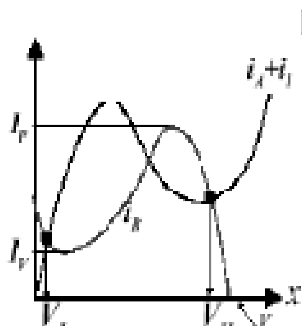
Self-consistent Poisson-Schrodinger Eqns. Solver Developed

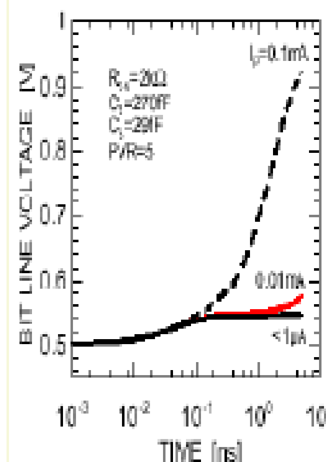
Proceedings of IEEE, Apr. 98,

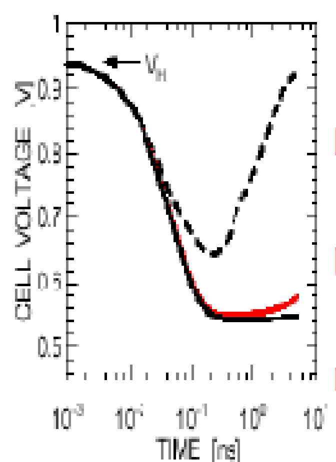
DARPA Ultra Program

Analysis of TSRAM Circuit







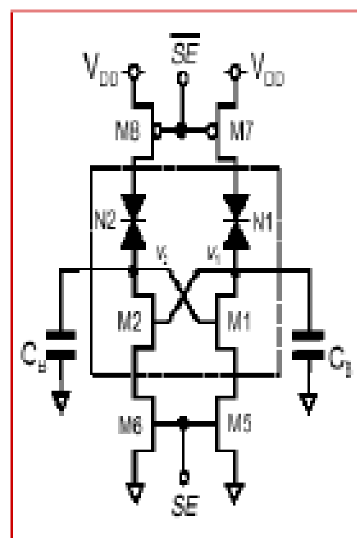


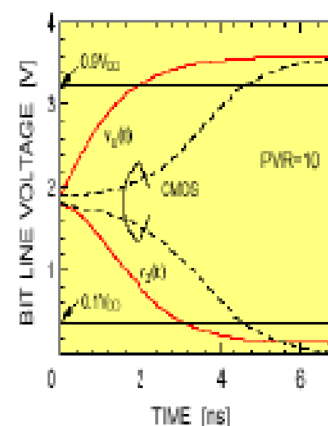
- Analysis of TSRAM (van der Wagt *et. al.* IEDM 96) for:
  - Standby
  - Read/Write
  - Stability
  - Access time
  - Power
- No periodic refresh required
- Reduced stand-by power
- Reduction in cell storage capacitor

Refresh Current	Conventional	Auto Refresh	UMckt1	TSRAM	TSRAMJMckt2
	3.6 pA	115 fA	44 fA	$50/k_1$ fA	$19/k_2$ fA

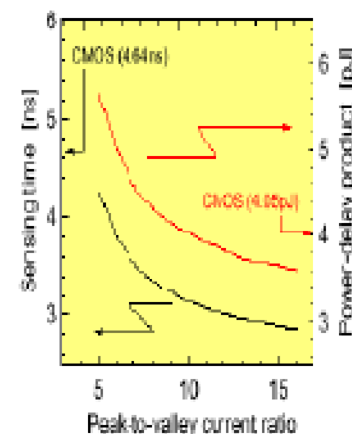
$$\eta = \frac{P_{\mathrm{TRAM}}^{\mathrm{Avg}}}{P_{\mathrm{DRAM}}} = \frac{\left(\frac{1}{\delta} + \frac{1}{\mathrm{PVCR}-1}\right)}{\delta \cdot \left(1+\frac{C_{\mathrm{bit}}}{C_0}\right) \cdot \frac{1}{1-\frac{C_{\mathrm{bit}}}{C_0}\frac{2V_T}{V_{DD}-2V_T}}},$$

QMOS Sense Amplifier





- 31% higher sensing speed than CMOS (@PVR=10)
- Lower power-delay product (@PVR>10)
- Smaller area



T. Ueymura and P. Mazumder, "Design and Analysis of Resonant-Tunneling-Diode (RTD) Based High Performance Memory System," *IEICE Trans. on Electronics* Vol. E82-C, No. 9, Sept. 1999.

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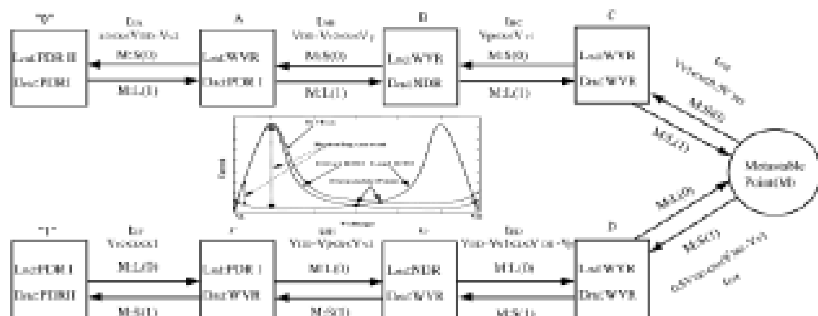
TUNNELING RANDOM-ACCESS MEMORY OPERATION MICROSTATES

TABLE I
PARAMETERS FOR WRITE "1" OPERATION

	State Transition			
	'0'→'A'	'A'→'B'	'B'→'C'	'C'→'M'
a'	[illegible]	[illegible]	[illegible]	[illegible]
b'	[illegible]	[illegible]	[illegible]	[illegible]

TABLE II
PARAMETERS FOR WRITE "0" OPERATION

State Transition			
'1'→'F'	'F'→'E'	'E'→'D'	'D'→'M'
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]



COMPARISON OF QC FOR TRAM & DRAM

H. Zhang, P. Mazumder, L. Ding, and K. Yang, "Performance Modeling of Resonant Tunneling Based Random Access Memories," *IEEE Transactions on Nanotechnology*, July 2005, pp. 472-480.

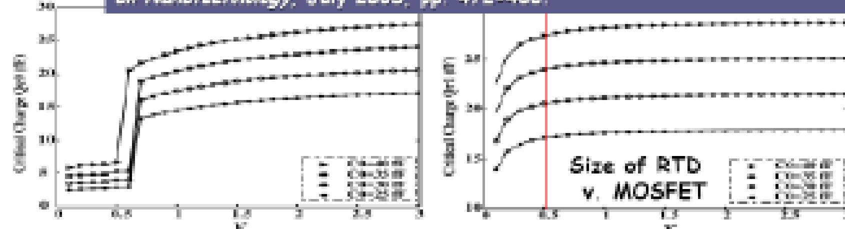


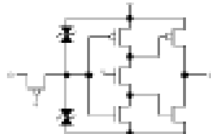
TABLE III
CRITICAL CHARGE COMPARISON OF TRAM AND CONVENTIONAL DRAM

150%-- 200% SER Improvement

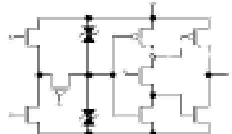
	DRAM Q_C (fC)									TRAM Q_C (fC)						
C_{bit} (fF)	150			200			250			Q_{1} (fC)			Q_{0} (fC)			Q_{a} (fC)
C_B (fF)	ΔV_{SEN} (mV)			ΔV_{SEN} (mV)			ΔV_{SEN} (mV)			ΔV_{SEN} (mV)			ΔV_{SEN} (mV)			
	50	60	70	50	60	70	50	60	70	50	60	70	50	60	70	
25	11.3	9.5	7.8	8.8	6.5	4.3	6.3	3.5	0.8	17.1	17.0	17.0	14.4	14.4	14.5	17.8
30	15.0	13.2	11.4	12.5	10.2	7.9	10.0	7.2	4.4	20.5	20.5	20.4	17.2	17.3	17.3	21.4
35	18.8	16.9	15.1	16.3	13.9	11.6	13.8	10.9	8.1	24.0	23.9	23.8	20.1	20.1	20.2	24.9
40	22.5	20.6	18.7	20.0	17.6	15.2	17.5	14.6	11.7	27.4	27.3	27.2	22.9	23.0	23.1	28.3

QMOS Edge Triggered Flip-Flop Circuits

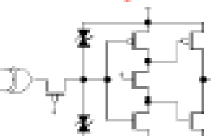
Positive Edge DFF



Positive Edge SRFF



Positive Edge TFF

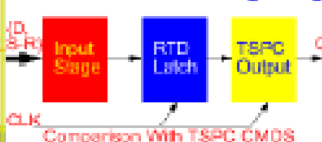


S. Kulkarni and P. Mazumder, "Edge Triggered Flip-Flop Circuit Based on Resonant-Tunneling Diodes and MOSFET's," *European Conference on Circuits: Theory and Design*, Aug. 2001.

US Patent No. 6,323,709

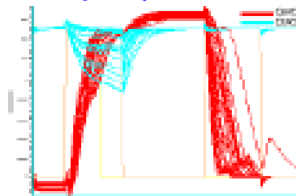
Key Features

QMOS Edge Triggered Flip-Flops



Comparison With TSPC CMOS

0.35 µm	CMOS	QMOS
Area (normalized)	1	0.75
Setup time (ns)	0.1	0.06
Hold time (ns)	0.2	0.09
Rise time (ns)	0.2	0.09
Fall time (ns)	0.12	0.06
Max Speed (GHz)	2.6	6.6
Power (µW)	129	34
Power-delay (fJ)	81	17

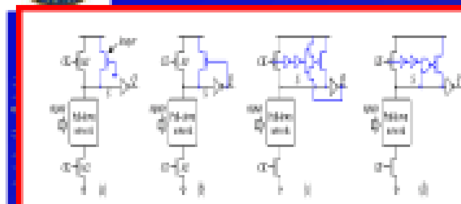


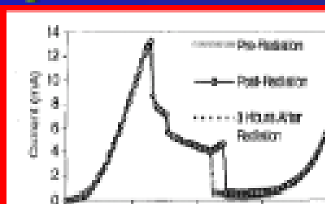
Key Features

- Smaller circuit and routing area
- Lower voltage operation possible with QMOS than purely CMOS, i.e. reduced power dissipation
- QMOS uses an RTD latch for storage unlike dynamic storage in TSPC CMOS implying better noise immunity

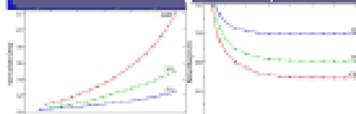
Improvement of Speed (x2.7) and Noise Margin (x300%) of True Single Phase Clocked (TSPC) Flip-Flop.

CMOS Rad-Hard and Noise-Resistant Domino Logic Circuits



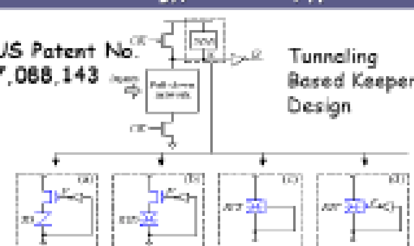


L. Ding and P. Mazumder, "Noise-Tolerant Quantum MOS Circuits Using Resonant Tunneling Devices," *IEEE Trans. on Nanotechnology*, Mar. 2004, pp. 134-146.



L. Ding and P. Mazumder, "On Circuit techniques to Improve Noise Immunity of CMOS Dynamic Logic," *IEEE Trans. on VLSI Systems*, Vol. 12, No. 9, pp. 910-25, Sept. 2004.

US Patent No. 7,088,143



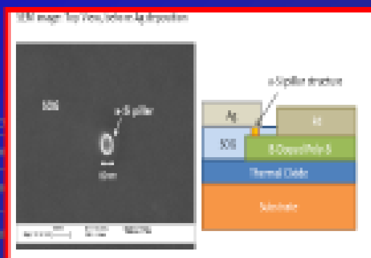
TOPIC #2

Single Barrier Tunneling

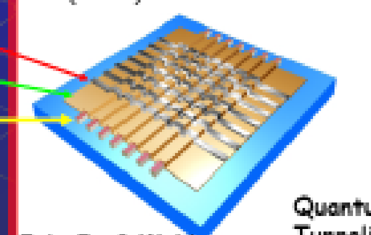
The device consists of Ag/a-Si/p+doped Si switches,

Low Resistance State

High Resistance State



Thin-film Metal-Insulator-Metal (MIM) nanostructures



Fab: Prof. Wei Lu

Quantum Tunneling Thru Single Barrier

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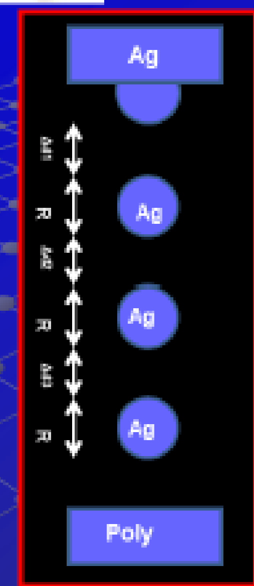
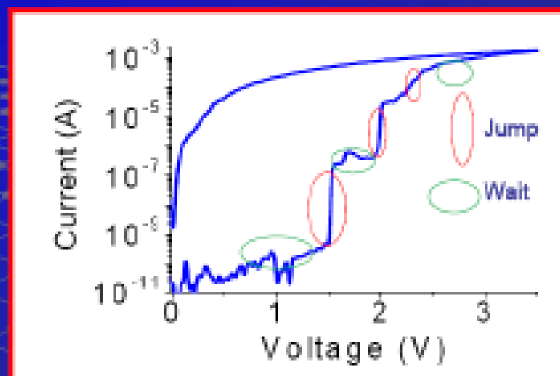
UNRAVELLING THE IONIC TRANSPORT AT NANOSCALE





$T(\Delta E) = e^{-2\gamma} = e^{-(2\sqrt{2m^*\Delta E}/\hbar)d}$ = Transmission Prob.

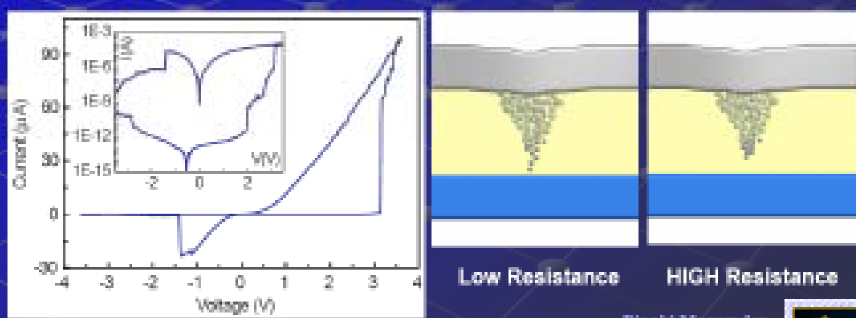
$$J(V) = \frac{qm^*}{2\pi^2\hbar^3}\int_0^\infty [f(E) - f(E+qV)]dE \times T(\Delta E)$$

$$\propto (D.O.S.) \times T(\Delta E) \times \ln[\frac{1+\exp(E_F - E)/kT}{1+\exp(E_F - E - qV)/kT}]$$

$$\text{if } V = 3.0V \Rightarrow t = \sqrt{\frac{2m_{Ag}\Delta d^2}{qV}} \equiv 7.1ps << \text{dwell time}$$

Switching Behavior

- Conventional M/a-Si/M devices require high voltage (>15V) forming process
- No necessity of high voltage forming process for M/a-Si/p-Si device
- Very high device yield (~ 99%)
- The switching is very sharp and high
- On/Off ratio R_{off}/R_{on} ~ 10^3 ~ 10^7



Typical switching behavior of 50x50 nm² device

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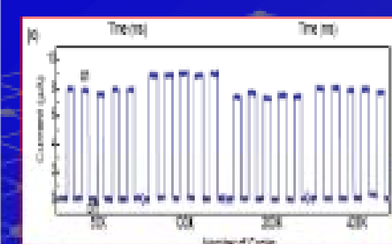
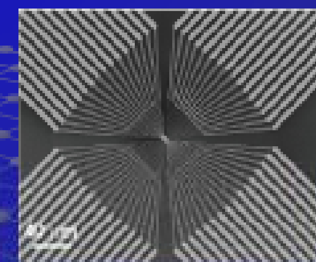
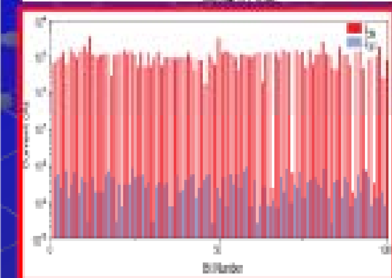
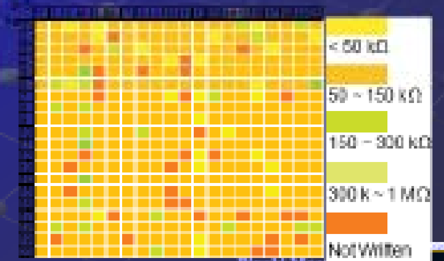
High Density a-Si Based Nano-Crossbar





1kb crossbar array fabbed at the UoM





Collaboration: Prof. Wei Lu

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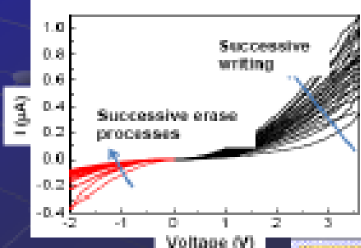
Analog a-Si Memristors

- Uniform motion of the conducting front – analog switching (memristor)
- Creation of uniform conducting front by co-sputtering of a-Si & metal

sputtered a-Si only
co-sputtered Si & Ag (~ 20nm)
mixture ratio (rough # of atoms), gradual change
i.e. Si : Ag = 20: 1 (bottom) ⟶ 10: 1 (top)
sputtered a-Si only

DARPA SyNAPSE PROJECT WITH HRL LABORATORIES



- Incremental conductance change
- Conductance ∝ total charge through the device

- Highest process temperature < 260°C

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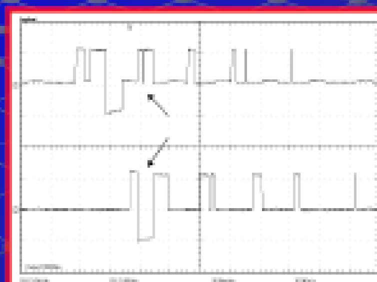
Spike Timing Dependence

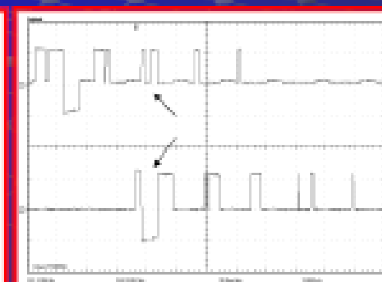
Post Neuron Spikes then Pre Neuron Spikes (LTD)

One Frame Afterwards



Longer duration across synapse

Two Frames Afterwards



Shorter duration across synapse

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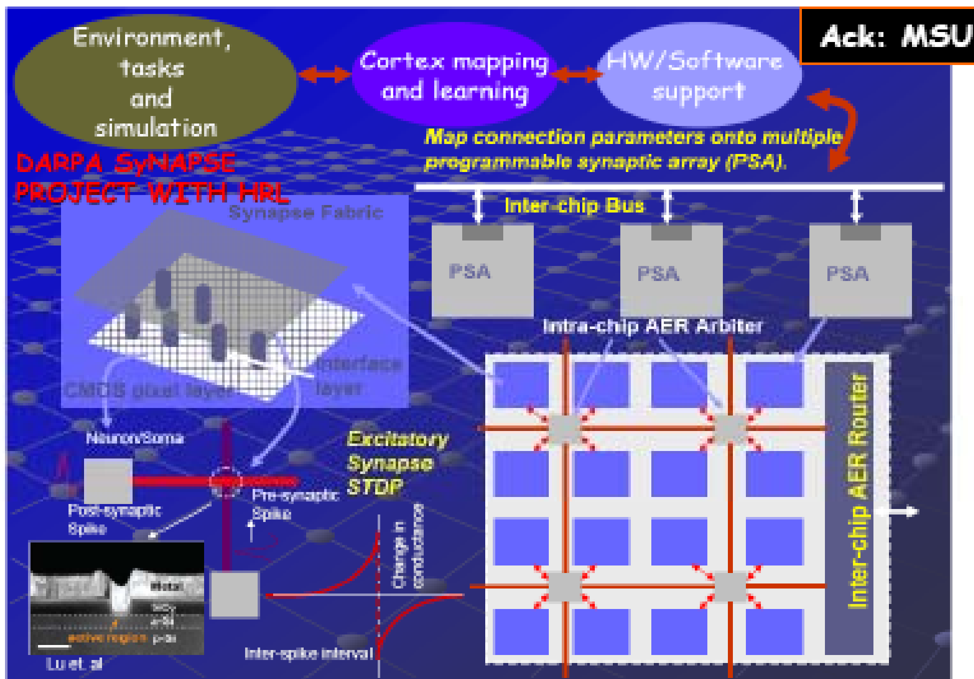
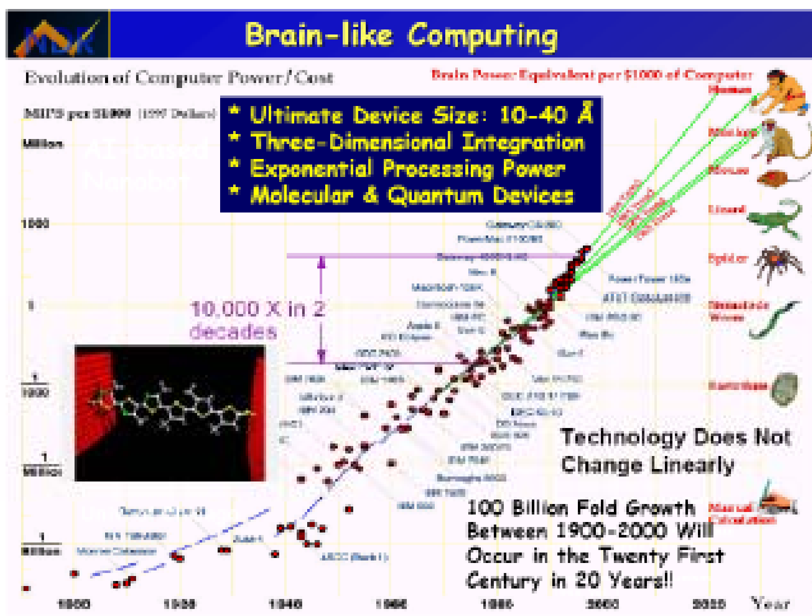
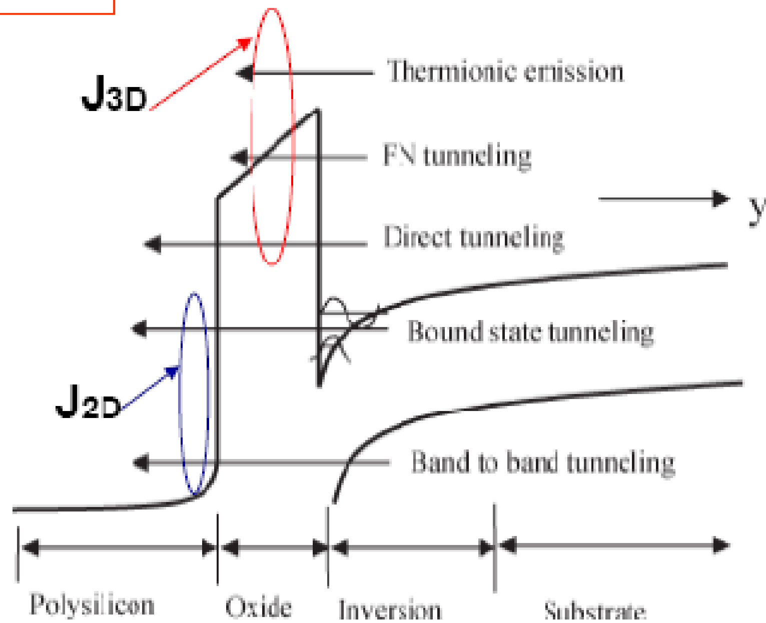


Brain-like Computing



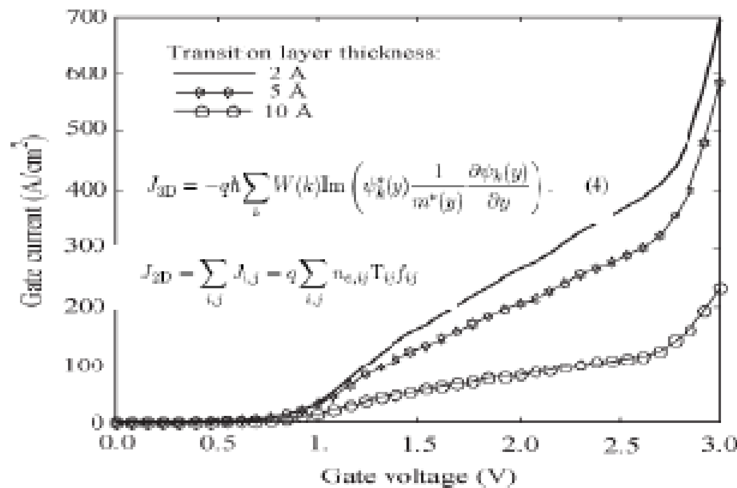
TOPIC #3

High K Dielectric Material Study for FETs and NV Flash



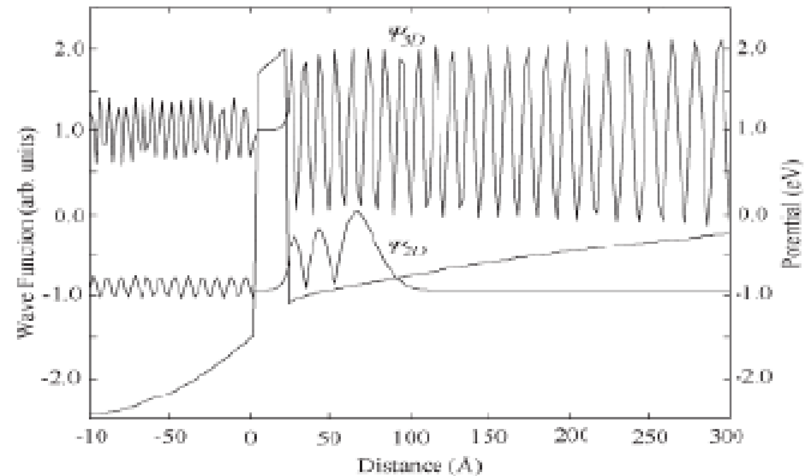
$$\frac{\partial^2 V(y)}{\partial y^2} = -\frac{q}{\varepsilon(y)}[N_D(y) - N_A(y) - n(y) + p(y)] \quad (1)$$

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m^*(y)}\frac{\partial \psi(y)}{\partial y}\right) + E_C(y)\psi(y) = E\psi(y). \quad (2)$$

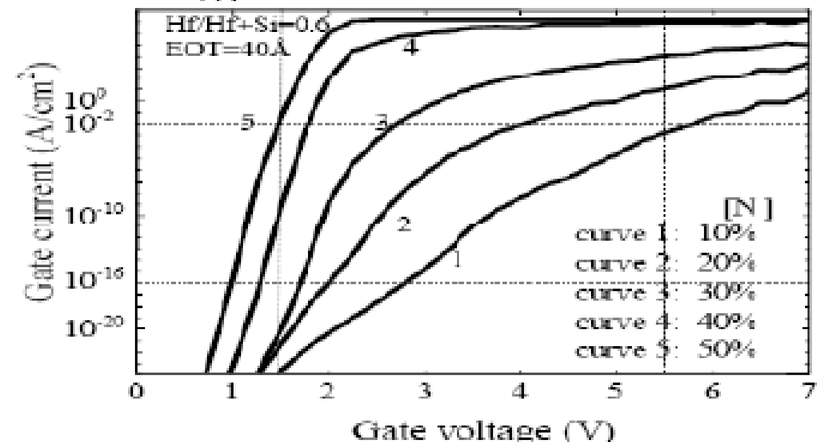


$$J_{3D} = -q\hbar \sum_k W(k) \mathrm{Im}\left(\psi_k^*(y)\frac{1}{m^*(y)}\frac{\partial \psi_k(y)}{\partial y}\right) \quad (4)$$

$$J_{2D} = \sum_{i,j} J_{i,j} = q\sum_{i,j} n_{s,ij} T_{ij} f_{ij}$$



J. P. Sun, W. Wang, N. Gu and P. Mazumder, "Gate Current and Capacitance Models of Nanoscale MOSFETs," *IEEE Transactions on Electron Devices*, vol. ED-53, no. 12, Dec.2006, pp. 2950-57.

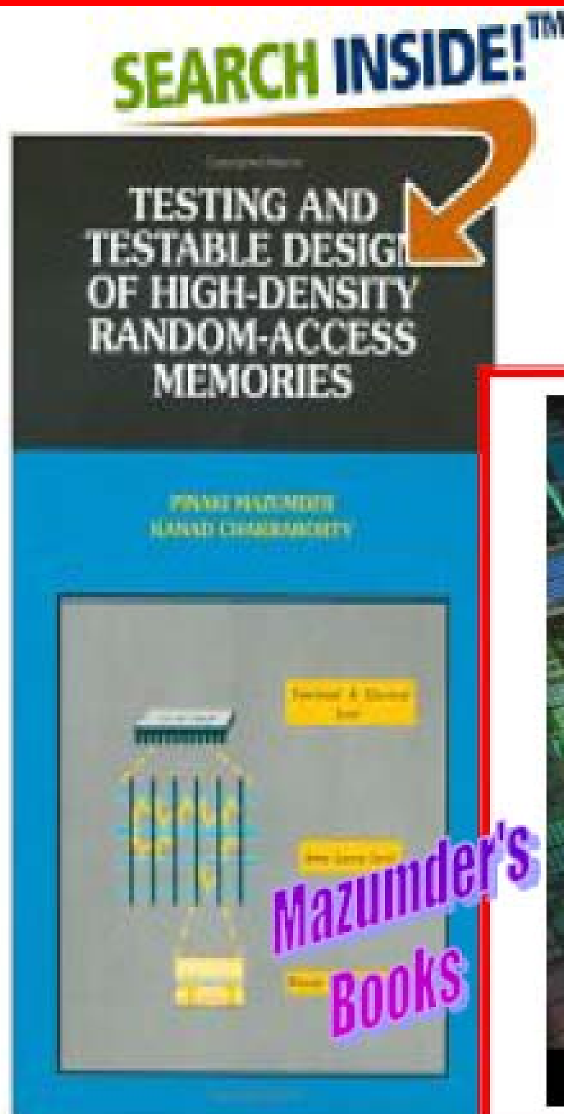


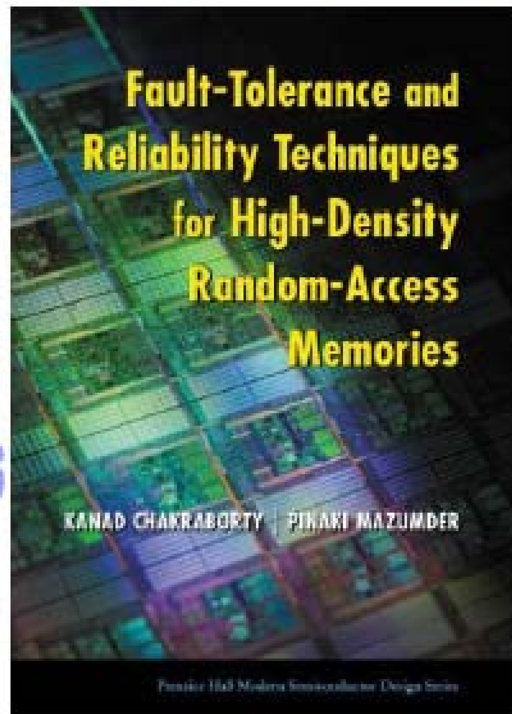
HfSiON Gate provides High Thermal Stability, Good Interface Property Requirement: I-RET < 10E-16 A/Cm^2 & I-PROG > 10E-2 A/Cm^2 is satisfied by Curves 2 and 3 Only ➔ N content 20%-30%

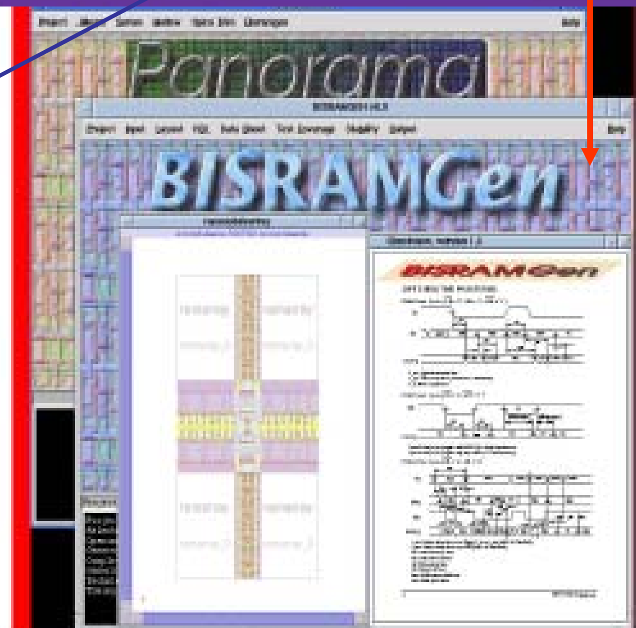
TOPIC #4

Mazumder's Books on Semiconductor Memories

Circuit Techniques	Test Algorithms	Error Correction	Self Repair	Compiler
• DFT for DRAM *TC-89* • DFT for CAM *TCAD-88* • DFT for random test *JETTA-92* • BIST for RAM *TIE-89* • ASIC for memory testing *JSSC-91*	• Parallel PSF *DAC-87, ITC-87* • Parallel parametric tests *JSSC-89* • Parallel stress tests *JETTA-94* • Tests for device-related faults *TCAD-93* • Board-level test *JETTA-2000*	• Double-bit ECC *JSSC-92* • Parallel signature analyzer based ECC *JSSC-93* • Projective geometric code *TC-93* • Radiation study • Reliability analysis	• Pseudo-analog adaptive circuits for self-repair *TCAD-96* • Digital adaptive circuits for self-repair *TCAD-93* • Generalized adaptive self-repair circuit techniques *TCAD-92,93*	• RAM compiler - Self-testing - Self-repair *EDAC-99* • ROM compiler - Self-testing - Self-repair *ICCD-99* *VLSIJ-99*







RAM Research Overview

Circuit Techniques	Test Algorithms	Error Correction	Self Repair	Compiler
• DFT for DRAM *TC-89* • DFT for CAM *TCAD-88* • DFT for random test *JETTA-92* • BIST for RAM *TIE-89* • ASIC for memory testing *JSSC-91*	• Parallel PSF *DAC-87, ITC-87* • Parallel parametric tests *JSSC-89* • Parallel stress tests *JETTA-94* • Tests for device-related faults *TCAD-93* • Board-level test *JETTA-2000*	• Double-bit ECC *JSSC-92* • Parallel signature analyzer based ECC *JSSC-93* • Projective geometric code *TC-93* • Radiation study • Reliability analysis	• Pseudo-analog adaptive circuits for self-repair *TCAD-96* • Digital adaptive circuits for self-repair *TCAD-93* • Generalized adaptive self-repair circuit techniques *TCAD-92,93*	• RAM compiler - Self-testing - Self-repair *EDAC-99* • ROM compiler - Self-testing - Self-repair *ICCD-99* *VLSIJ-99*

Books written by P. Mazumder

- Testing and Testable Design of High-Density RAM, 1996
- Fault Tolerance of RAM, 2000
- Circuit Techniques for DRAMs (under preparation)

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