SRC/NSF/A*STAR Forum on 2020 Semiconductor Memory Strategies
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Performance Projections for Nanomechanical Memory

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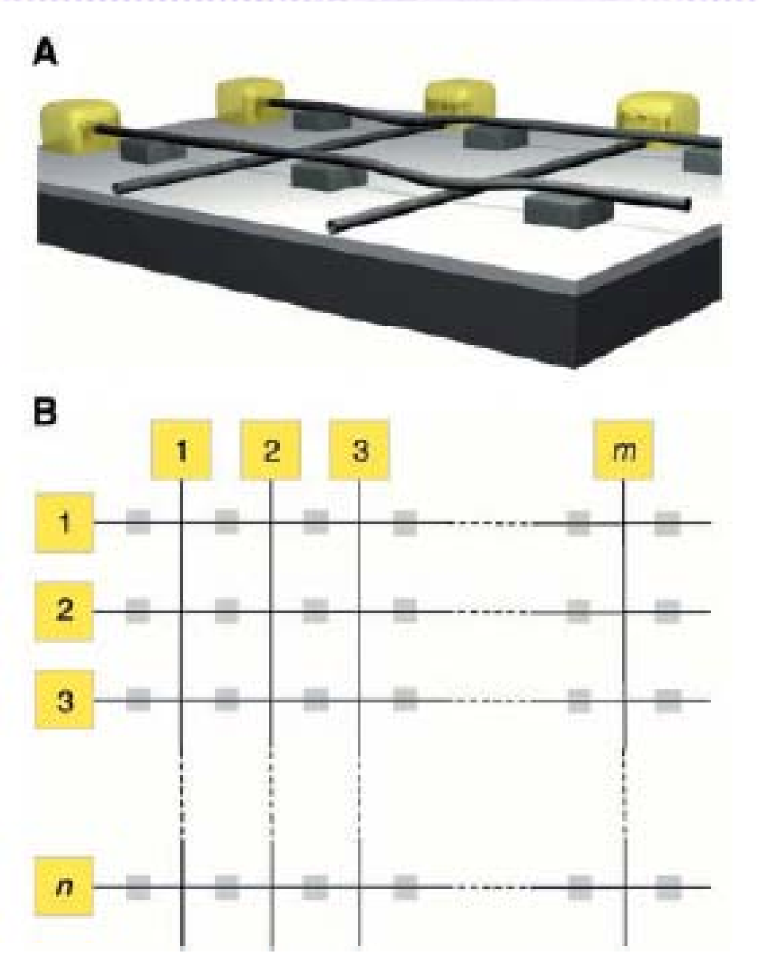
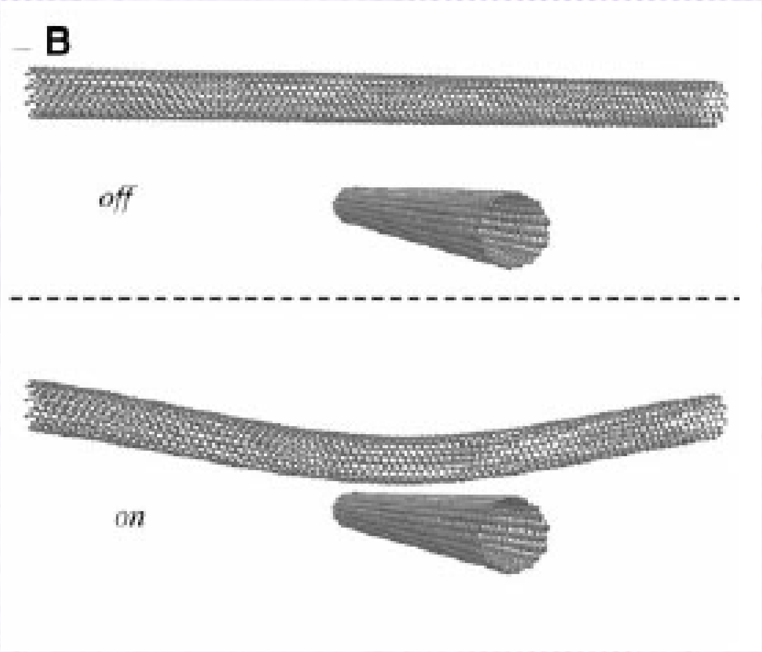
TOKYO TECH Pursuing Excellence TOKYO INSTITUTE OF TECHNOLOGY

QNERC Quantum Nanoelectronics Research Center

SORST JST

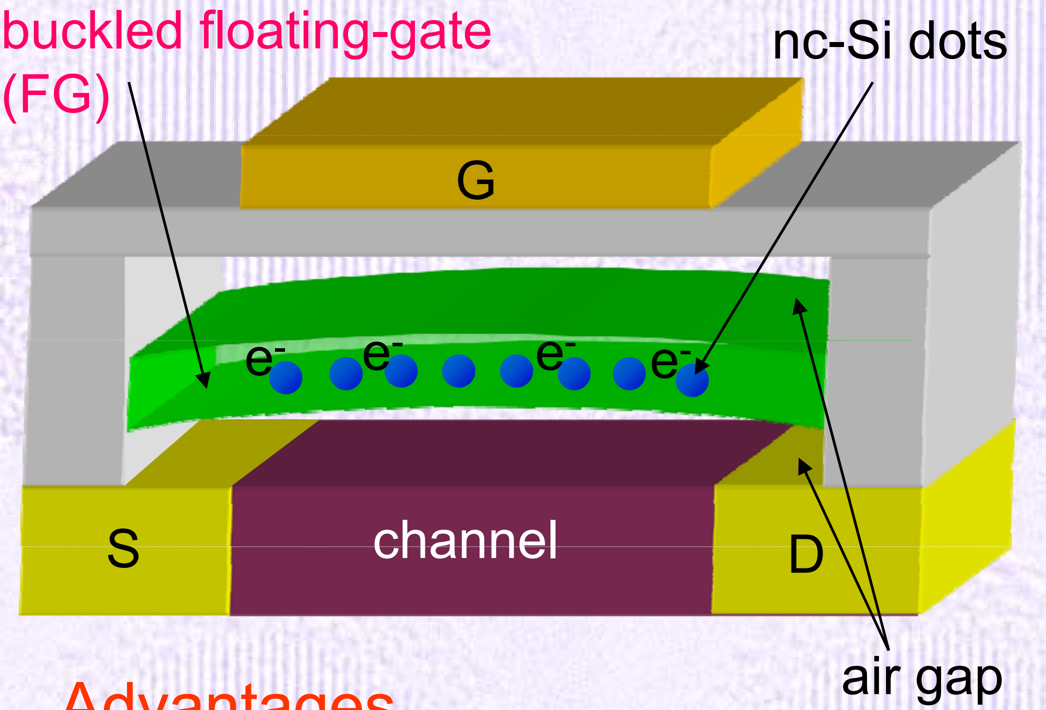
CNT based NEMS mamory

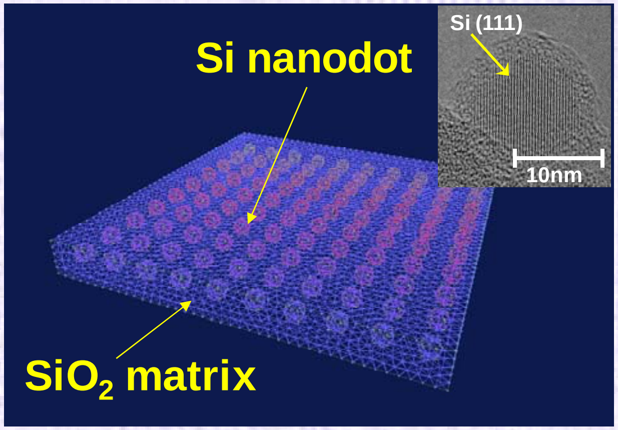


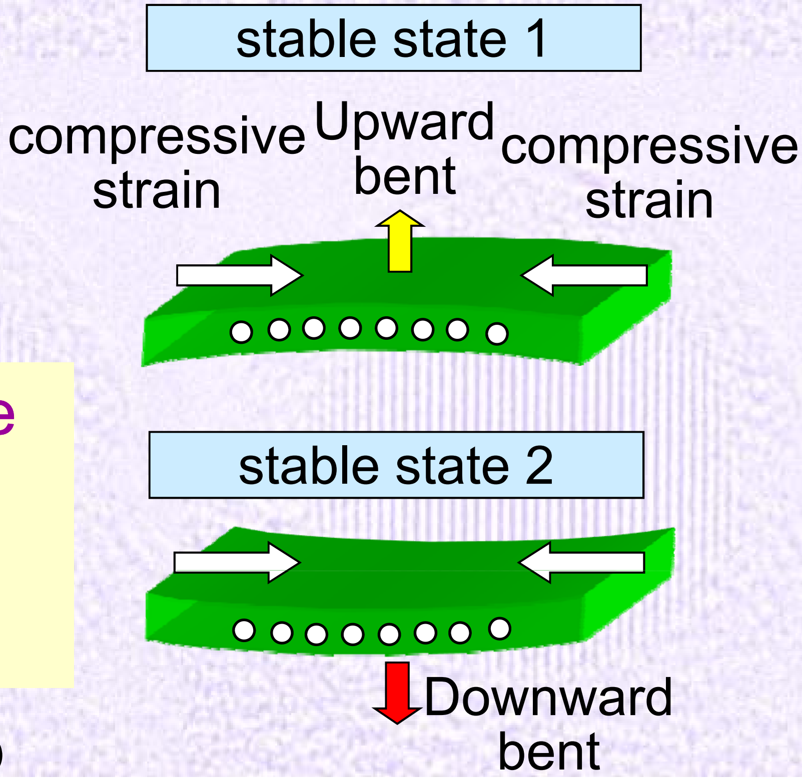


Rueckes et al, Science 2000

Si-based bistable FG nonvolatile NEMS memory






stable state 1

compressive strain

Upward bent

compressive strain

stable state 2

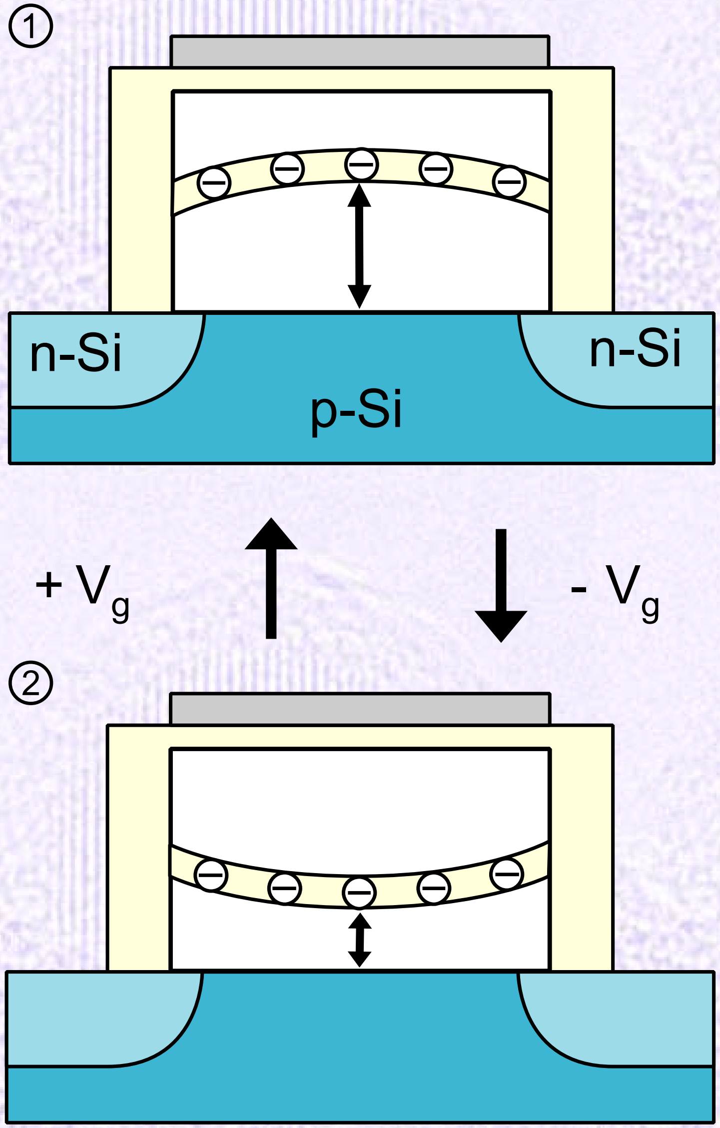
Downward bent

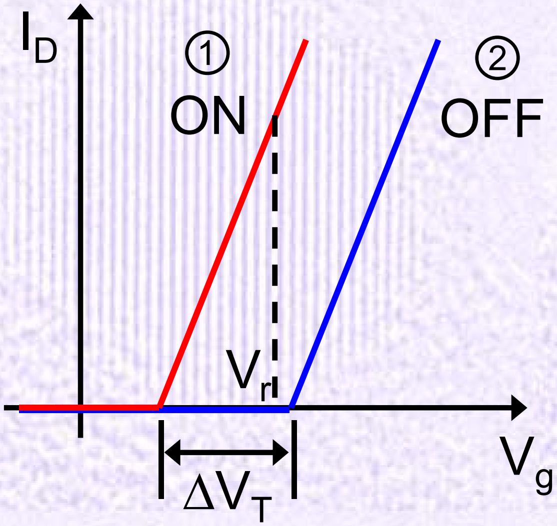
Advantages

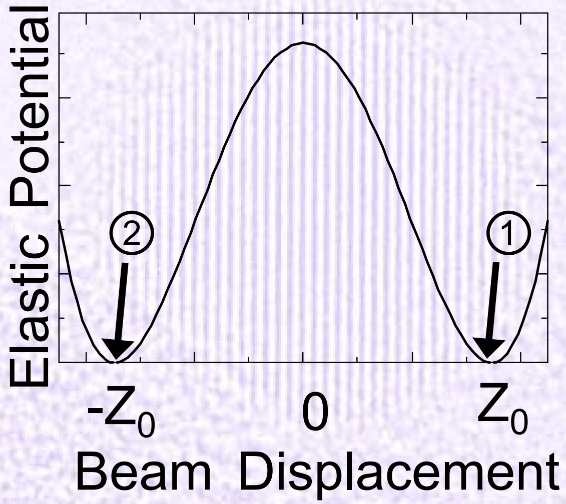
- No charge tunneling via gate oxide
- High-speed write/erase operation
- Compatibility with conventional Si process

J. Appl. Phys. **100**, 094306 (2006), IEEE T-ED **54**, 1132 (2007)

NEMS memory: Operation principle







Write/Erase (switching)

Apply positive or negative gate voltage.

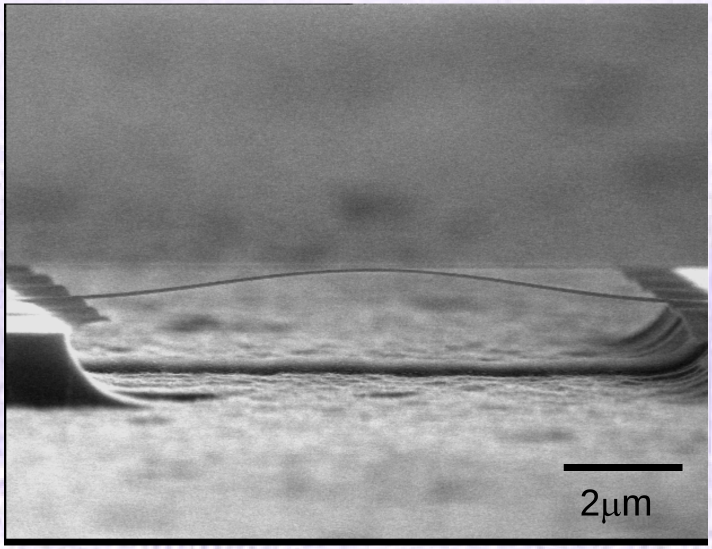
FG moves upward or downward
by electrostatic force

Read state

Difference of distance between FG and substrate causes threshold voltage shift.

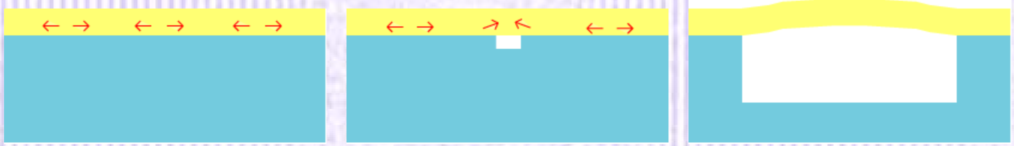
Test beam structure fabrication

SEM image of a beam



Naturally upward-bent bridge structure observed

→ Release of stress at Si/SiO_2 interface after undercut



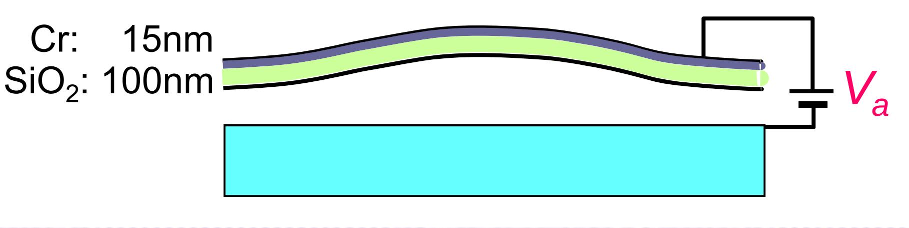
Thermal oxidation

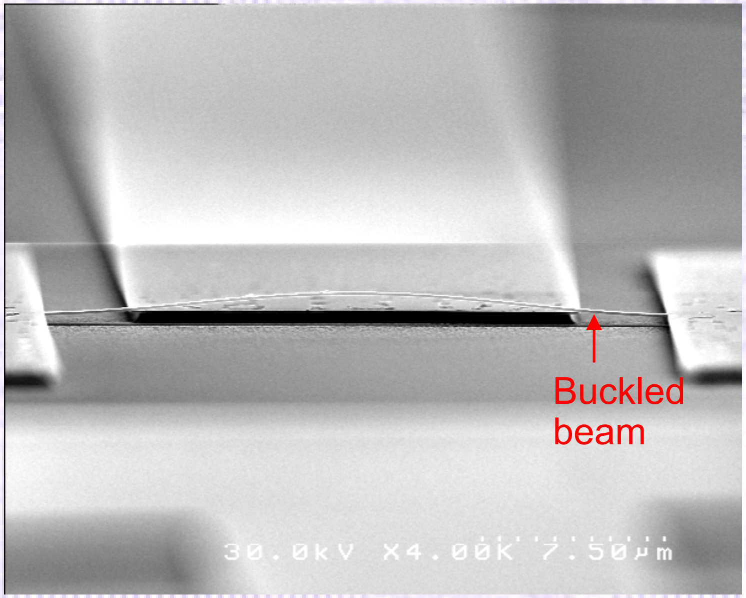
Isotropic etching

Bent upward

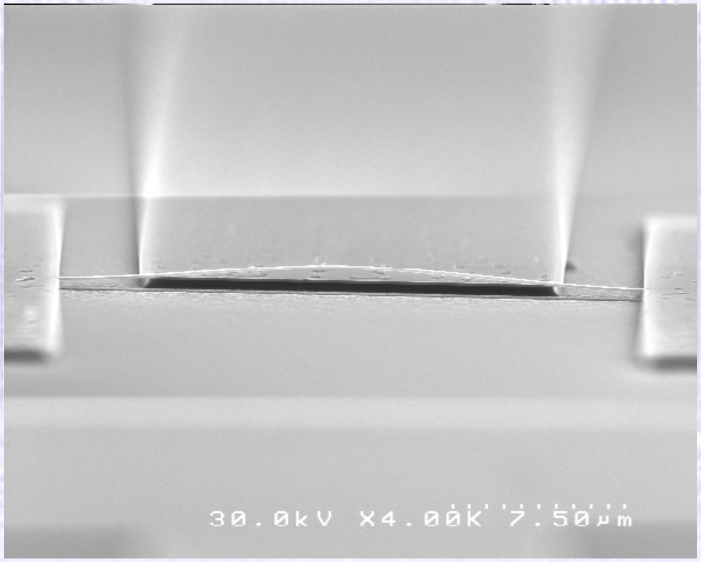
J. Appl. Phys. **100**, 094306 (2006)

Electrical switching of the beam





$V_a = 0V$

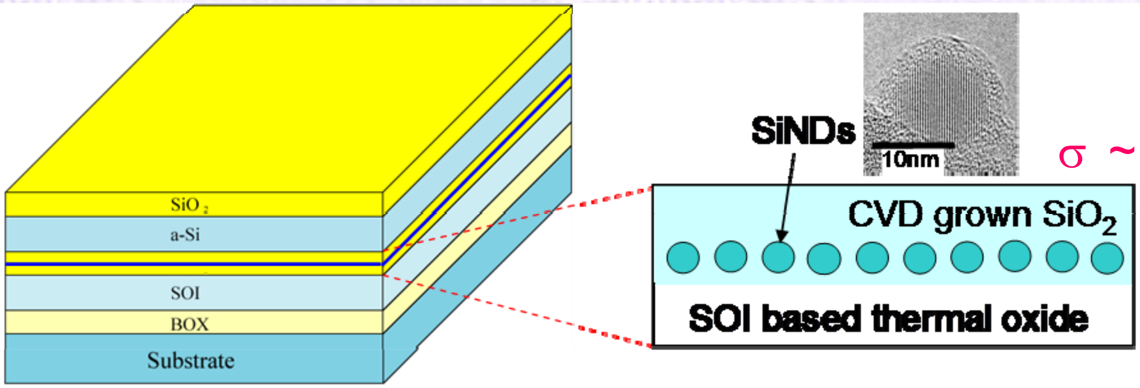


$V_a = 36V$

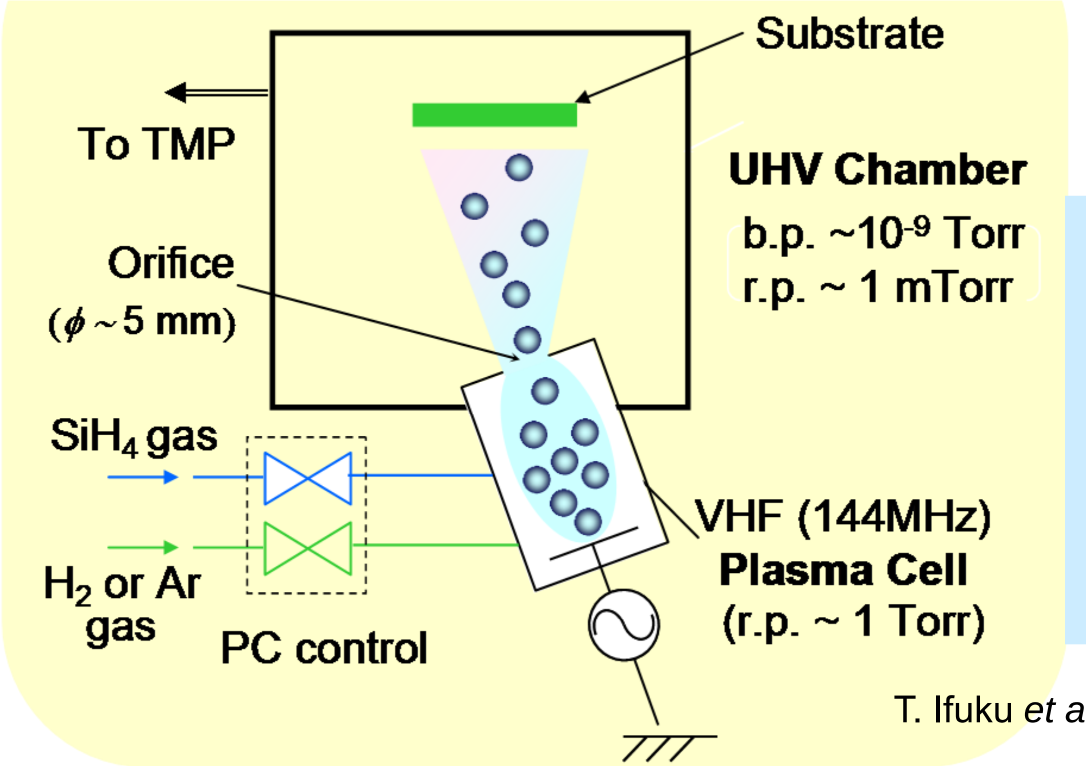
$V_a = 37V$

Mechanical bistability of a self-buckling beam

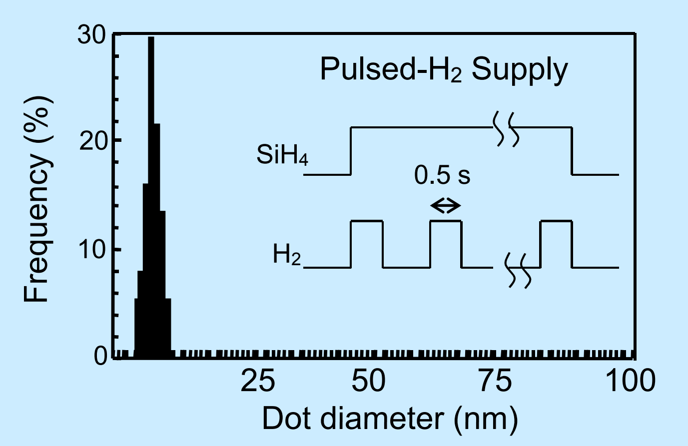
Fabrication of FG with SiNDs



σ ~ 2 x 10^{11} cm^{-2}



Diameter < 10 nm & dispersion ±1nm

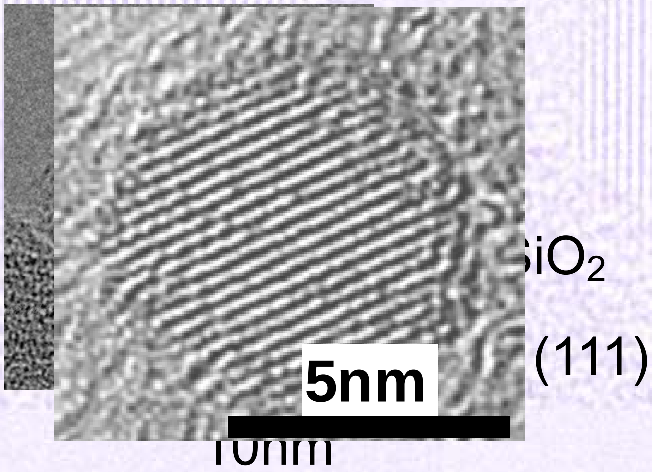


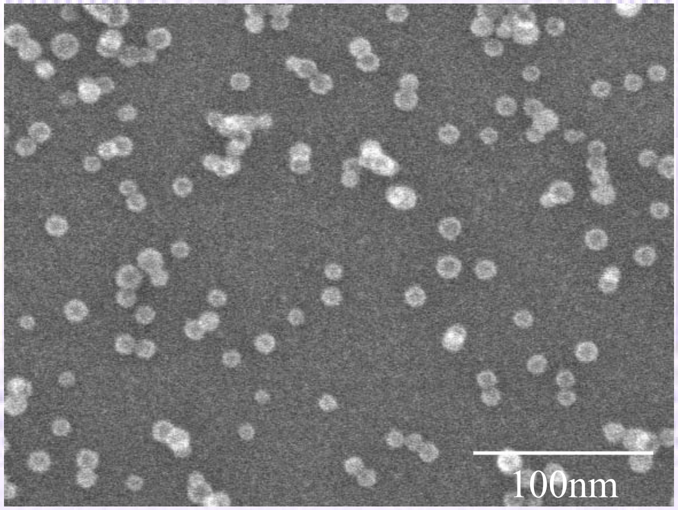
T. Ifuku *et al.*, Jpn. J. Appl. Phys. 36, 4031 (1997)

VHF pulsed plasma process: nc-Si dot deposition

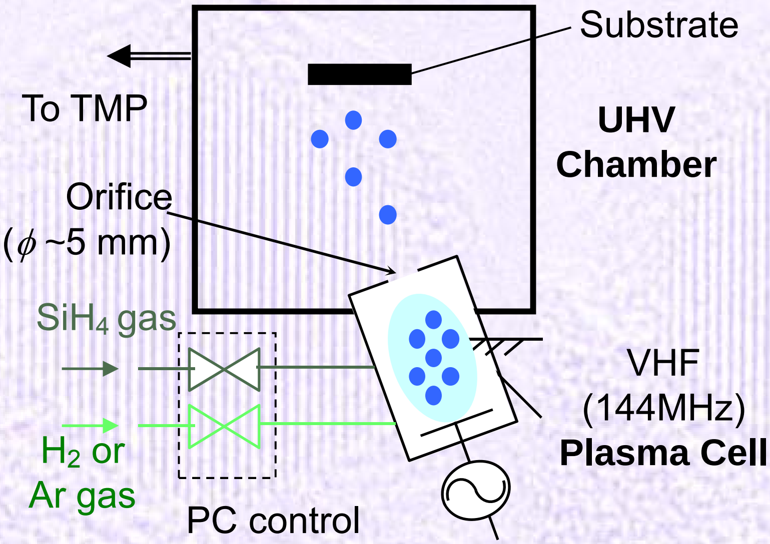
Fabrication of FG with SiNDs

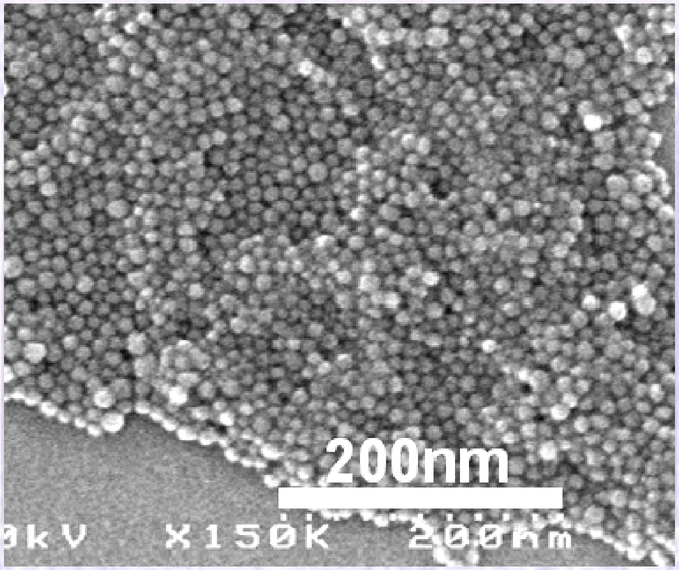
TEM image of a nc-Si dot





As deposited

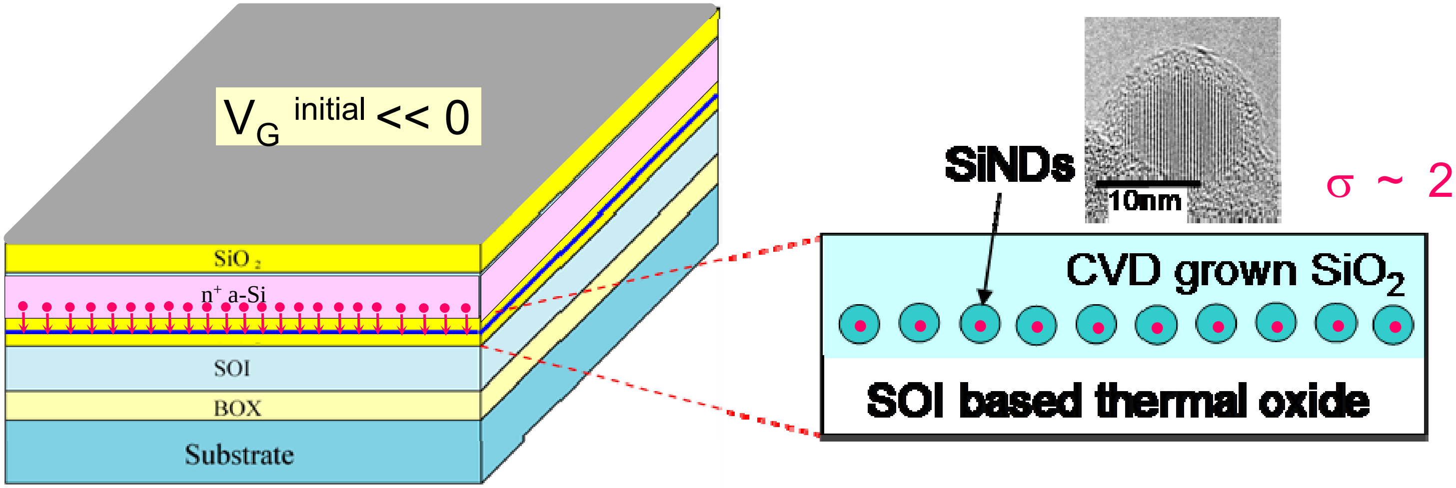




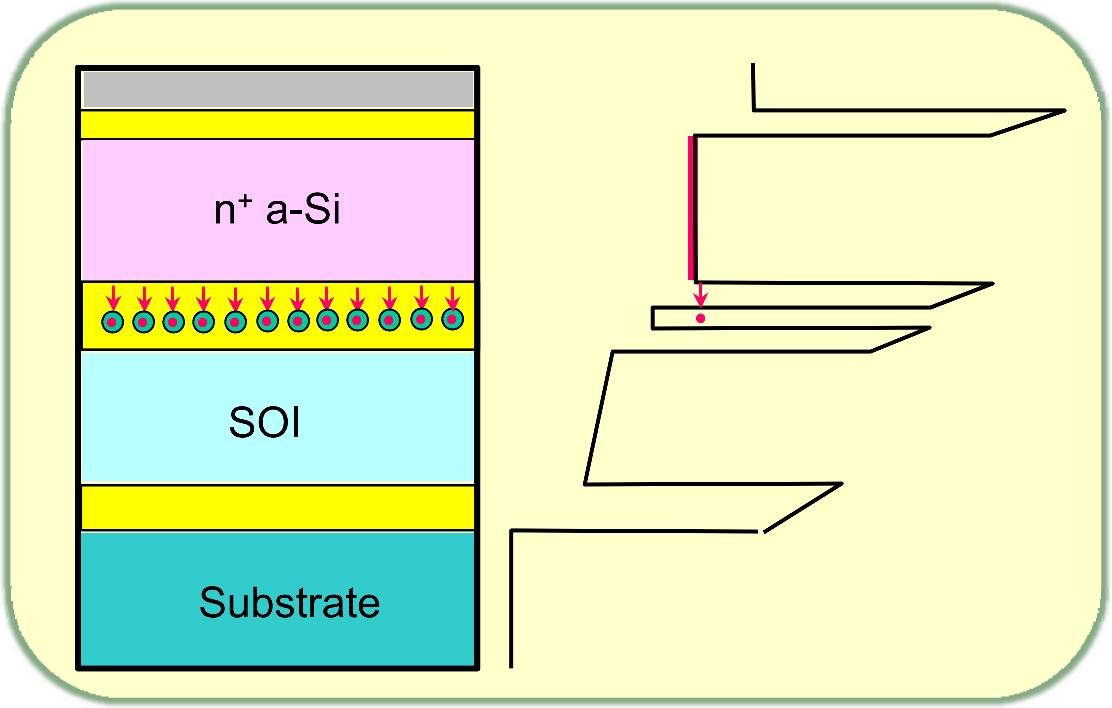
Assembled

Current Applied Physics **6**, 344 (2006)

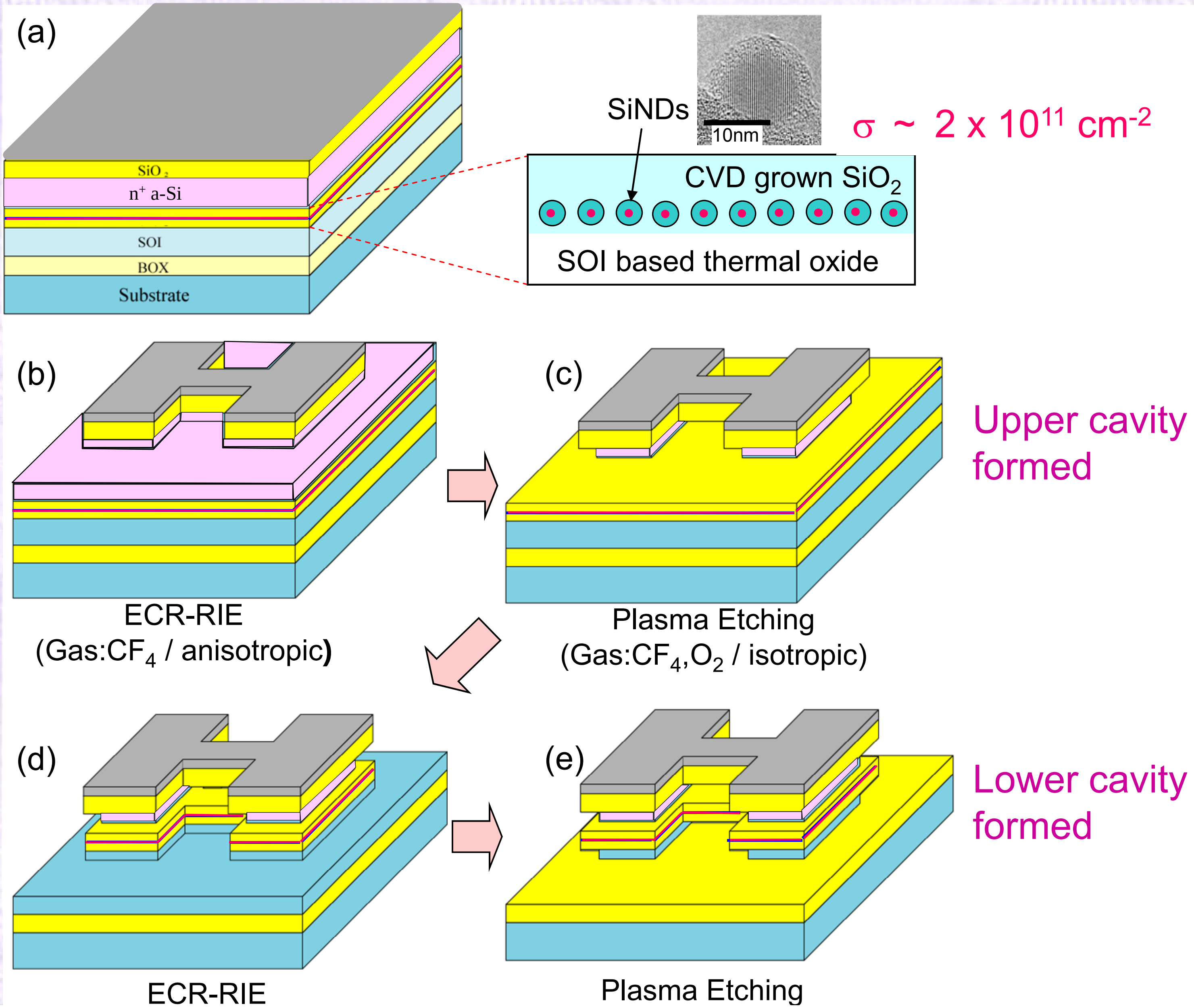
FG charge initialization



$\sigma \sim 2 \times 10^{11}\ \mathrm{cm}^{-2}$



Fabrication of FG with SiNDs



$\sigma \sim 2 \times 10^{11}\ \mathrm{cm}^{-2}$

ECR-RIE
(Gas:CF_4 / anisotropic)

Plasma Etching
(Gas:CF_4,O_2 / isotropic)

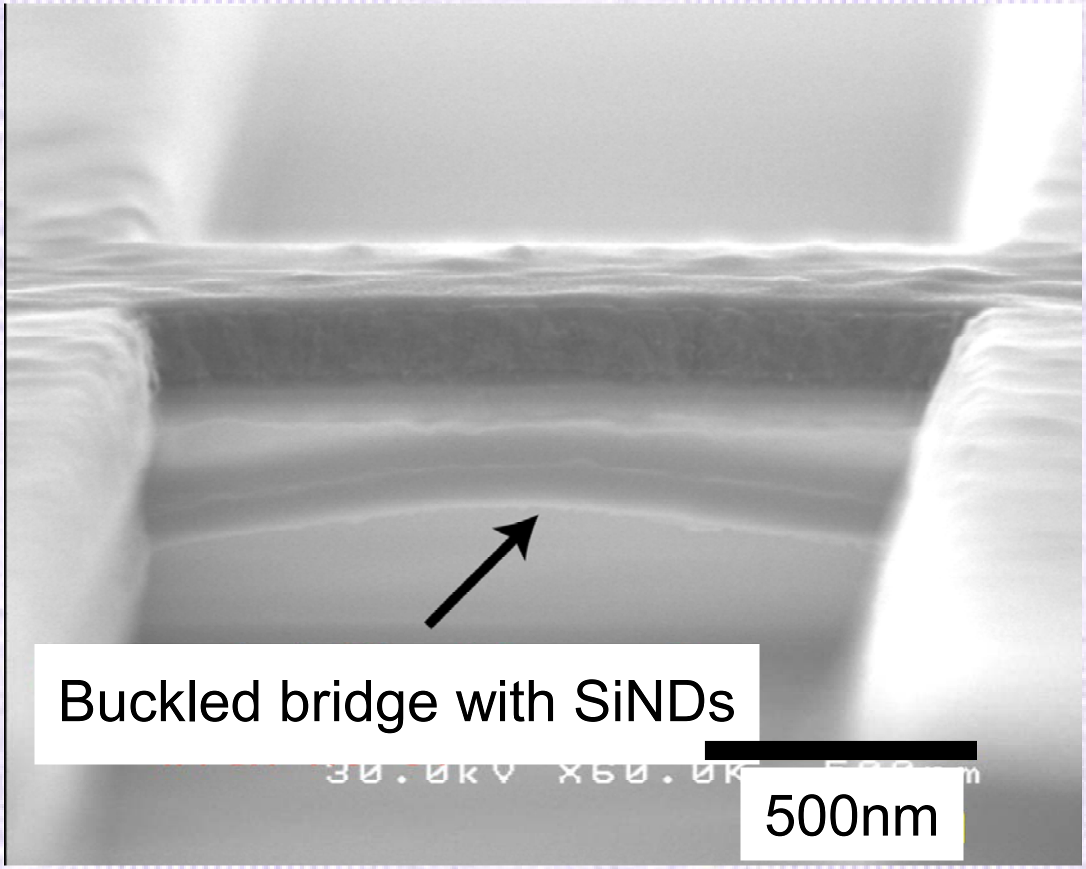
Upper cavity formed

ECR-RIE

Plasma Etching

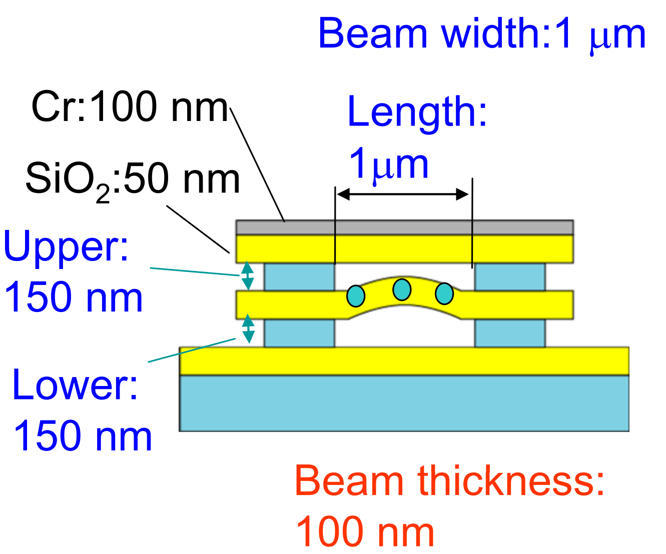
Lower cavity formed

Fabrication of FG with SiNDs



Buckled bridge with SiNDs

500nm



Beam width:1 μm

Cr:100 nm

SiO_2:50 nm

Length:
1μm

Upper:
150 nm

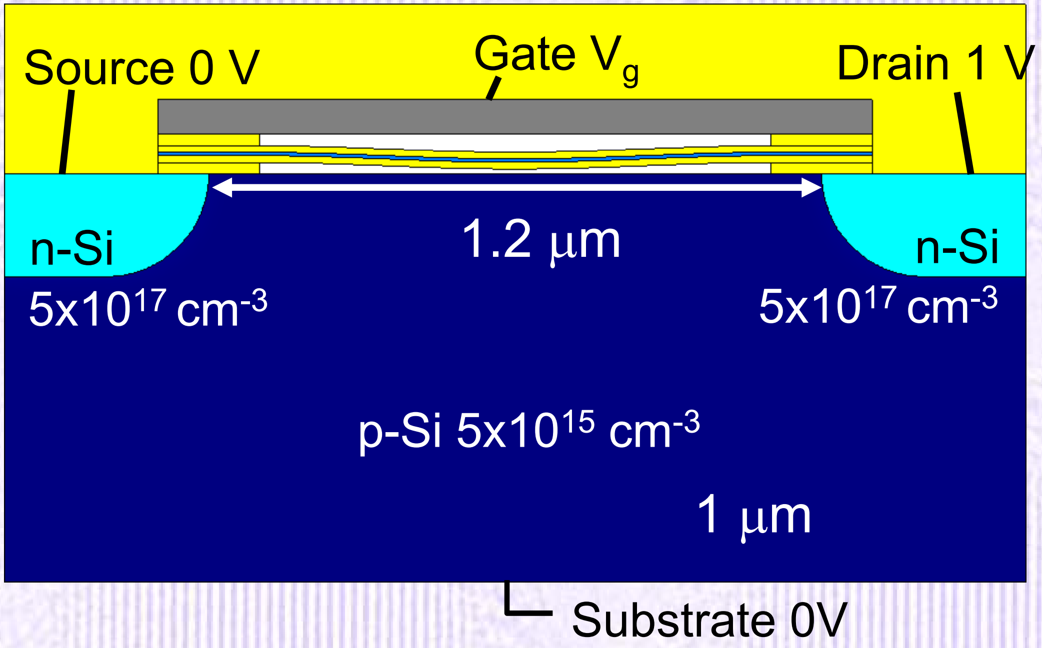
Lower:
150 nm

Beam thickness:
100 nm

2D simulation of NEMS memory

Finite element method multiphysics simulation

Structural mechanics + Electrostatics + Drift-diffusion

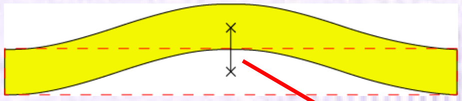


🟨 SiO_2 (70 GPa)

🟦 Si (170 GPa)

⬛ Metal (140 GPa)

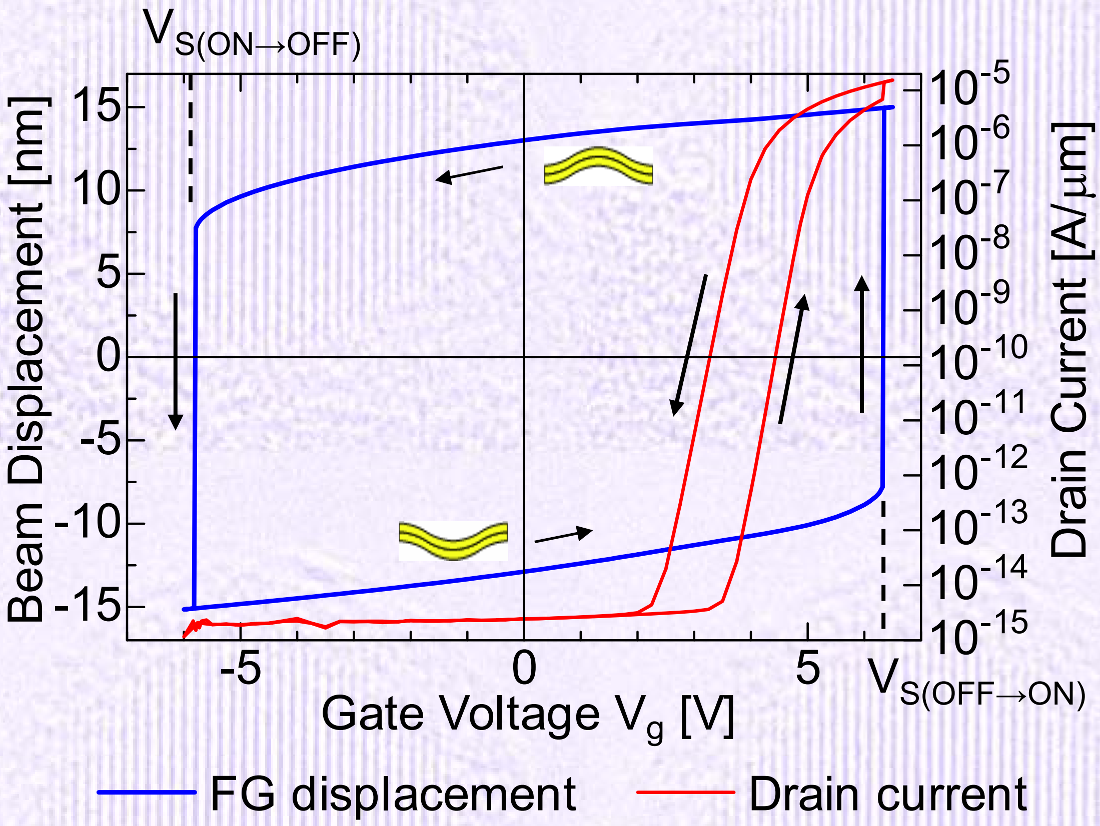
Stored charge density
-0.096 [C/cm^3]

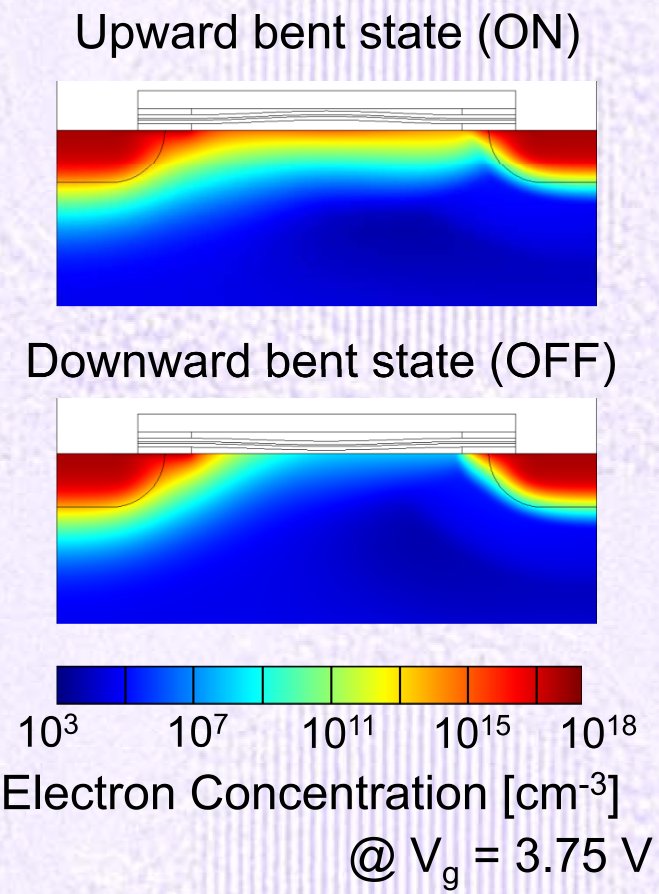


Calculating floating gate displacement and drain current characteristics

$$\begin{aligned} J &= \left(-qn\mu_n \nabla\psi + qD_n \nabla n\right) \\ &\quad + \left(-qp\mu_p \nabla\psi - qD_p \nabla p\right) \end{aligned}$$

Steady state analysis of NEMS memory



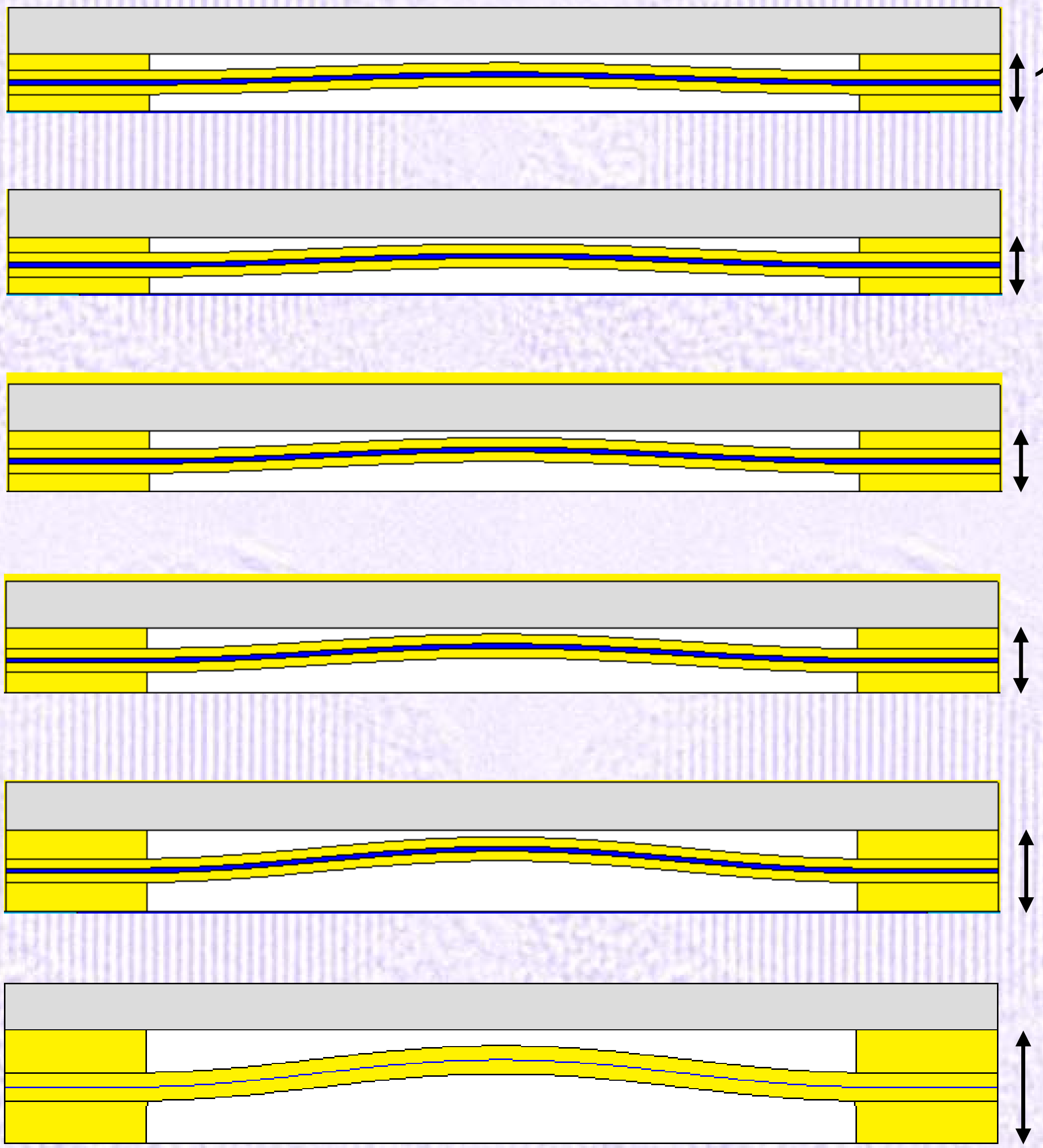


@ V_g = 3.75 V

Floating gate can be switched by applying gate voltage.

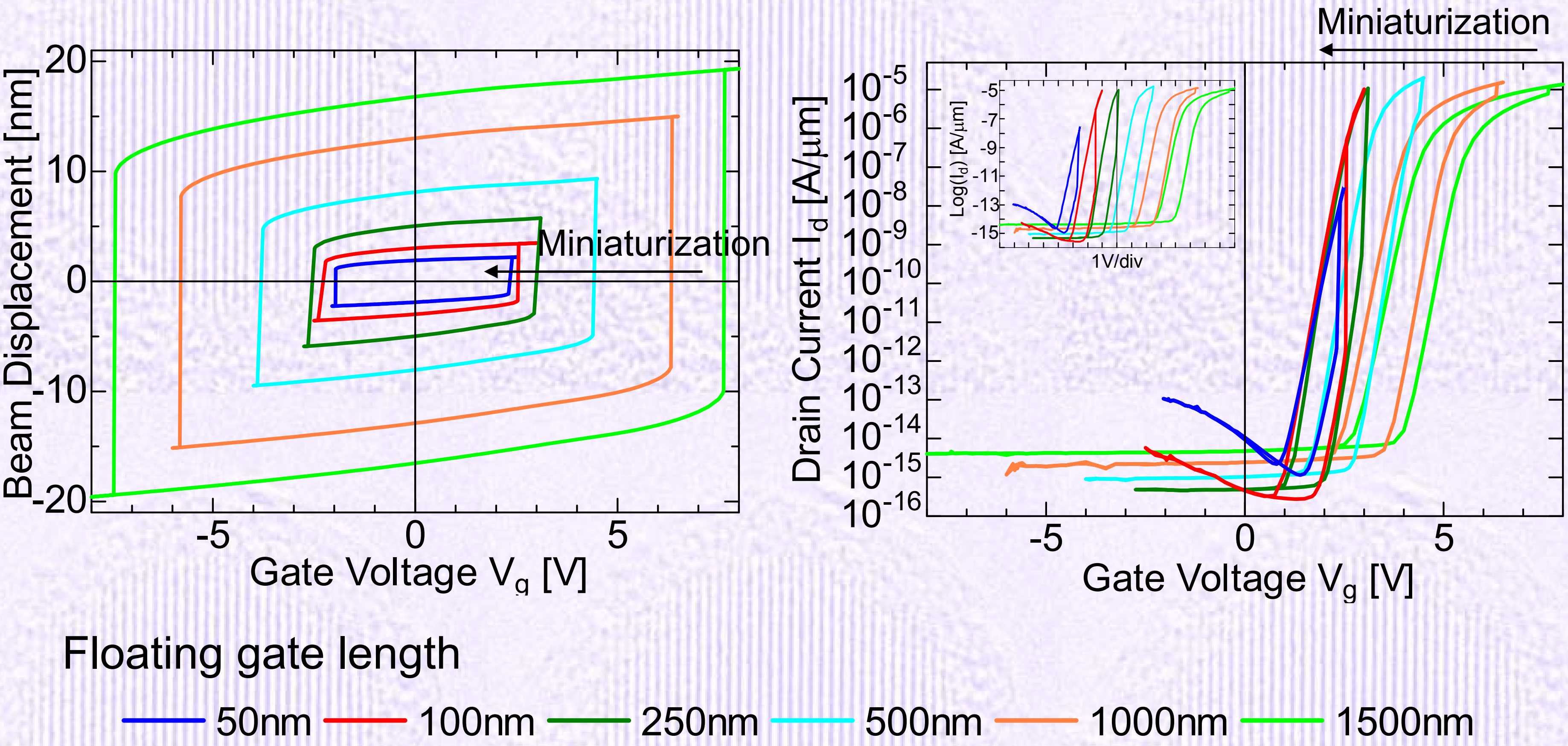
Drain current changes by position of floating gate.

Simulated structures

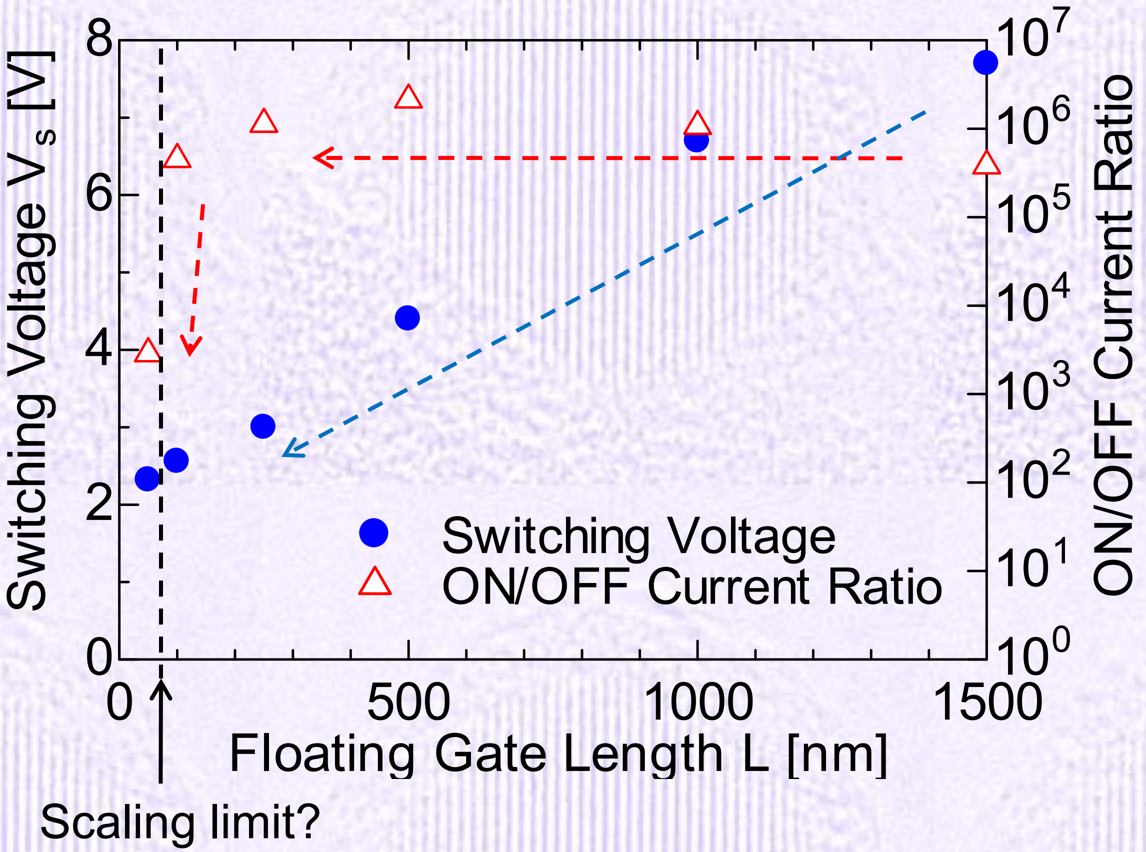


	FG length
120 nm	1.5 µm
79.3 nm	1 µm
41.7 nm	500 nm
22.3 nm	250 nm
12.7 nm	100 nm
8 nm	50 nm

Beam displacement and drain current characteristics



Memory property changes by scaling



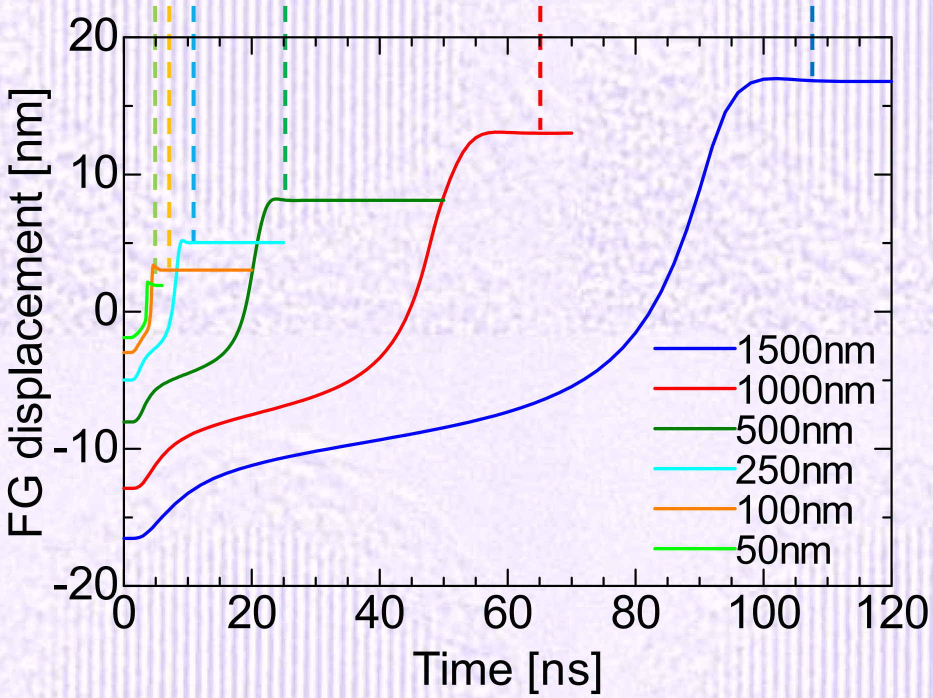
Switching voltage decreases with size reduction.

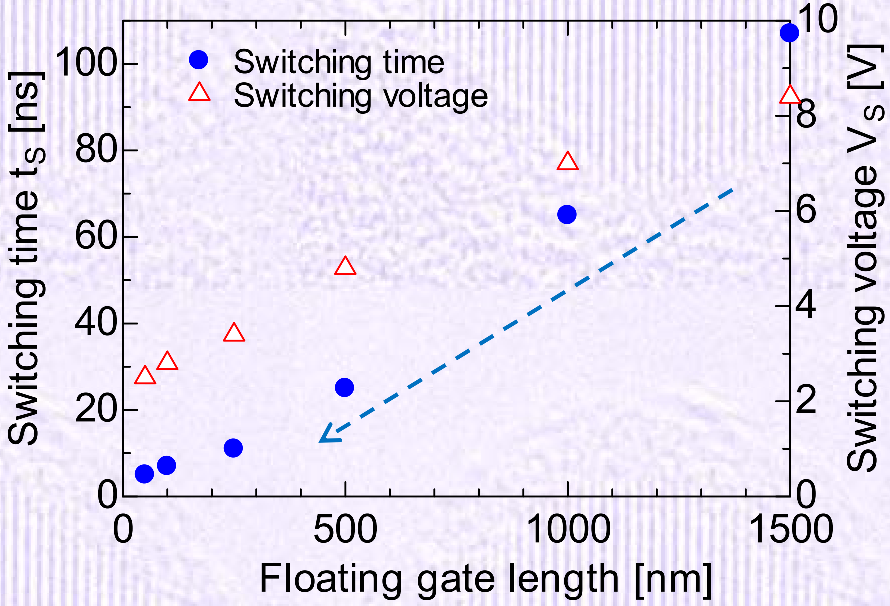
Current ratio is maintained 10^5~10^6 until L = 100 nm.

Transient response and switching time

Applying pulse voltage and calculating switching response

(Assuming ideal damping factor for each structure)





Switching time decreases with size reduction.

Switching time 7 ns @ L100 nm, V_g2.8 V

Estimation of energy consumption

Estimating energy consumption from total energy

$$E_{sum} = E_m + E_k + E_d + E_e + E_R$$

Mechanical energy

$$E_m = \int_V \frac{1}{2} \varepsilon \cdot \sigma dV = W \times \int_S \frac{1}{2} \varepsilon \cdot \sigma dS$$

σ : stress ε : strain

Kinetic energy

$$E_k = \int_V \frac{1}{2} \rho \mathbf{v}^2 dV = W \times \int_S \frac{1}{2} \rho \mathbf{v}^2 dS$$

Electrostatic energy

$$E_e = \int_V \frac{1}{2} \mathbf{E} \cdot \mathbf{D} dV = W \times \int_S \frac{1}{2} \mathbf{E} \cdot \mathbf{D} dS$$

Damping loss

$$E_d = \int_V \int_0^t \mathbf{F}_d \cdot \mathbf{v} dt dV$$

$$= W \times \int_S \int_0^t \left(\alpha \rho \mathbf{v}^2 + \beta \frac{\partial \sigma}{\partial t} \cdot \frac{\partial \varepsilon}{\partial t} \right) dt dS$$

α: mass damping factor

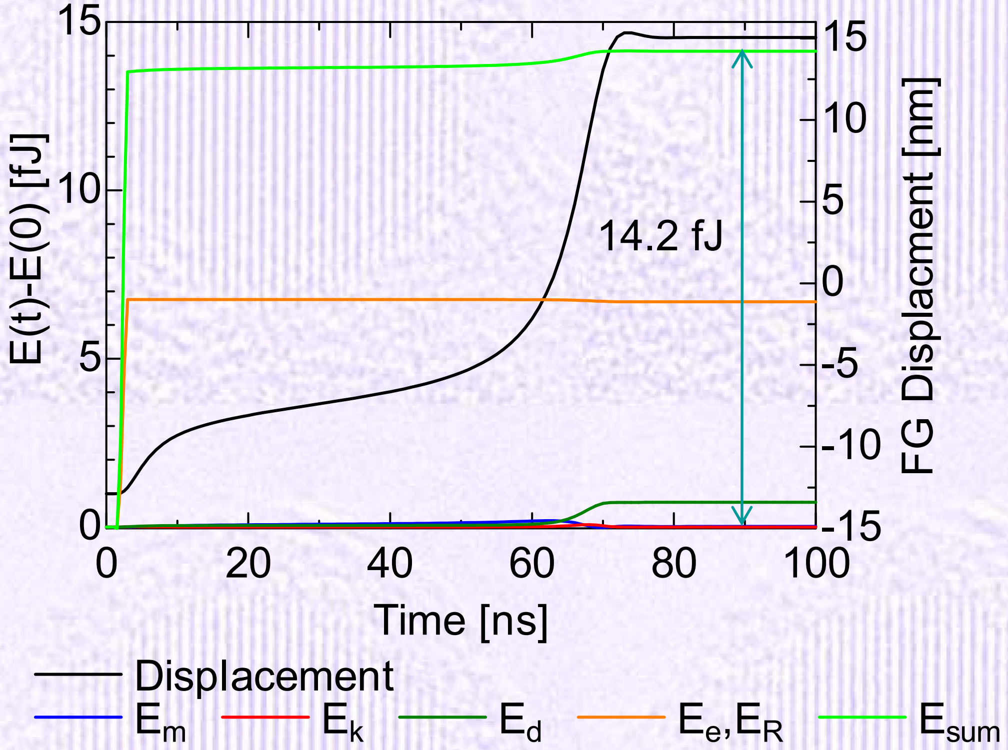
β: stiffness damping factor

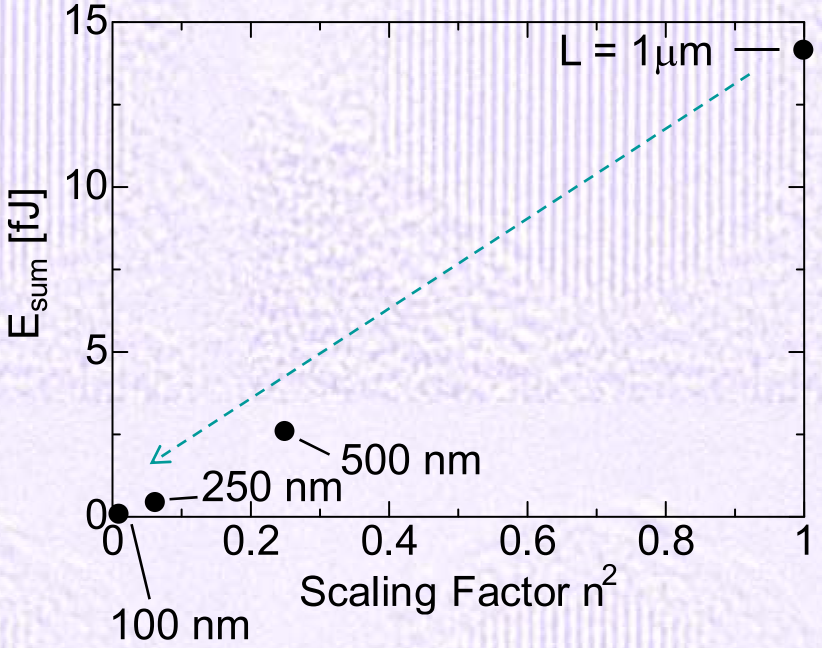
Charging loss

$$E_R = E_e(t) - E_e(0)$$

Switching energy variation by scaling

V_g 6.7 V step voltage (L = 1 μm)





E(t=0)

E_m: 31.5 fJ, E_e: 0.73 fJ, E_k,E_d,E_R: 0 fJ

Size reduction

⬇

Low energy consumption

(0.07 fJ? @ L100nm)

Conclusion

- We have performed numerical simulation of NEMS memory devices featuring mechanical bi-stability as a memory node.
- Memory performances enhance with decreasing suspended floating gate length L from 1000nm to 100nm, where switching voltage of 2.5V, switching speed of 15ns, and switching energy of 0.2fJ are projected.
- However, at 50nm, memory window collapses in this device structure. Although not suitable for ultra large scale integration, the fast and ultra low power NEMS memory, which does not require current flow for switching, may find suitable application in mobile terminals.
- Alternative structure, e.g., CNT, may extend scalability.