A-STAR/SRC/NSF Memory Forum – Singapore

Panel VI: Needs and Models for Collaborative Research

Research Priorities/Needs

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Panel VI: Needs and Models for Collaborative Research

Background

There are many successful examples of collaborative research by semiconductor industry. What model would work best for the memory industry?

Discussion

Please identify **drivers** for research collaboration in emerging memory technologies

- e.g. application landscape

Please identify **barriers** to research collaboration in emerging memory technologies.

What are promising areas for path-finding research in future memory technologies via an inter-regional industry-government-university collaboration?

What principles should a collaborative model embrace?

- How should the research be implemented?
  - What are the appropriate roles of industry, academia, and government organizations in the conduct of the research?
- What mechanisms should be used to develop research goals and to ensure program focus?
- How can intellectual property rights be shared among research performers/program sponsors?
- How can program agility with respect to emerging research opportunities be maintained?
  - For example, can collaborative research be performed without the need to build and own a state-of-the-art fabrication facility?
  - How can management overhead costs be controlled and minimized?
- What mechanisms should be put in place to enable transfer of knowledge and 'know-how' to the sponsors?

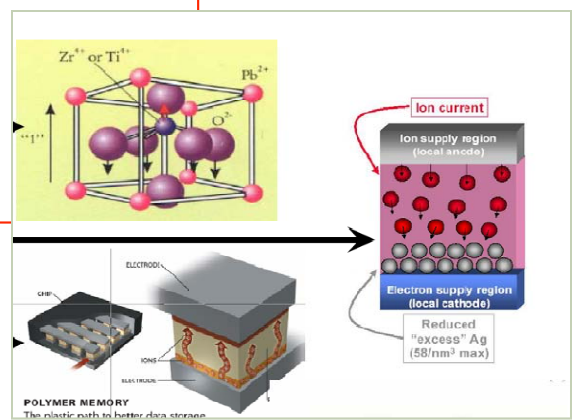
How important is the production of highly-trained graduate students in a collaborative memory research program?

Emerging Memory Research Collaboration - Drivers

- Drivers
  - End of the roadmap scaling limits for DRAM/Flash
  - Applications landscape
    - Socket level chip replacement unlikely
    - Application specific solutions likely to be required
  - Market participation is Global
  - To many options, too little time (and $$)

Alternate Storage Mechanisms

- Moving Atoms
  - PCM, RRAM (Filament, Metal Oxide), FeRAM, CNT, Molecular….
- Moving Spins
  - MRAM, STTRAM, Racetrack…



Emerging Memory Research Collaboration - Barriers

- Barriers
  - Standards
    - Performance metrics and requirements
    - Communication interfaces to CPU
    - Applications specifications
  - IP
    - Commodity memory is a low margins business
  - Competitive Landscape
    - Level playing field

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Research Priorities/Needs

- Potential benefits from research collaboration
  - Resource/expertise sharing
  - Standardized performance characterization methodology
  - Guide research with consolidated success metrics
- Requirements
  - Fast paced learning
  - Materials screening, device level data at scale of interest
  - Comprehensive approach to address all aspects of memory technology performance

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Emerging Memory Technologies

Storage Mechanism	*Present Day Baseline Technologies (taken from ITRS 2005 Edition)*		*Nanowire Memory (C. Zhou)*	*Single Electron Memory (J. Liu)*	*Hybrid Memory (Y.Yang & C.Ozkan)*	*Phase – Change RAM (Y.H.Xie)*	*Polymer Memory (R.Kaner & Y.Yang)*	*Molecular Memory (F.Stoddart & W. Goddard)*	*Spin Memory (K.W. Kim)*
Device Type, Material Used	Standalone DRAM (2005) 80nm node	NOR Flash - (2005) 130nm node	Nanowires; In_2O_3, Si with redox active molecules	floating gate using $CoSi_2/Si$ hetero-nanocrystals	protein virus nanowires with platinum nanoparticles & quantum dots	GeSbTe templated self-assembled PS-PI block copoly.	polyaniline nanowires with Au nanoparticles	rotaxanes or catenanes	spin state variable using high temp DMS
Read Time	**(<15ns)**	**(14ns)**	<80 ns	<80 ns	~1µs	<50ns	~25 ns	~ns	< 10ns
Write Time	**(<15ns)**	**(1 µs)**	**(~ 30 ns)**	**(~100 µs)**	~1µs	**(<50ns)***	~25 ns	~µs	~1 ns
Retention Time	**(64 ms)**	>10 years	**(600 hours)**	10-20 years	**(days)**	>10 years	**(months)**	**(minutes)**	>years
Write/Erase Cycles	infinite	**(>100,000)**	**(> 20,000)**	**(100,000)**	**(400)**	~ 10^{11}	>100,000 **(~4,000)**	**(<35)**	> 100,000
On/Off Ratio	**(< 10,000)**	**(< 10,000)**	**(~ 10,000)**	**(~10^4 -10^5)**	<10,000 **(~ 1000)**	>100	**(~ 10,000)**	**(~ 2-11)**	unknown
[a] *Scalability cell size in µm²* *Limiting Factor*	32nm node $6F^2$ = 0.0061 (year 2013) High-k material	45nm node $10F^2$=0.021 (year 2010) Oxide thickness	<0.0001µm² redox molecule stability & self assembly variability	**(1µm²)** < 0.0011µm² dot density fluctuation	**(0.01µm²)** <0.0001µm² variability of metal particle size & density	**(0.06µm²)*** ~0.04µm² density-limited by thermal proximity effect	**(0.04µm²)** <0.0001µm² size and fluctuation of metal particles	**(0.0002µm²)** <0.0001µm² molecule stability and variability	<0.0001µm² curie temp of DMS
General Advantages	High Density, Economy	Non-volatile	low cost, flexible, High density	high density, CMOS compatible	low cost, high density, bio compatible	non-volatile, stable, scalable	low cost, high density, fast	ultra high density	high density, low power, scalable
Challenges	scaling, gate leakage, capacitor formation	scaling, oxide thickness, power dissipation	integration and material stability	dot density fluctuation, scaling	material stability integration, scaling	large write current, new materials and process	material stability, integration, temp influence	speed, stability, on/off ratio, temp influence	material, high curie temp
Fabrication Technique	Lithography	Lithography	lithography and self-assembly	lithography and self-assembly	self-assembly, wet synthesis	templated and lithography	self assembly, wet synthesis	litho & self-assembly	lithography

Prof. Kang Wang, UCLA

Memory Technology Development

EDA tool Vendors

Materials suppliers

Module and PI

Design and modeling

Test and Product Eng

Memory Technology

Electronic systems producers

Business Development

Packaging Development R@D and QA

Tool Vendors

IDM perspective

Memory IC - Ecosystem

Manufacturing Fabs

Equipment and Materials suppliers

Customers

Electronics systems producers

Memory Product

Process module integration

Collaborative Research Programs

Assembly Packaging Testing

Circuit Design and Architecture

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