Materials For Future Memories

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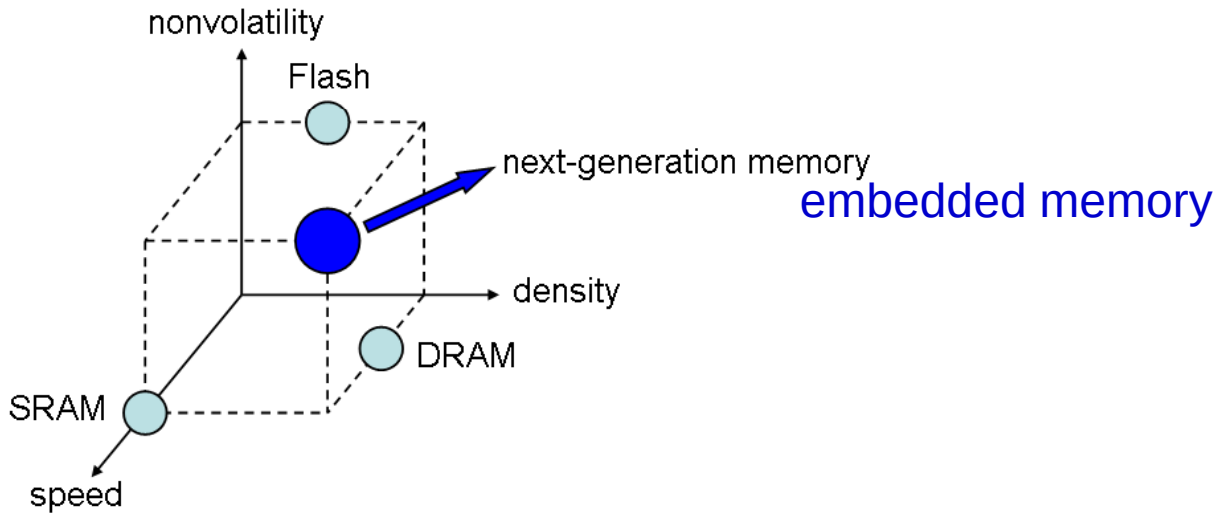
Outline

- Emerging memories introduction
- Materials for Ferroelectric random access memory
  - Capacitor-type FRAM
  - Ferroelectric gate FRAM
- Materials for Resistive random access memory
- Summary

Introduction

An ideal nonvolatile memory



- An ideal nonvolatile memory
  - Low operation voltage, low power consumption, high endurance, long retention time, nondestructive readout, simple structure, low cost, etc
- Possible candidates of next-generation nonvolatile memory
  - Ferroelectric random access memory (FeRAM)
  - Magnetroresistive random access memory (MRAM)
  - Phase change random access memory (PCM)
  - Resistive random access memory (RRAM)

Comparisons

Function	DRAM	SRAM	Flash	OUM	MRAM	RRAM
Non-volatility	No	No	Yes	Yes	Yes	Yes
Program power	Low	Low	High	Low	High	Low
Program voltage	Lo1	Lo1	High		Medium	Low
Read dynamic margin	100-200mV	100-200mV	Delta Current	10X – 100X	20 – 40%	10X – 1000X
Write - Erase time	50ns - 50ns	8ns - 8ns	1μs – 1-100ms	10ns - 50ns	30ns - 30ns	10ns - 30ns
Read time	50ns	8ns	50ns	20ns	30ns	20ns
Program energy	Medium	High	High	Low	Medium	Low
Multi-bit storage	No	No	Yes	Yes	No	Yes
Scalability limits	Capacitor	6T	T-Ox/HV	Litho	Current	Litho
Endurance	∞	∞	10^{12}	$>10^{12}$	$?10^{15}$	$?10^{15}$
Cell size (F^2)	6-12	50-80	7-11	5-8	?	4

2002 IEDM Zhuang et.al. Sharp

Typical or estimated parameter values for a variety of memory technology

Feature	DRAM	SRAM (6T)	FeRAM	Flash	MRAM	PRAM	RRAM
Cell elements	1T1C	6T	1T1C	1T	1T1MTJ	1T1R	1T1R
Density	High	Low	Medium	High	High	High	High
Nonvolatile	No	No	Yes	Yes	Yes	Yes	Yes
Endurance R/W	Good	Good	Moderate	Poor	Good	Good	Moderate
Nondestructive read	No	Partial	No	Yes	Yes	Yes	Yes
Direct overwrite	Yes	Yes	Yes	No	Yes	Yes	Yes
Write	Moderate	Fast	Moderate	Slow	Fast	Fast	Slow
Read access	Moderate	Fast	Moderate	Moderate	Fast	Fast	Moderate
Erase	Moderate	Fast	Moderate	Slow	Fast	Moderate	Slow
Transistor performance	Low	High	High	High voltage	High	High	High
Scalibility limits	Capacitor	6 Transistors	Capacitor	Tunnel oxide/Power	Current density	Lithography	Lithography

Chapter 5, Handbook of Nanoceramics and Their Based Nanodevices, Vol.4,2009

Nonvolatile Memory at a Glance

Parameter	Flash (production)	Ferroelectric RAM	Magnetoresistive RAM	Ovonic Unified Memory
Largest array built, Mb[a]	256	64	1	4
Cell size factor[b]	8-10	18	10-20	5-8
Endurance, cycles	10^6	10^{16}	10^{14}	10^{12}
Read/write voltages, V	2/12	1.5/1.5	3.3/3.3	0.4/1
Read/write speeds, ns	20/1000	40/40	50/50	50/50
Extra mask steps needed to embed memory	6-8	2	4	3-4
In production	Yes	Yes	2004	N.A.
Some major players	• AMD • Intel • Semiconductor Storage Technology • Sharp • Toshiba • STMicroelectronics	• Fujitsu • Ramtron • Samsung • Texas Instruments	• IBM • Infineon • Motorola • NEC • Toshiba	• BAE • Intel • Ovonyx • STMicroelectronics

[a] 1Mb = 1024 by 1024 bits [b] In multiples of the square of interconnect width on the chip's lowest metal level.

IEEE Spectrum, March 2003,pp.49-54

Ferroelectric random access memory (FeRAM)

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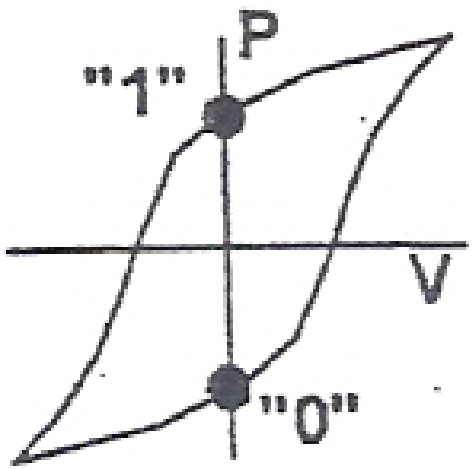
Materials for FRAM



FRAM

$PbZrTiO_3$ (PZT)

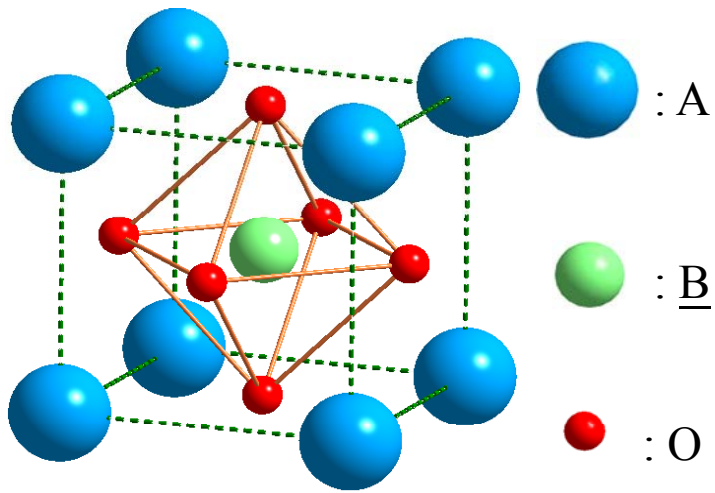
- Larger P_r
- Fatigue-free
- With oxide Electrodes
- Low deposition temp

$SrBi_2Ta_2O_3$ (SBT)

- Smaller P_r
- Fatigue-free
- With Pt Electrodes
- High deposition temp

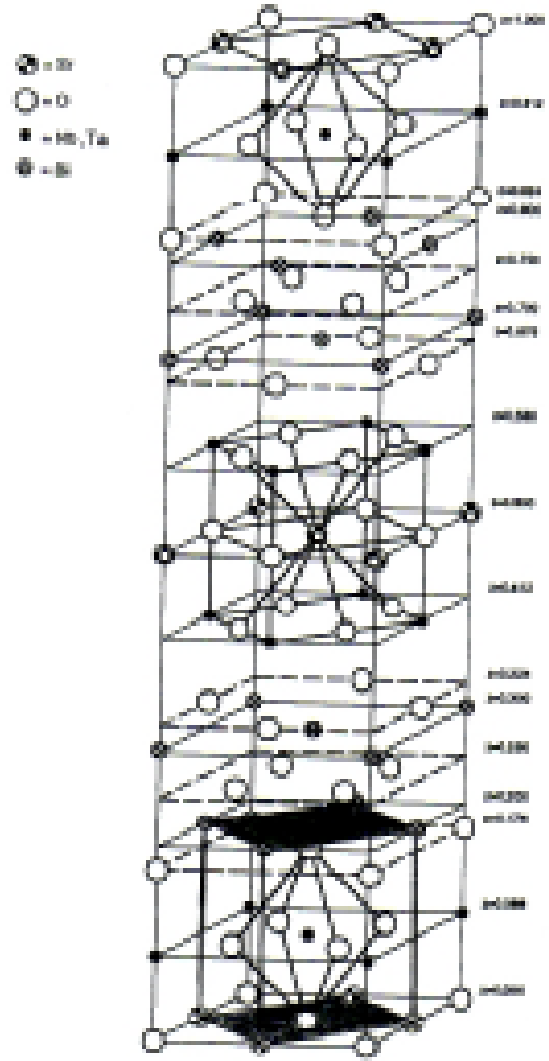
Crystal Structure

$Pb(Zr_{1-x}Ti_x)O_3$(PZT)



Perovskite structure

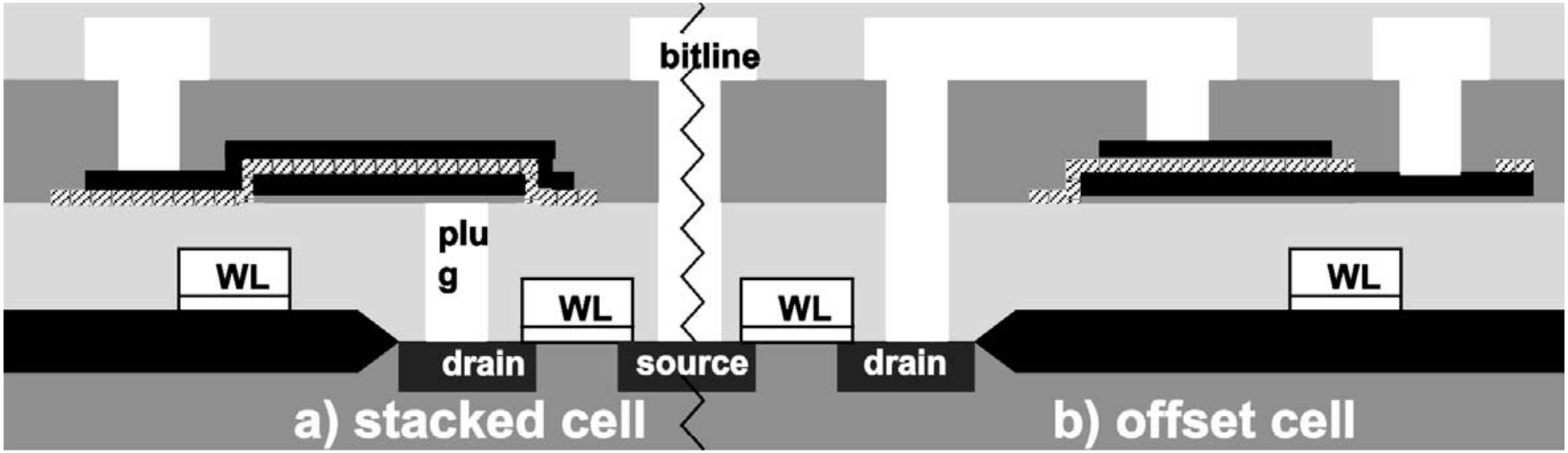
$SrBi_2Ta_2O_9$ or $SrBi_2Nb_2O_9$

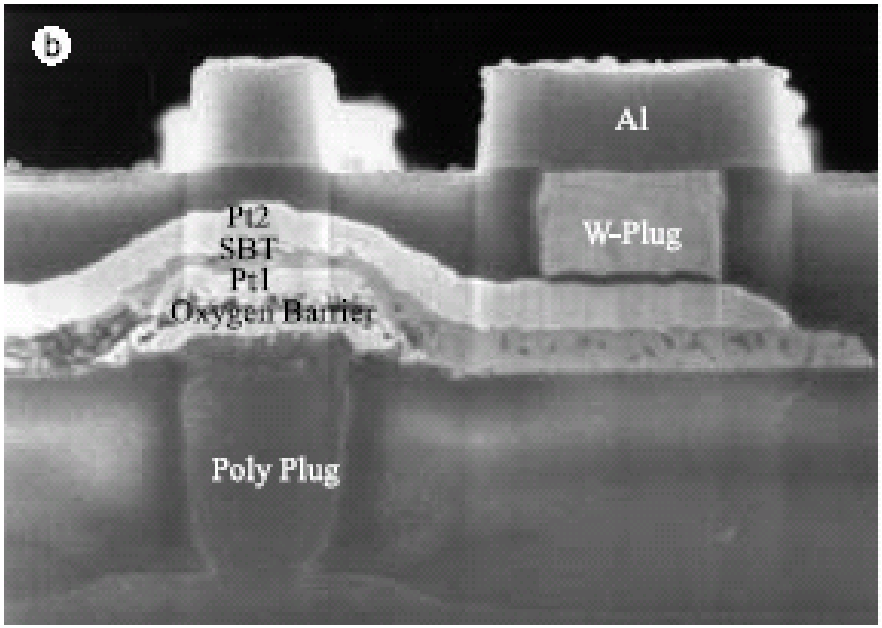


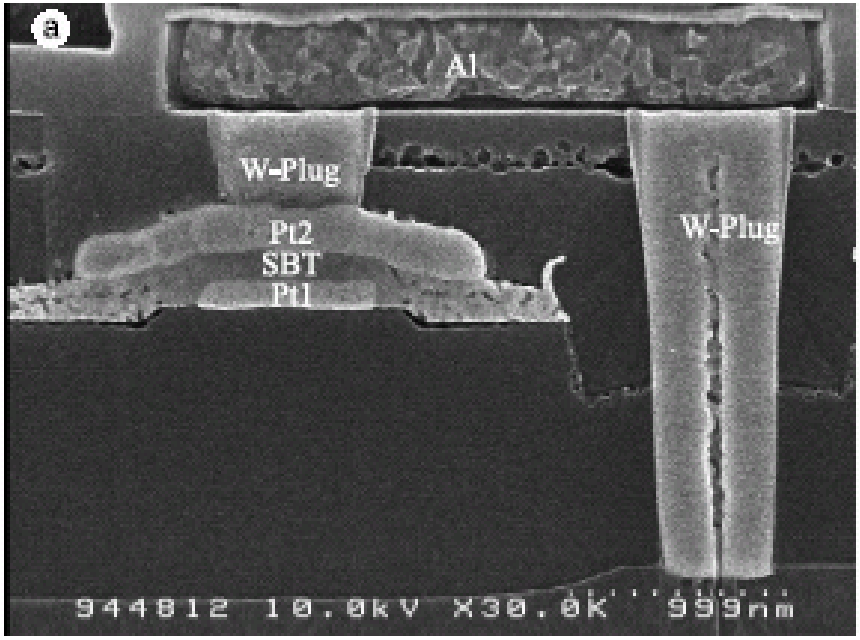
Layered Perovskite

Smith, Ferroelectrics,2009

Capacitor type ferroelectric random access memory(FeRAMs)

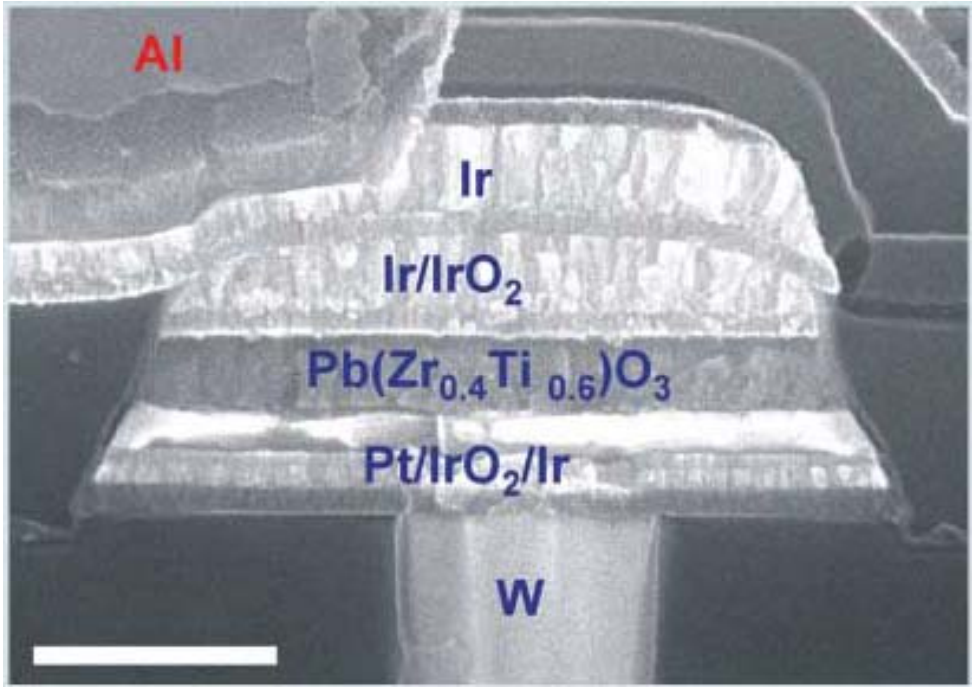






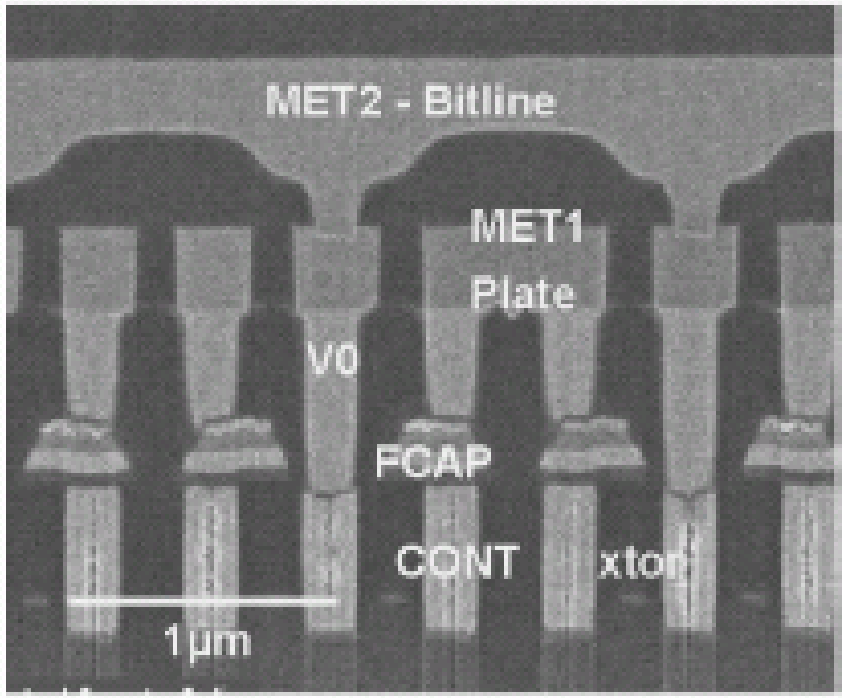
Mikolajick et.al., Microelectronics Reliability,41(2007)947.

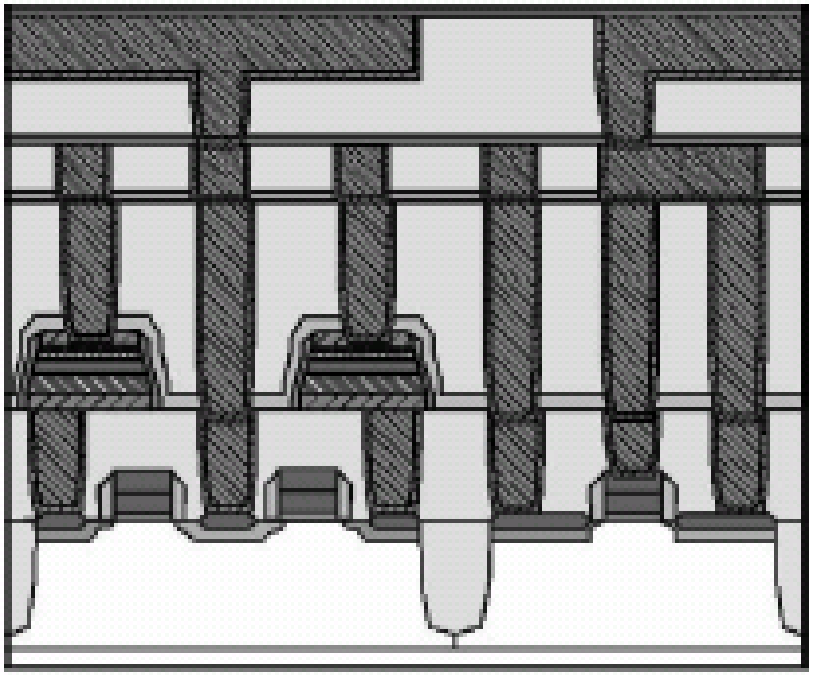
32 Mb Samsung PZT FeRAM



J.F. Scott, Science, Vol.315,954,Feb. 2007

SEM image of embedded FRAM(64 Mb 1T/1C, TI)





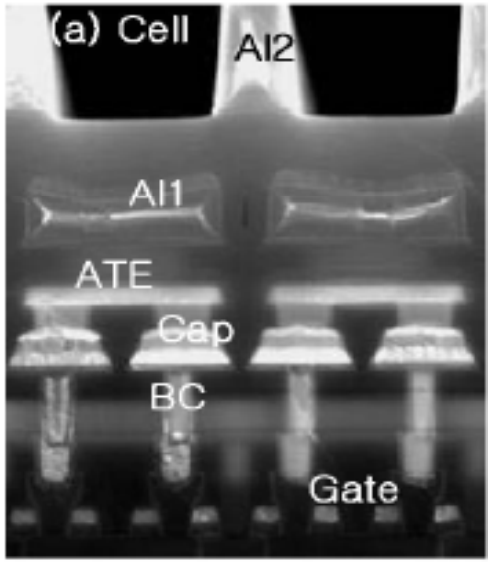
Cross-section schematic diagram(IEEE J. Solid State Circuits, April 2004)

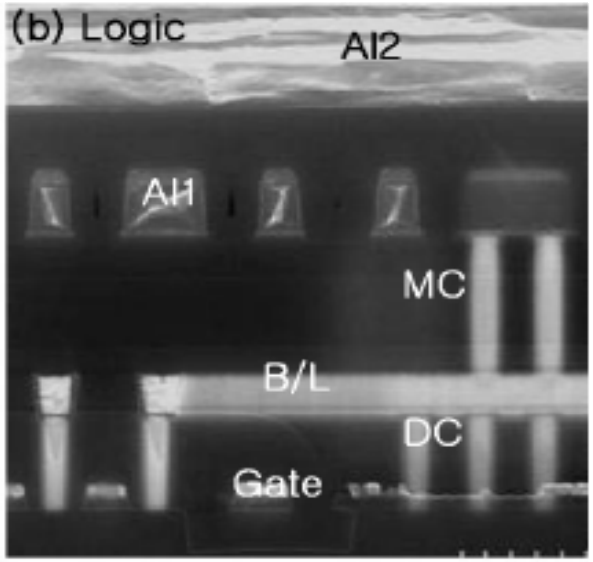
64-Mb eFRAM Device Features

Technology	130 nm, 5LM, Cu/FSG
Organization	2M Words x 32 bits
64Mb Macro Size	56.5 mm^2
Memory Density	1.13 Mb/mm^2
Array Efficiency	64%
Cell Size	0.54 μm^2
Capacitor Size	0.25 μm^2
Cell Type	1T1C, CUB
Architecture	Folded, Twisted Bit-Line
Access / Cycle Time	30 ns / 35 ns
Operating Voltage	1.3 V

IEEE J. Solid State Circuits, April 2004

64 Mb, 1T1C FRAM, Samsung

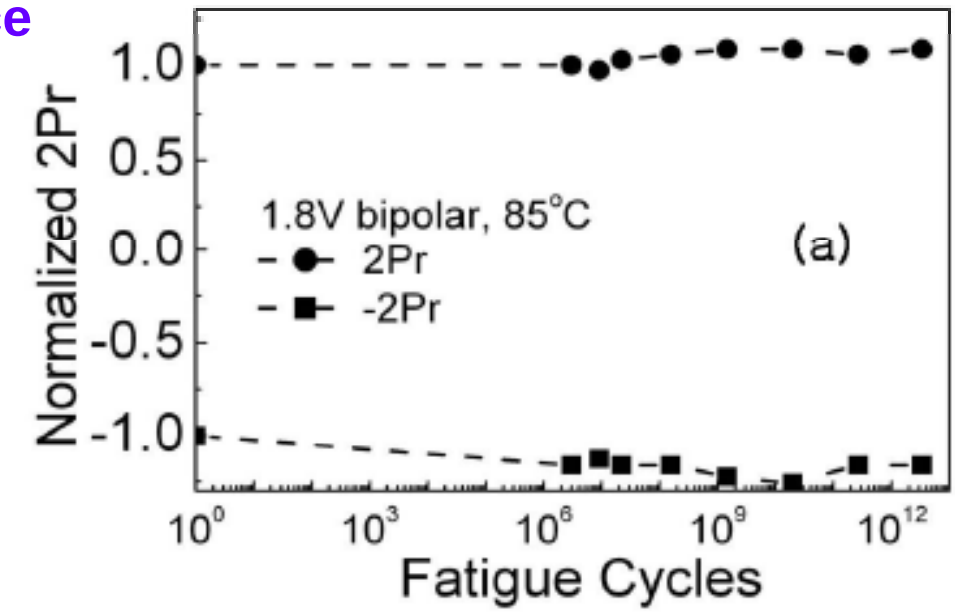




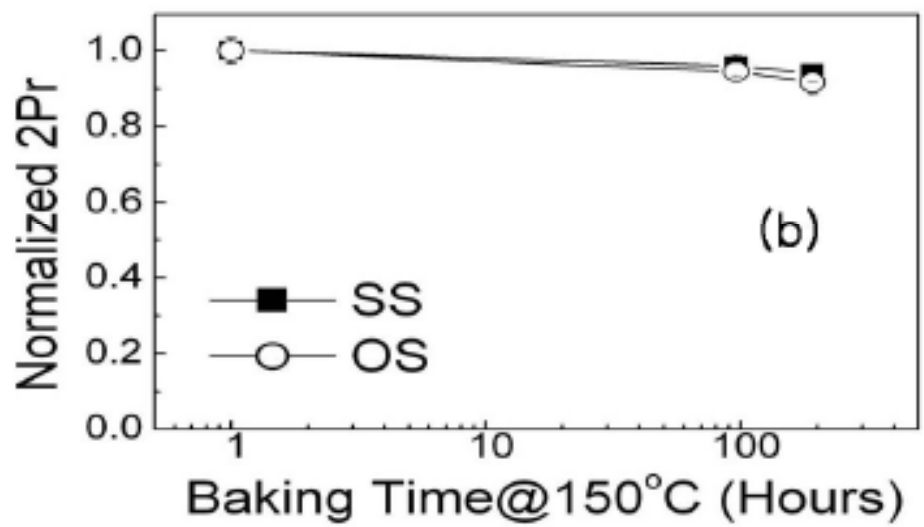
Device	Density	16 I/O x 4Mb
	Voltage	1.8V
	tAA	70ns
	tRC	100ns
	ISB CMOS	<20uA
	Cell Size	0.34um^2
	Cap. Size	0.16um^2
	D/R	150nm
Process	Logic	Dual gate oxide process
	Interconnect	W(DC, BC, MC, Via 1)
	Metallization	3 levels (W, Al1, Al2)
	Capacitor	Ir/SRO/PZT/Ir/TiAlN

2006 IEDM Samsung

Endurance

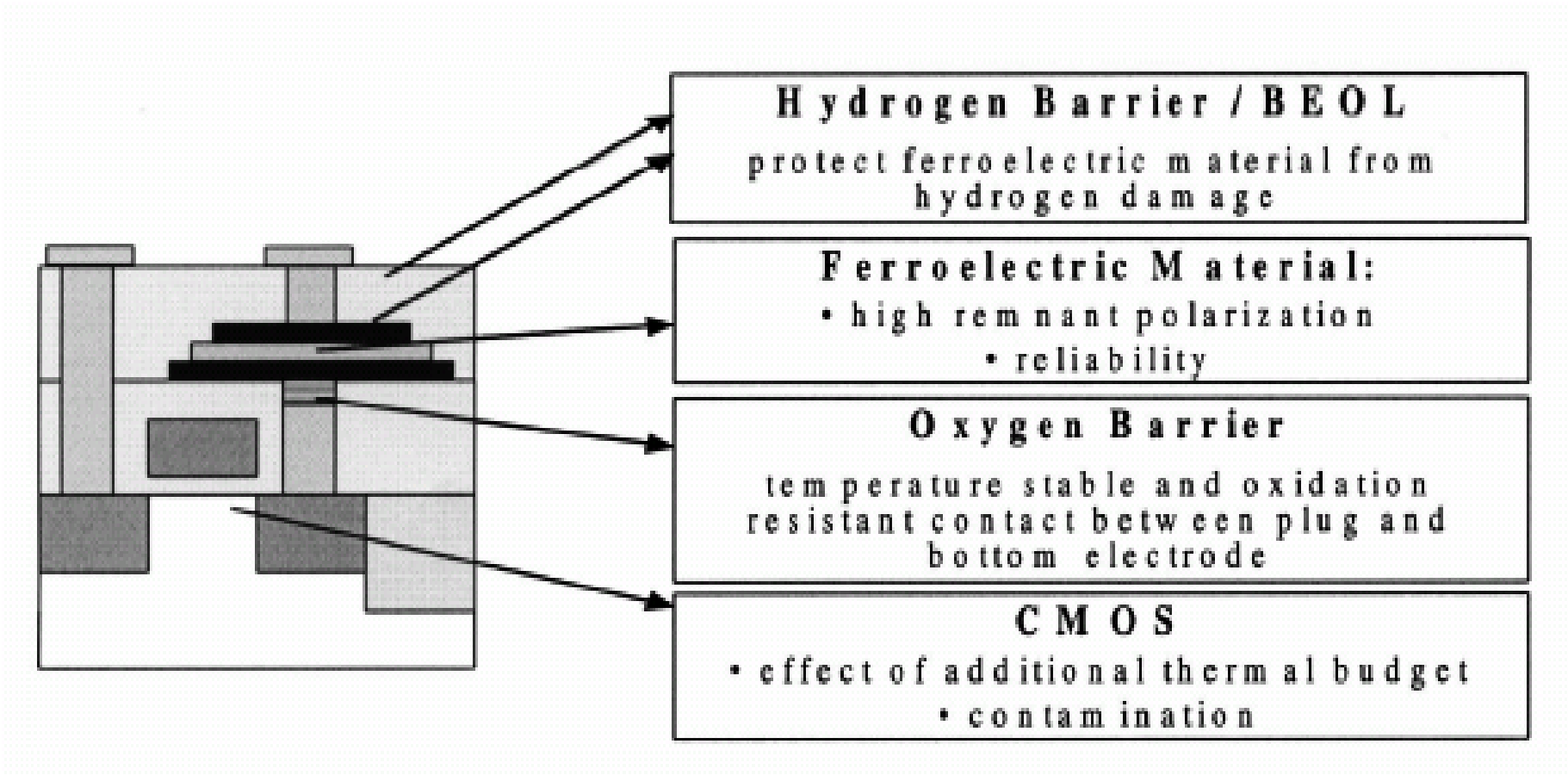


Retention



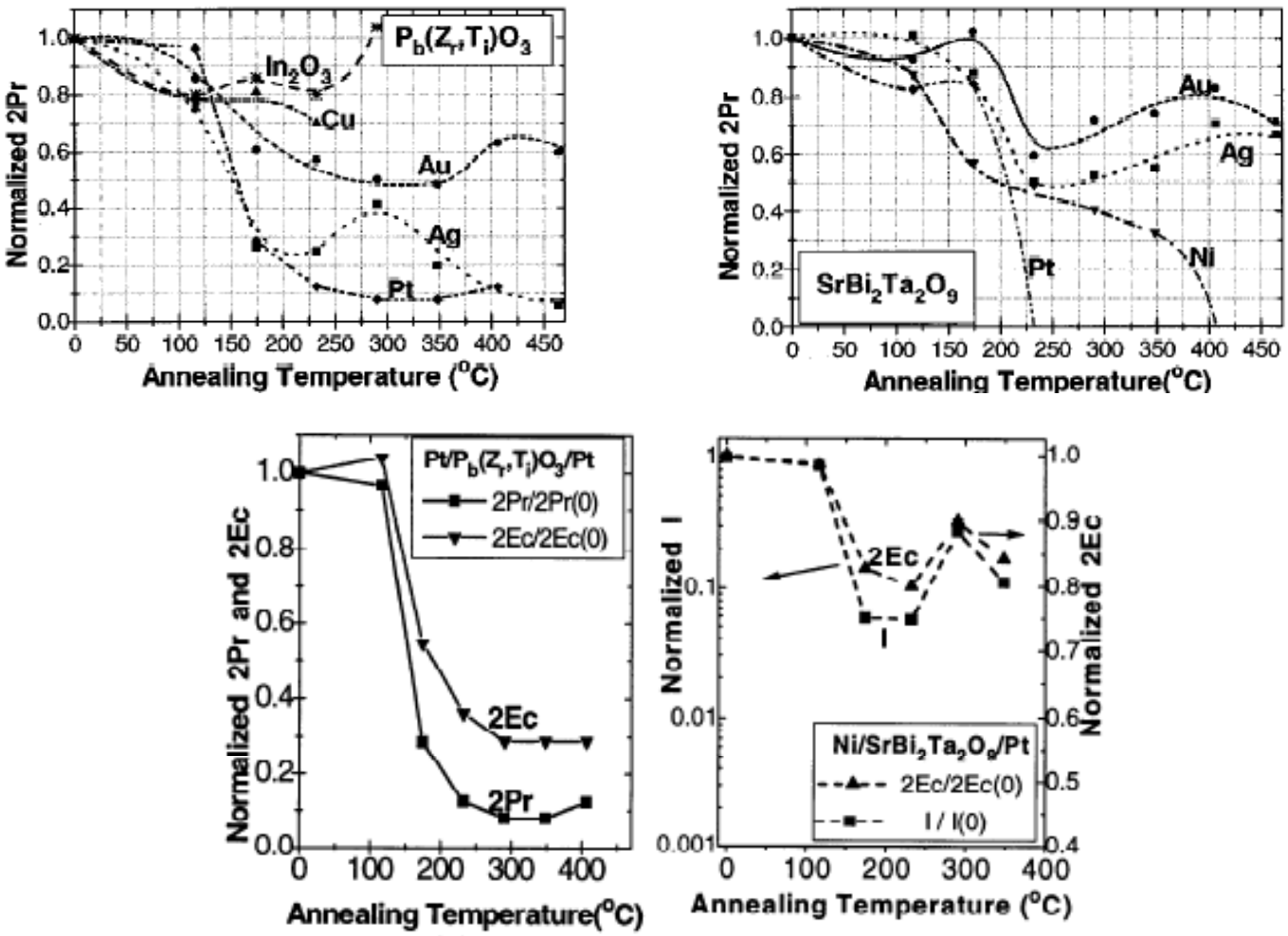
2006 IEDM Samsung

Issues for materials development and Integration



J.Electrochem.Soc.,151, 2004

Forming gas annealing effect



Han and Ma, Appl. Phys. Lett.,71(9),1267,1997

Issue for FeRAMs

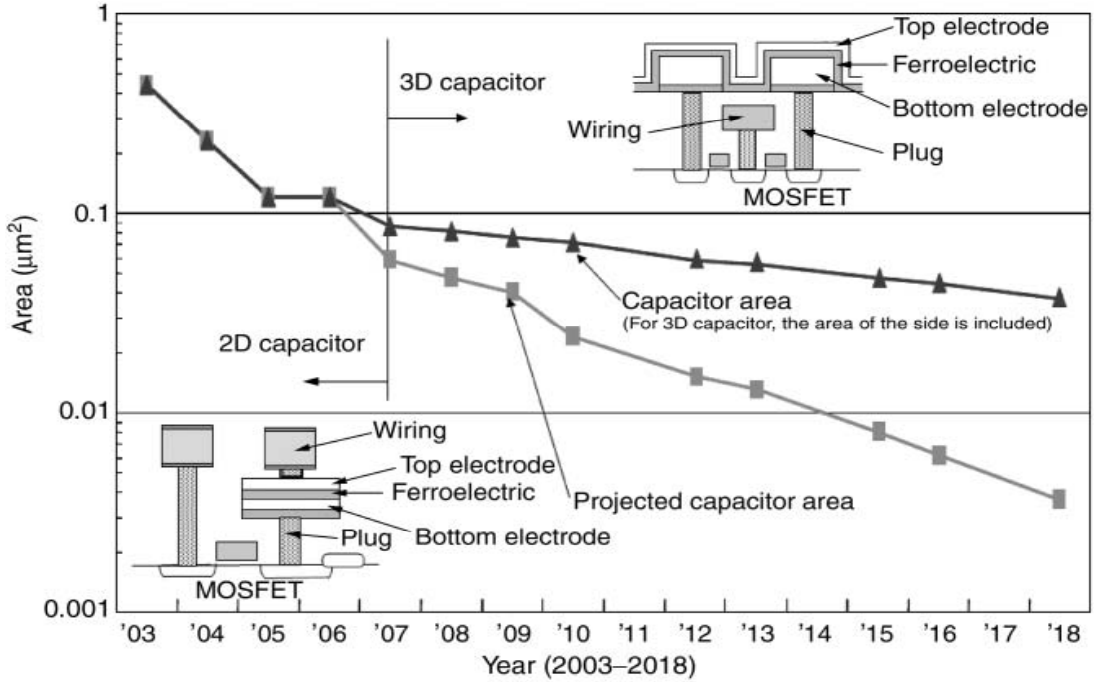
Limiting factor for scaling: minimum 2D capacitor area

Solutions

3D ferroelectric capacitor structures

Conformal coverge of 3-D electrode with ferroelectric has to be uniform in thickness but should also exhibit uniform properties

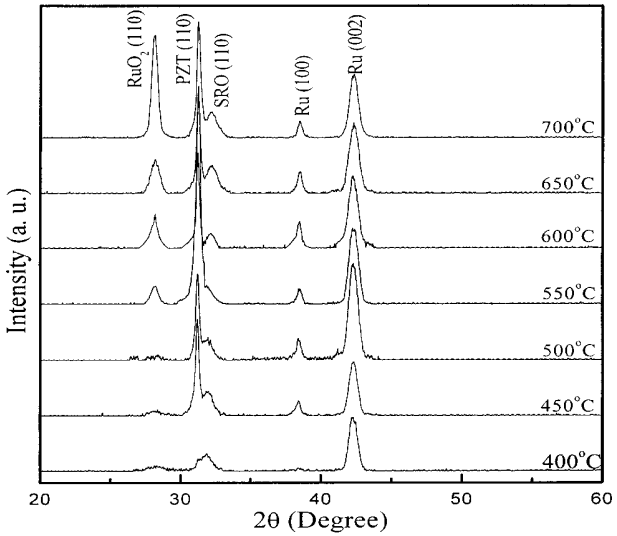
Ferroelectric materials with a higher Pr

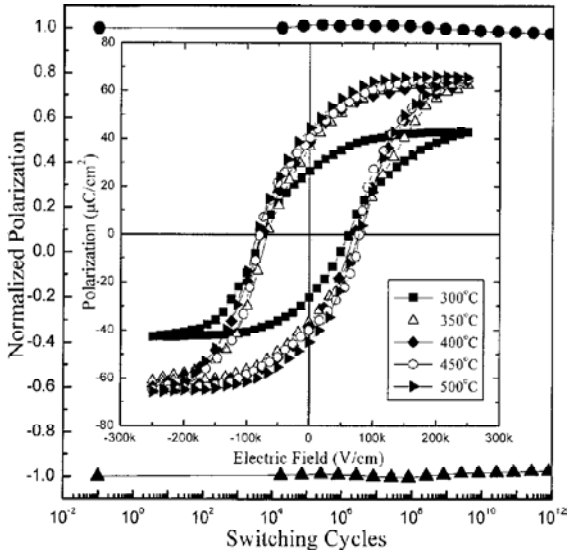


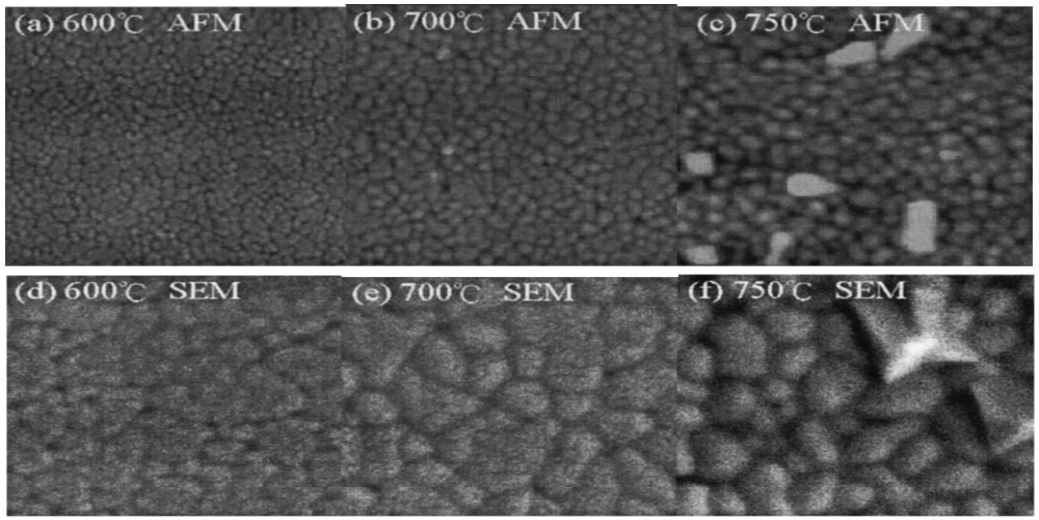
Ishiwara et.al., MRS Bull.,825,2004

PZT with high P_r

PZT/$SrRuO_3$/Ru/SiO_2/Si







Wang et.al. **NCTU**,Appl.Phys.Lett.,80(20),3790,2002

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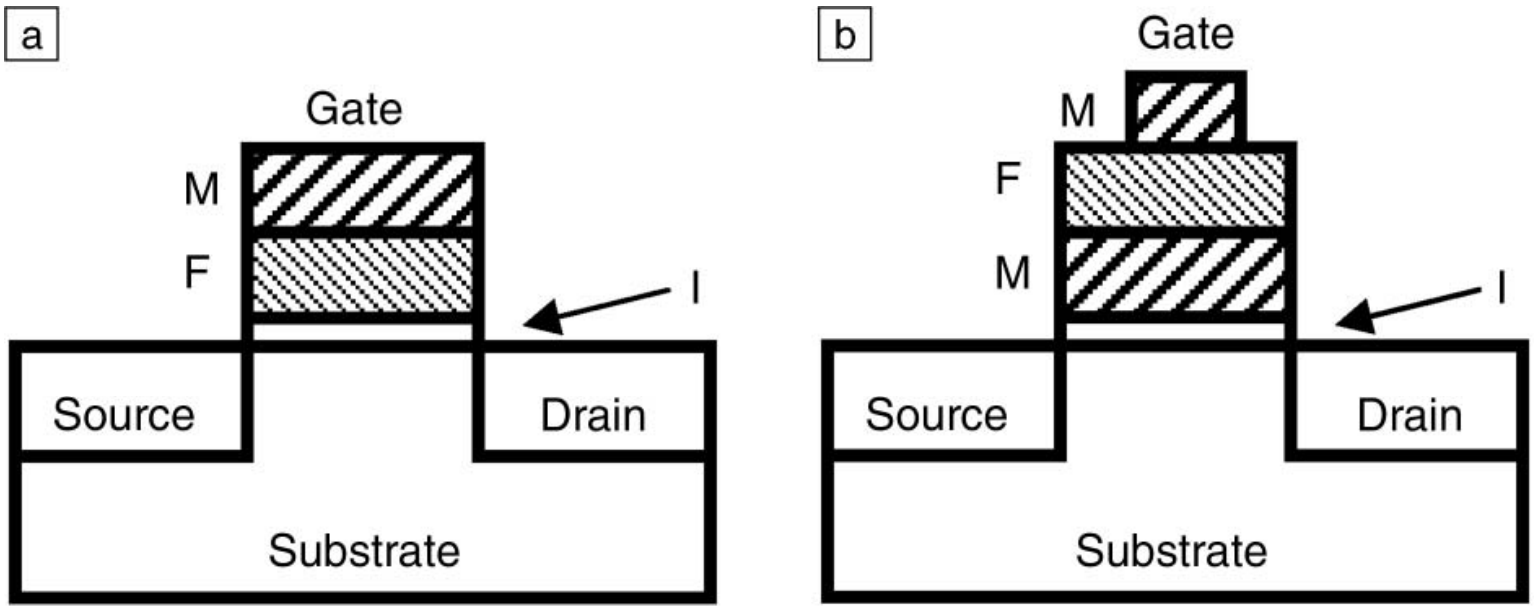
Ferroelectric Gate Field-Effect Transistors(FETs)

Ferroelectric is in direct contact with the drain-source channel of the transistor
resistive storage readout device(non-destructive)

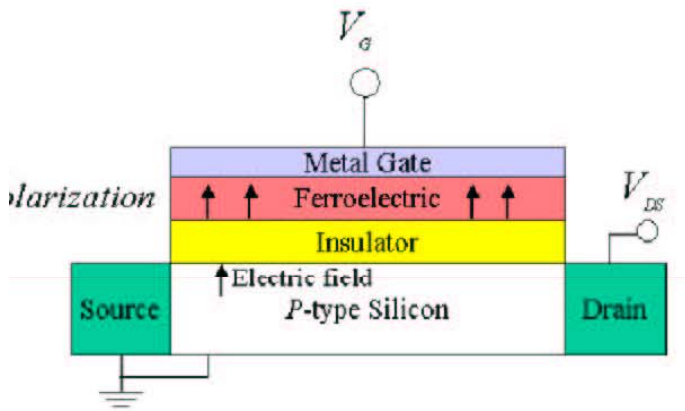


MFIS FETs

MFMIS FETs

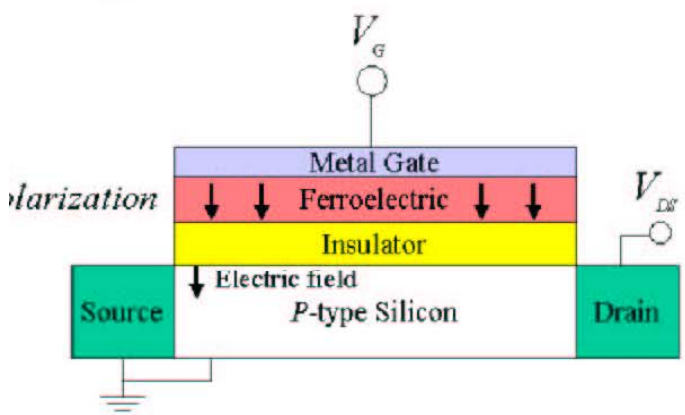
H. Ishiwara et.al.,MRS Bull.,823,2004

Operation principle of Ferroelectric Gate FET



(a) OFF state (Logic 0)

After writing at $-V_w$
the polarization is stored in the ferroelectric.
The electric field cause accumulation of holes,
Therefore the threshold voltage V_{th} is larger.



(b) ON state (Logic 1)

After writing at $+V_w$
The polarization is stored in the ferroelectric.
The electric field cause inversion of electrons,
Therefore the threshold voltage V_{th} is lower.

Lue & Tseng. NCTU

Short achieveable retention time

Reported Data Retention Time for Various Ferroelectric Gate Field-Effect Transistors.

Structure	Material	Area Ratio (MFM:MIS)	Data Retention Time	Year
MFMIS	$Pt/Sr_2(Ta,Nb)_2O_7/Pt/IrO_2/poly\text{-}Si/SiO_2/Si$	1:3.12	14 days (capacitor)	1999
	$Pt/SBT/Pt/SrTa_2O_6/SiON/Si$	1:5.9	2 days	1999
	$Pt/Pb_5Ge_3O_{11}/Ir/poly\text{-}Si/SiO_2/Si$	1:1	4 days	2002
MFIS	$Pt/SBT/Si_3N_4/Si$	1:1	3 days	2002
	$Pt/SBT/Si_3N_4/SiO_2/Si$	1:1	0.5 days	2002
	$Pt/SBT/HfAlO/Si$	1:1	12 days	2004
	$Pt/SBT/HfO_2/Si$	1:1	30 days	2004

MFM – metal–ferroelectric–metal.
MIS – metal–insulator–semiconductor.
MFMIS – metal–ferroelectric–metal–insulator–semiconductor.
MFIS – metal–ferroelectric–insulator–semiconductor.

H. Ishiwara et.al.,MRS Bull.,823,2004

Issues for ferroelectric gate FETs

Ferroelectric Si interface reaction during fabrication leading to create defects at the interface.

Interface traps can capture and or emit charge carriers and affect the operation of the device.

Solutions

Insulating buffer layers inserted between ferroelectric film and Si.

The insulating layer must fulfill the following requirements:

- Form a good interface with silicon.
- Have a strong barrier property against interdiffusion.
- Have a high dielectric constant to realize low operating voltage and long retention time.
- Keep low leakage currents through the device.
- Enhance the crystallization of the ferroelectric film.
- Remain smoothness during the fabrication process.
- Maintain stable at processing temperature.

Materials used as the buffer layer

SiO_2 Si_3N_4 SiON CeO_2 ZrO_2 MgO Al_2O_3 $SrTiO_3$ Y_2O_3 PrO_x $LaAlO_3$

La_2O_3 Ta_2O_5 HfO_2 $SrTa_2O_6$ $YMnO_3$ Bi_2SiO_5

Resistive random access memory (RRAM)

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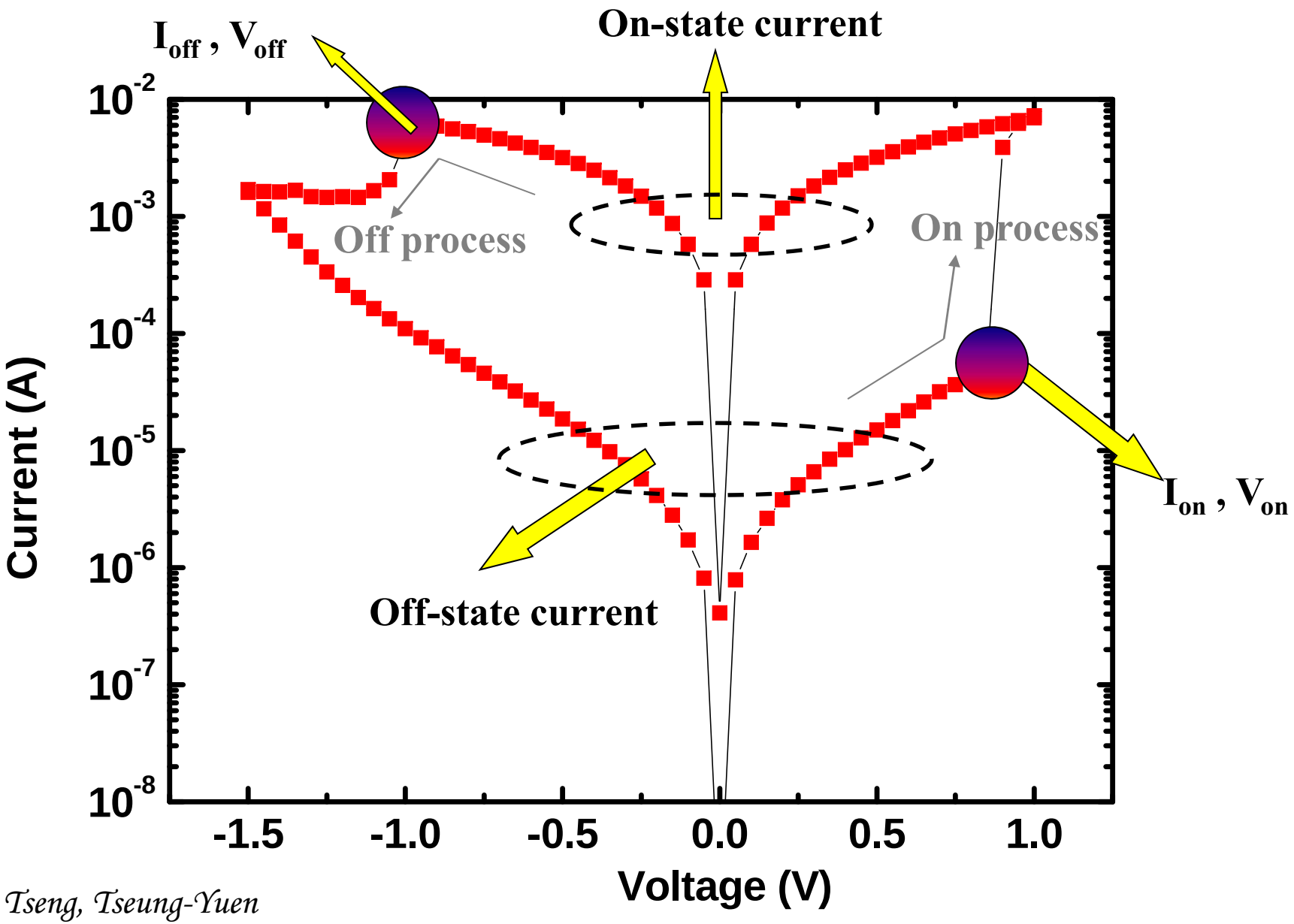
Bipolar resistive switching



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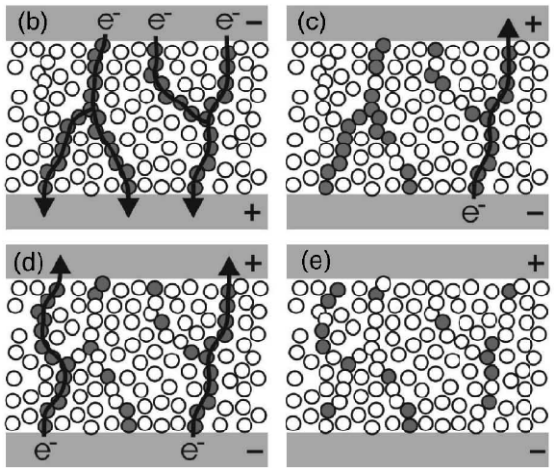
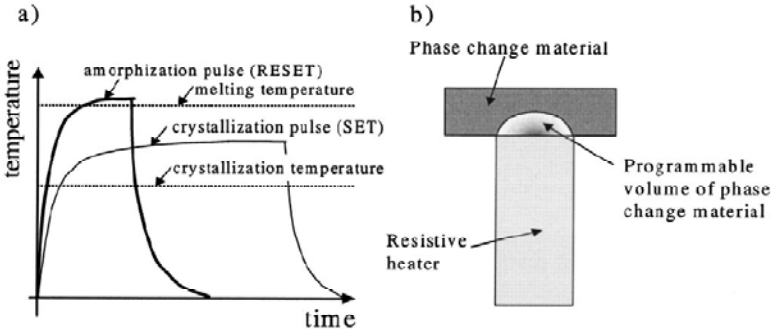
RRAM switching mechanisms

- **Filamentary**

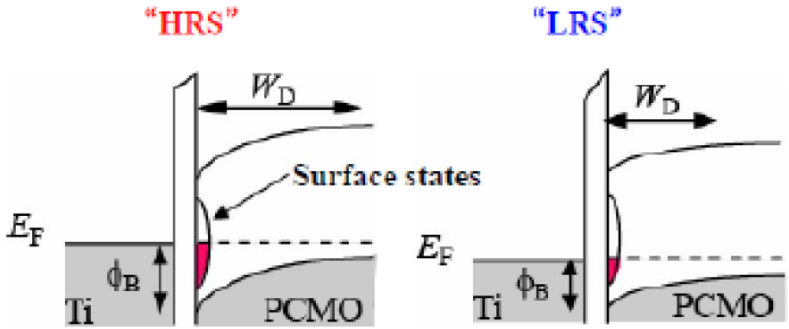


- **Phase change**



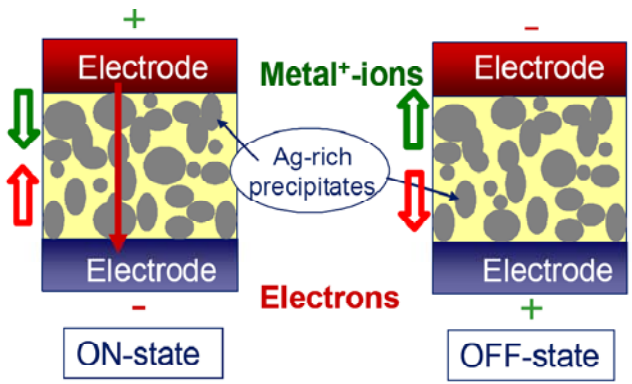
- S.Lai et al., IEDM (2001)

- **Interface controlled**



- M. Kawasaki et al., SSDM (2006)

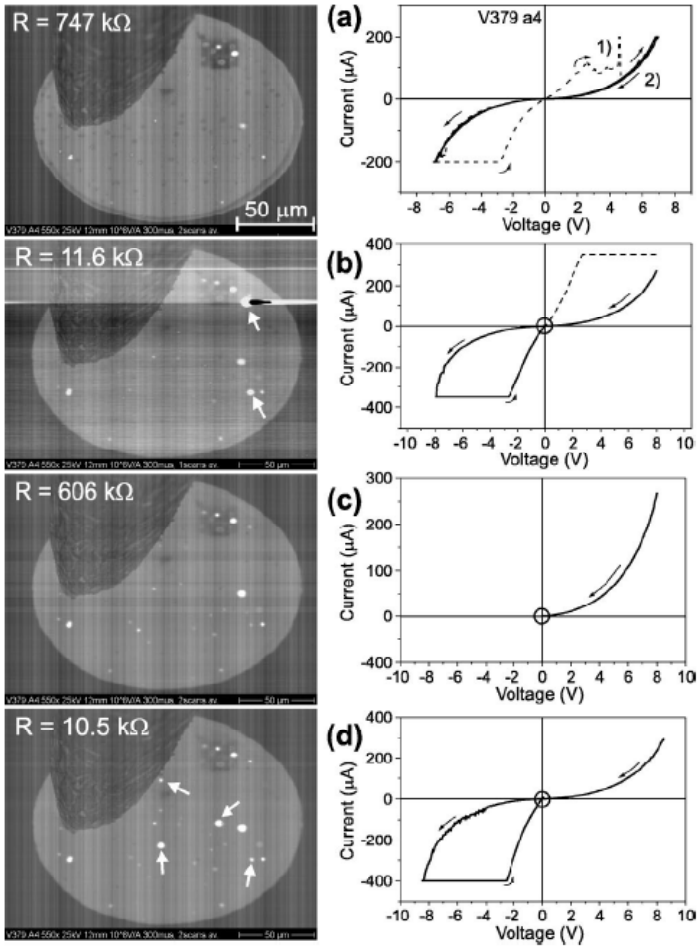
- **Solid-state electrolyte**

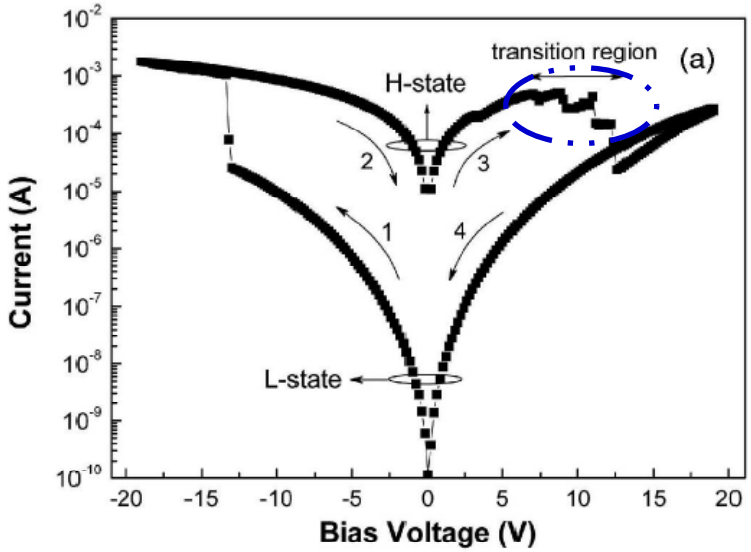


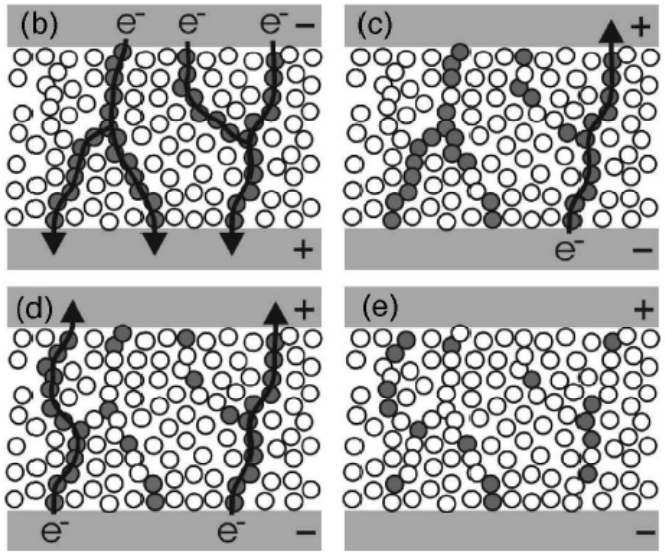
- M. Kund et al., IEDM (2005)

Formation/Rupture of conduction path

EBIC







2001 JAP Rossel et al. **IBM**
2006 EDL Lin et al. **NCTU**

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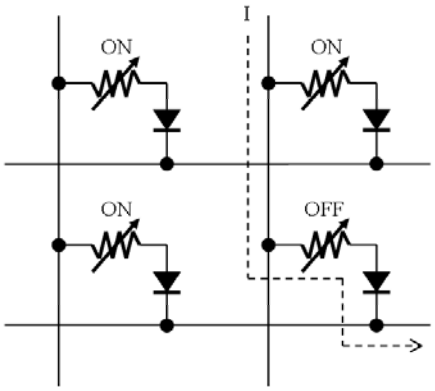
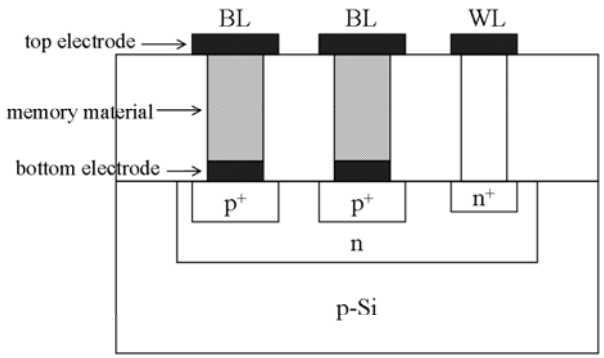
Structure of RRAM

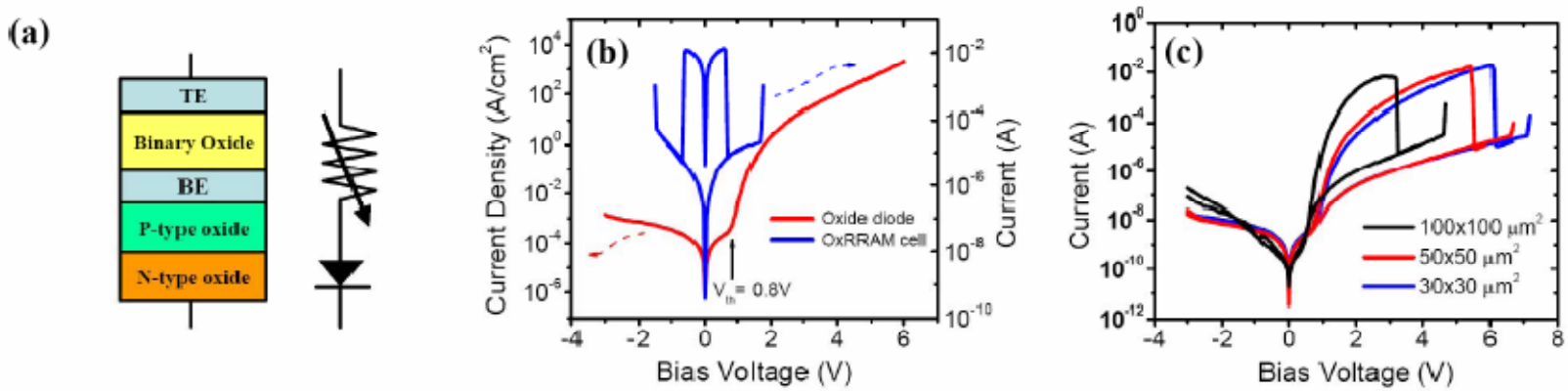
One Diode and One Resistor (1D1R)

- Avoiding the misread problem
- Minimum cell size of $4F^2$
- Diode fabricated in the front-end, and the resistor fabricated in the back-end of CMOS process





2003 IEDM Sezi et al. **Sharp**

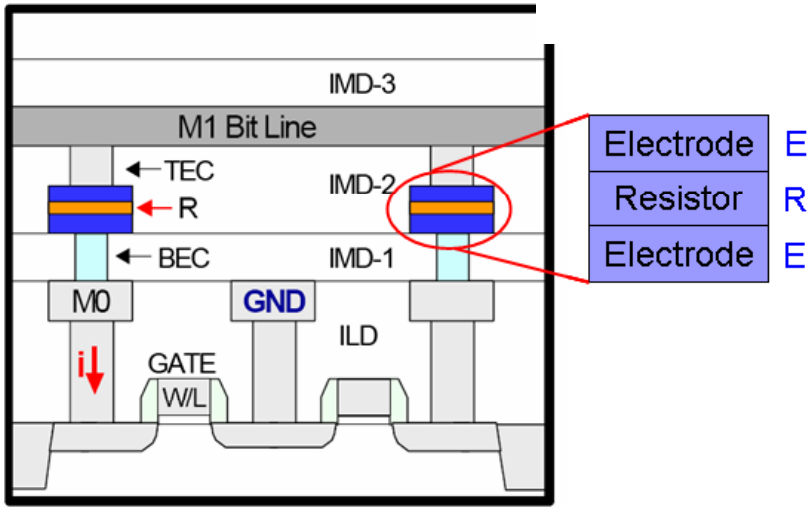


2005 IEDM Baek et al. **Samsung**

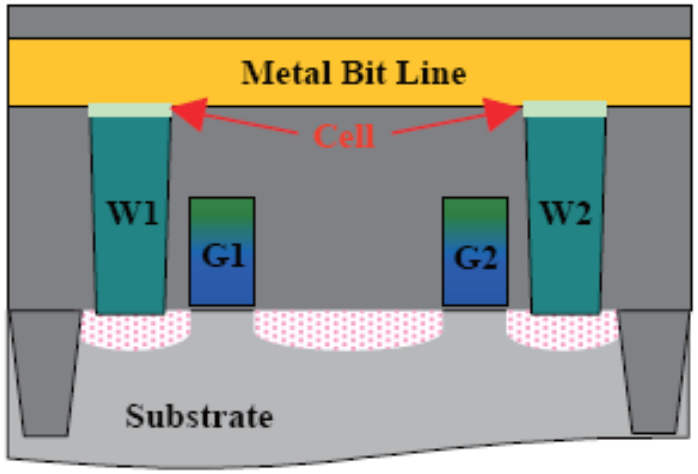
Structure of RRAM

One transistor and one resistor (1T1R)

- Minimum cell size of $6F^2$ (common source)
- Transistor fabricated in the front-end, and the resistor fabricated in the back-end of CMOS process



2004 IEDM Baek et al. **Samsung**



2007 VLSI-DT Ho et al. **MXIC**

Materials for RRAM

Thin Film Technologies	Insulating Materials
(RF) magnetron sputter	Al_2O_3, $SrZrO_3$, Cr:$SrZrO_3$, V: $SrZrO_3$, ZrO_2, CeO_2, TiO_2, CuO, SiO_2, Cr:$SrTiO_3$, $La_{0.7}Ca_{0.3}MnO_3$, Eu_xO_y
(RF) reactive magnetron sputter	NiO, TiO_2, ZrO_2, ZrO_x, Cu_2O, CuC
(DC) magnetron sputter	NiO
(DC) reactive magnetron sputter	NiO, TiO_2
Reactive magnetron sputter	TiO_2, MnO_x, ZnO, $La_{0.7}Ca_{0.3}MnO_3$
PLD	NiO, TiO_2, HfO_2, Cu_2S, (BaSr)(ZrTi)O, $SrRuO_3$, $YBa_2Cu_3O_{6+x}$, $Ba_{0.7}Sr_{0.3}TiO_3$, $SrTiO_3$, $SrTiO_x$, Cr:$SrZrO_3$, $La_{0.67}Ca_{0.33}MnO_3$, $La_{0.7}Ca_{0.3}MnO_3$, $La_{0.7}Ca_{0.3}MnO_3$, $Pr_{0.7}Ca_{0.3}MnO_3$, $La_{0.67}Sr_{0.33}MnO_3$, $La_{0.7}Sr_{0.3}MnO_3$, $La_{0.8}Sr_{0.2}MnO_3$
ALD	NiO, HfO_x, HfO_2
Reactive magnetron sputter	TiO_2, MnO_x, ZnO, $La_{0.7}Ca_{0.3}MnO_3$
PLD	NiO, TiO_2, HfO_2, Cu_2S, (BaSr)(ZrTi)O, $SrRuO_3$, $YBa_2Cu_3O_{6+x}$, $Ba_{0.7}Sr_{0.3}TiO_3$, $SrTiO_3$, $SrTiO_x$, Cr:$SrZrO_3$, $La_{0.67}Ca_{0.33}MnO_3$, $La_{0.7}Ca_{0.3}MnO_3$, $La_{0.7}Ca_{0.3}MnO_3$, $Pr_{0.7}Ca_{0.3}MnO_3$, $La_{0.67}Sr_{0.33}MnO_3$, $La_{0.7}Sr_{0.3}MnO_3$, $La_{0.8}Sr_{0.2}MnO_3$
ALD	NiO, HfO_x, HfO_2
Plasma-enhanced ALD	TiO_x, TiO_2,
Liquid injection ALD	TiO_x, $La_{0.83}Sr_{0.17}MnO_3$
MOCVD	NiO, ZnO, HfO_2
Laser MBE	NiO heterostructured nanowires
Electron beam evaporation	NiO, TiO_2, Au:ZrO_2, Zr^+: ZrO_2, Cu: ZrO_2, ZrO_2/Au/ ZrO_2, MnO_x, SiO_x
Sol-gel	V: $SrZrO_3$, ZrO_2, Ag- ZrO_2, TiO_2, Gd:TiO_2, $Mg_{0.2}Zn_{0.8}O$,
RTA	NiO
Anodic oxidation	TiO_2
Thermal oxidation	Cu_2O, Cu_xO, FeO_x
Plasma oxidation	Al_xO_y

Electrode Materials for RRAM

Thin Film Technologies	Electrode Materials
(RF) magnetron sputter	Pt, $LaNiO_3$, Ti, WN, $SrRuO_3$, ITO, TiN
(DC) magnetron sputter	Pt, Ag, Al, Cu
Reactive magnetron sputter	TiN, Pt
Electron beam evaporation	Pt, Au, Ti, Ni, Cu, Al
Thermal evaporation	Pt, Au, Ti, Al, Cr, Ag
ALD	TiN
PLD	$SrRuO_3$, $YBa_2Cu_3O_{7-\delta}$, Al-Ag

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Factors that influence resistive thin film properties

- Processing methods and parameters
- Film composition and dopant
- Crystalline structure
- Microstructure
- Surface morphology
- Film thickness
- Electrode materials
- Embedded layer

Effect of ZrO_2 processing temperatures

	Forming Voltage (V)	DC sweep			
		On-state current at 0.3V	Off-state Current at 0.3V	On/Off Ratio at 0.3V	Endurance
		mA	μA	times	number of testing cycle
25°C	2.5~4	1.21	33.3	22.8	2200
100°C	4~5	1.95	11.7	110	900
150°C	4~5.5	1.64	5.16	66	4000
200°C	4~5	1.04	4.53	114	10599
250°C	4~6	1.55	14.3	96	6100

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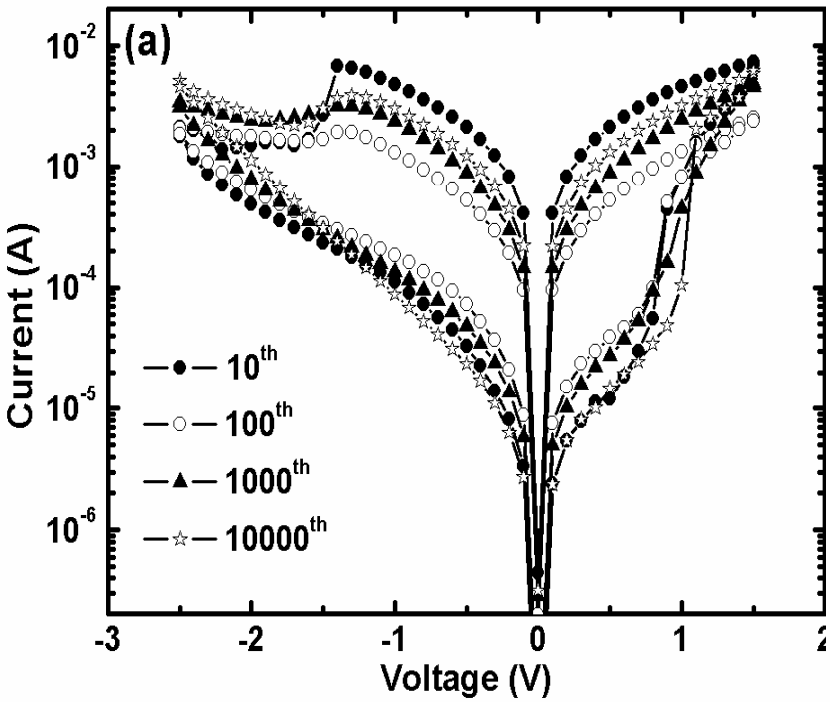
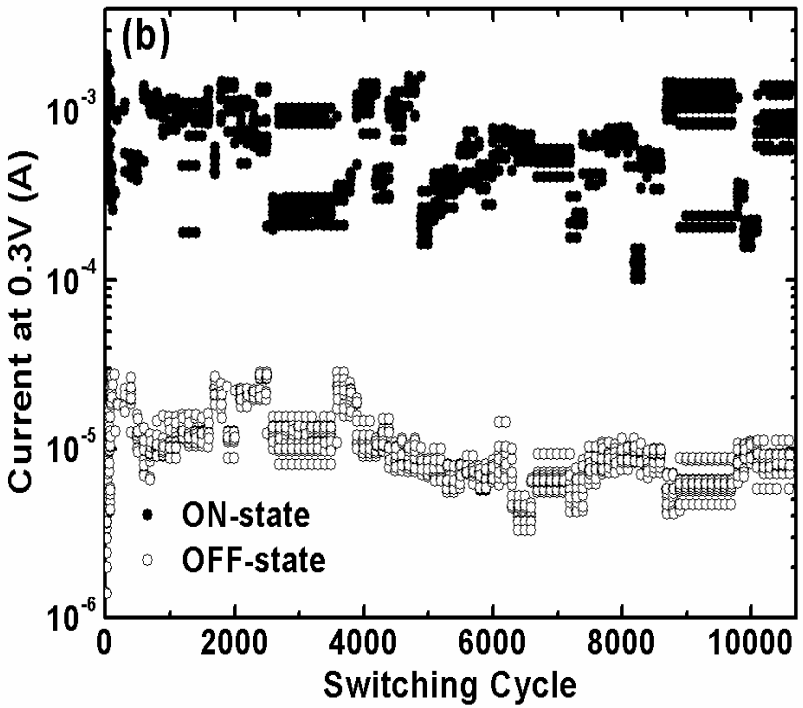
$Ti/ZrO_2(200^oC)/Pt/Ti/SiO_2/Si$

Amorphous phase





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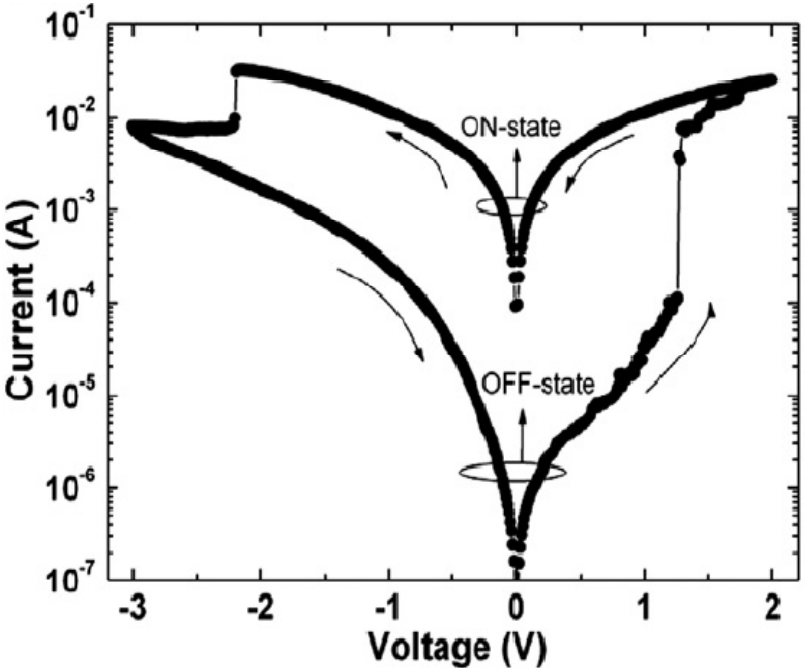
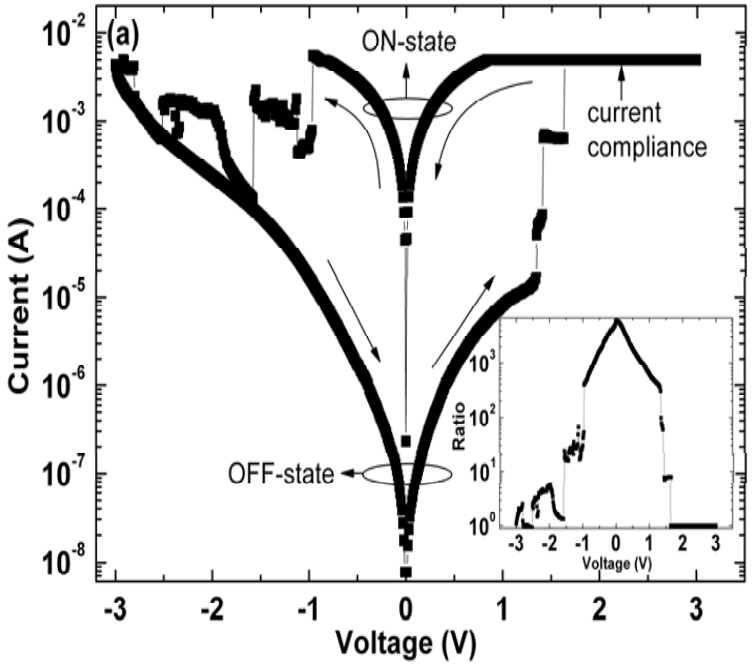
Compositional effect

Ti/ZrO2/Pt



Ti/Al_2O_3/Pt



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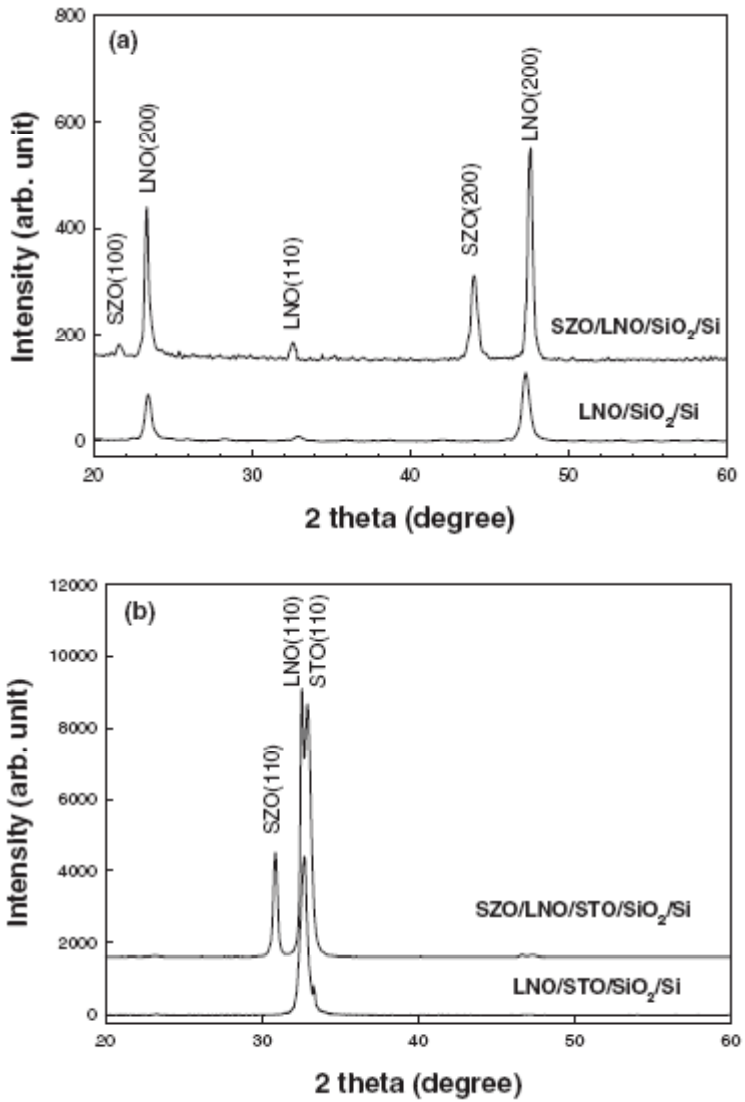
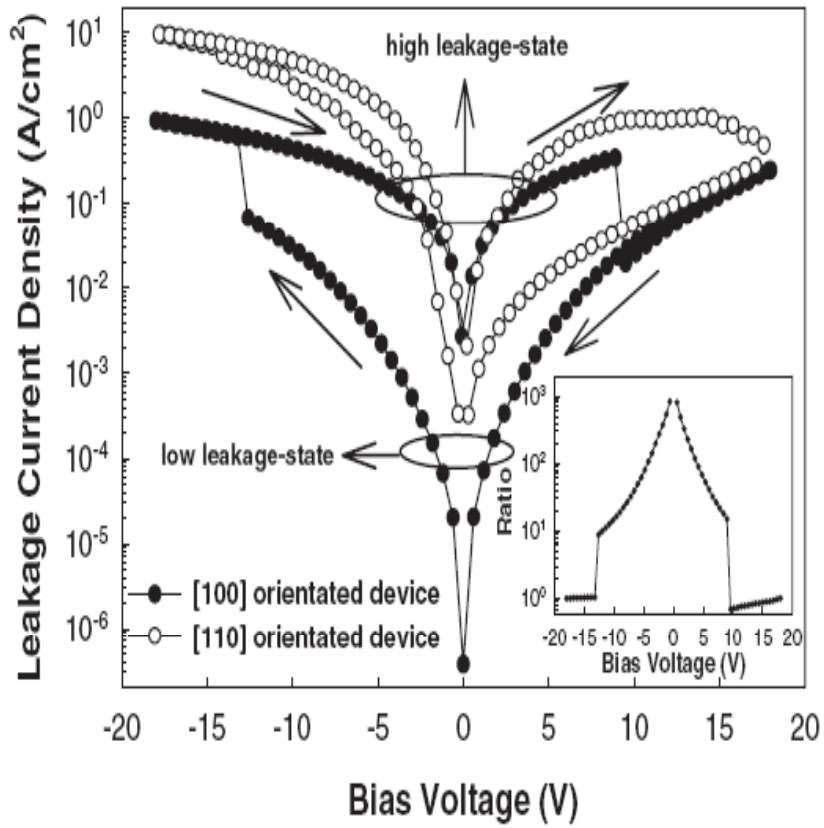
Effect of Crystallinity





Liu & Tseng et.al.JPD, 39, 1156,2006

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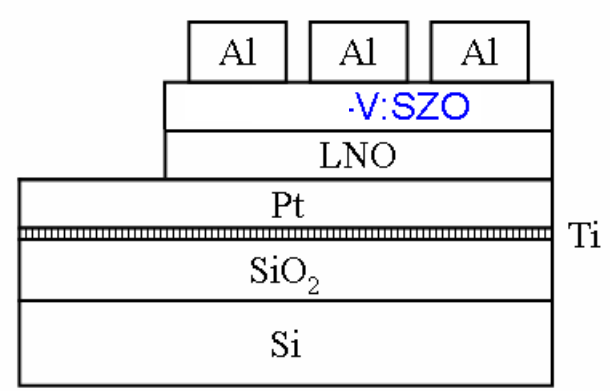
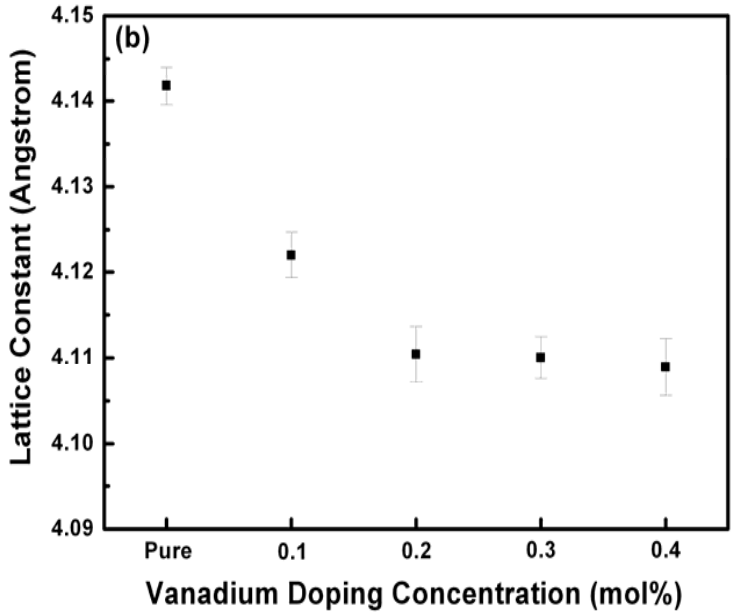
Doping Effect



Device Structure

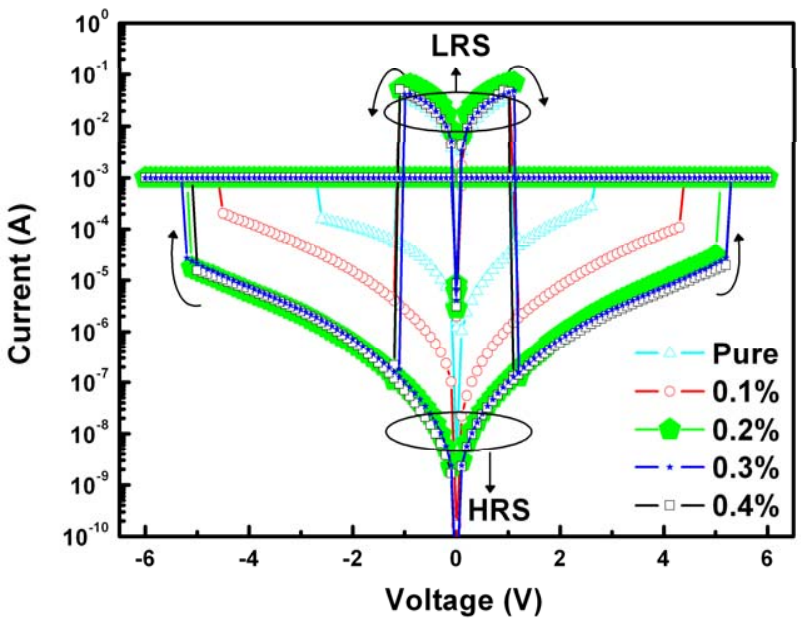


Ionic Radius

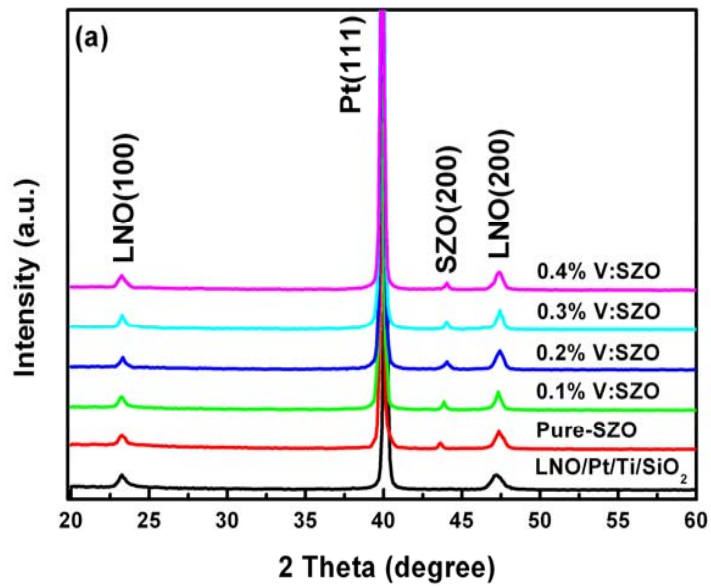
V^{5+}(0.054 Å)

Zr^{4+}(0.072 Å)

Sr^{2+}(0.118 Å)



Tipical I-V Characteristics



XRD patterns of 500°C deposited films

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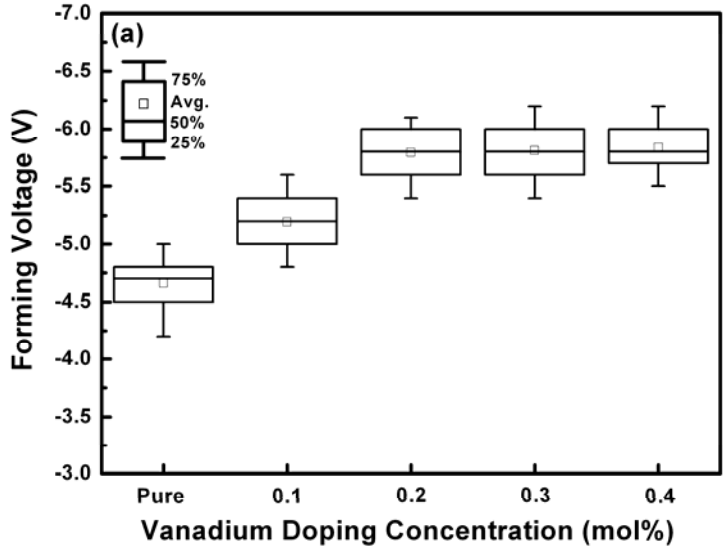
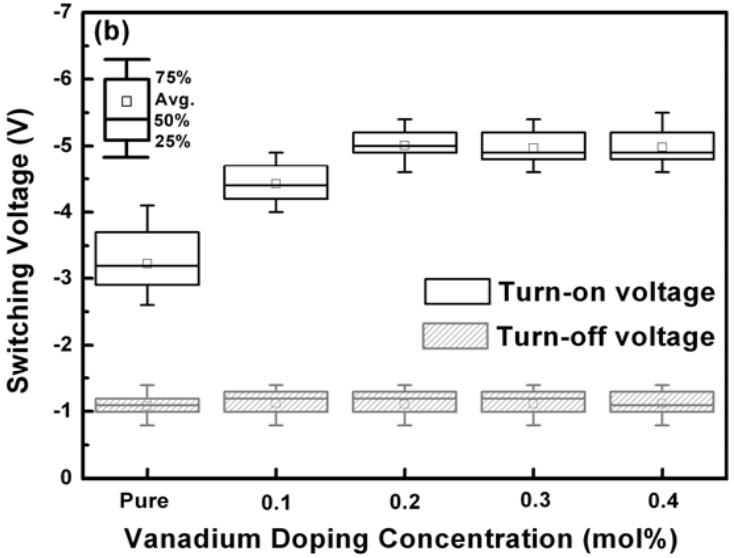
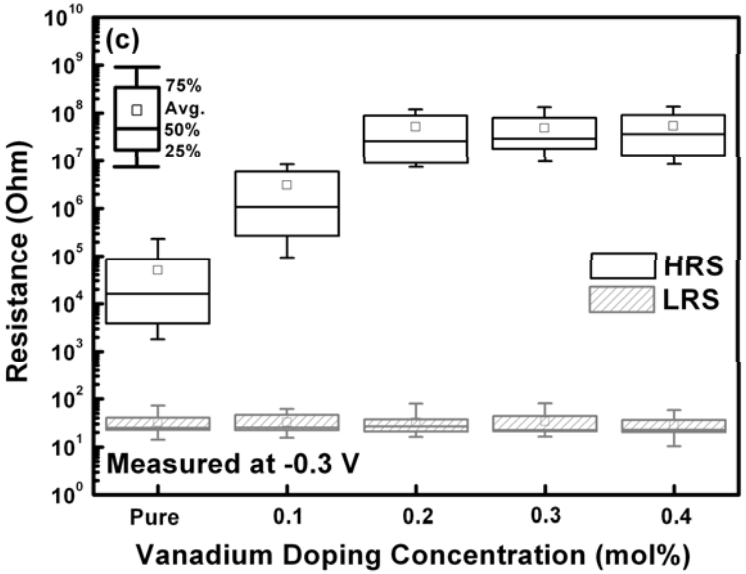
Forming voltage, turn-on voltage, and resistance ratio increase with increasing vanadium doping concentration up to 0.2 mol%, but those of 0.2, 0.3 and 0.4 mol% V:SZO films are almost the same.







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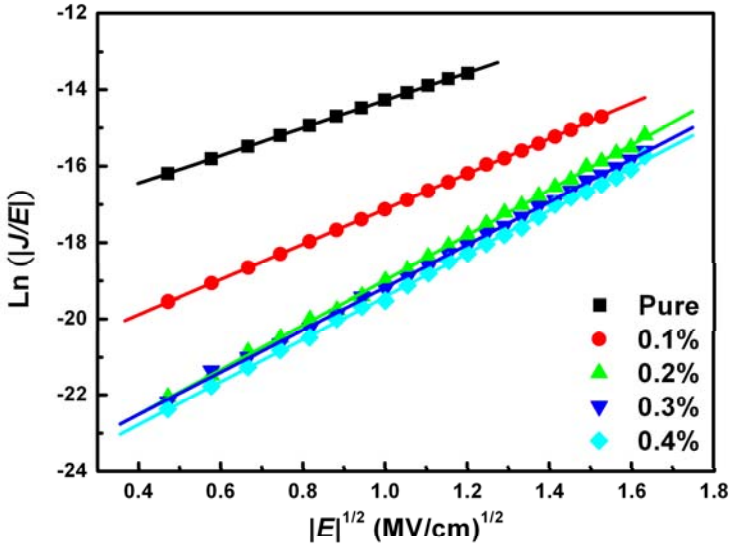
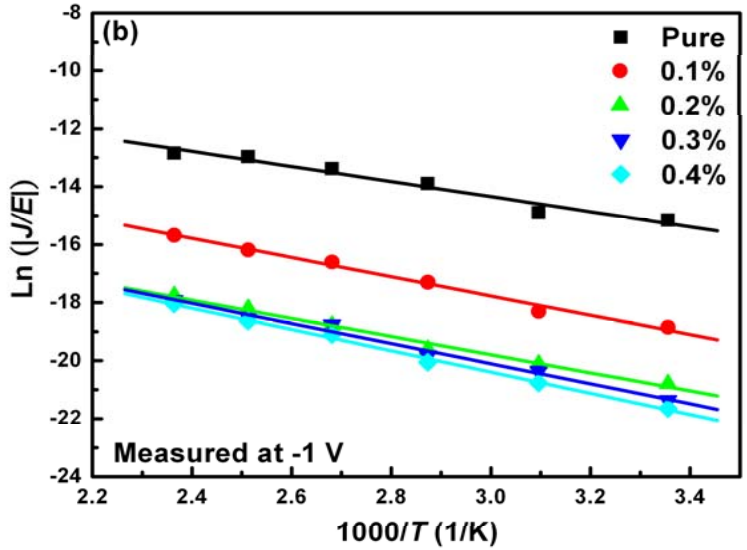
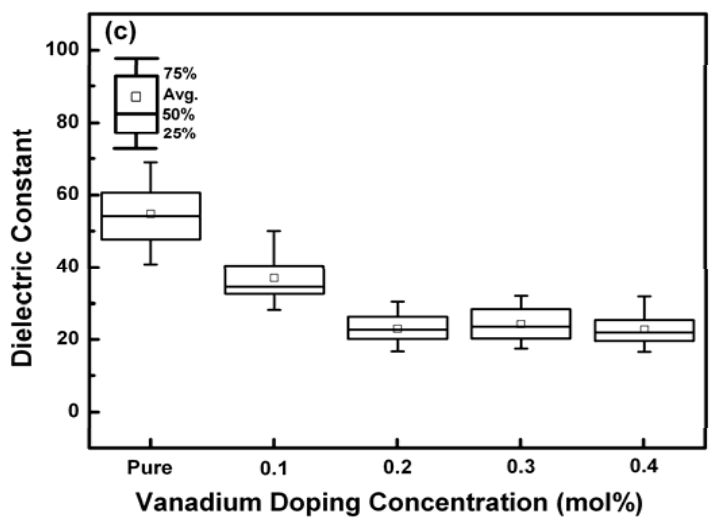




HRS currents: Carrier conduction in films dominated by F-P emission

$$J \sim E \exp\left(\frac{-q(\phi_{B,eff} - \sqrt{qE/\pi\varepsilon_i})}{kT}\right)$$

Temperature dependence of HRS currents



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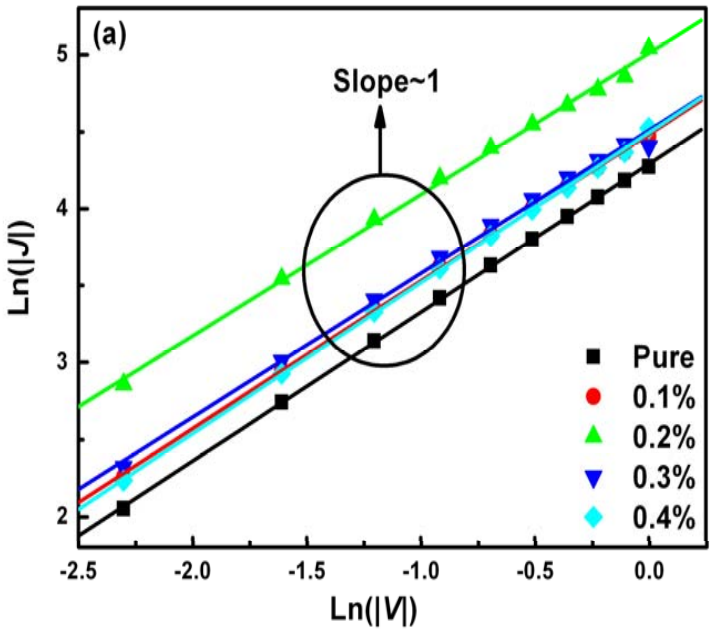

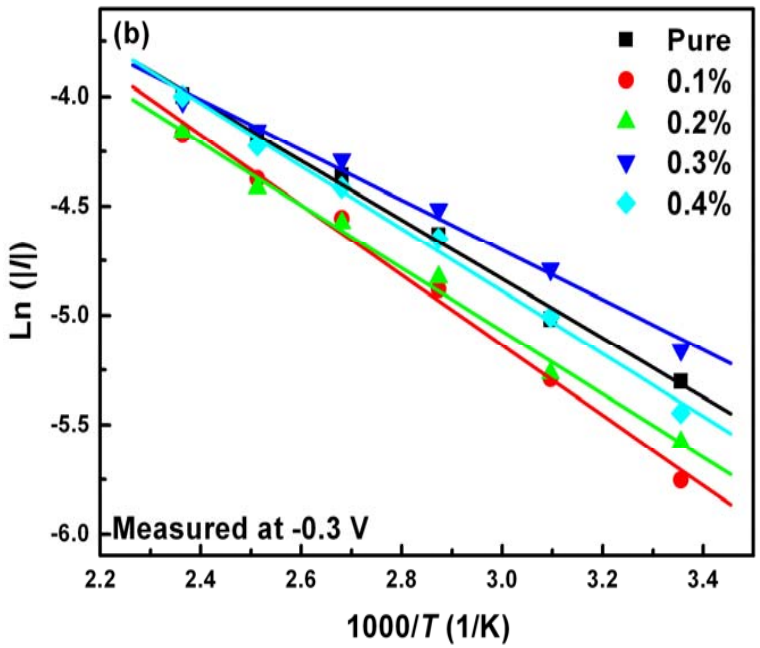

Carrier transport of LRS followed by Ohmic conduction

LRS currents increased with increasing measured temperature(hopping conduction)

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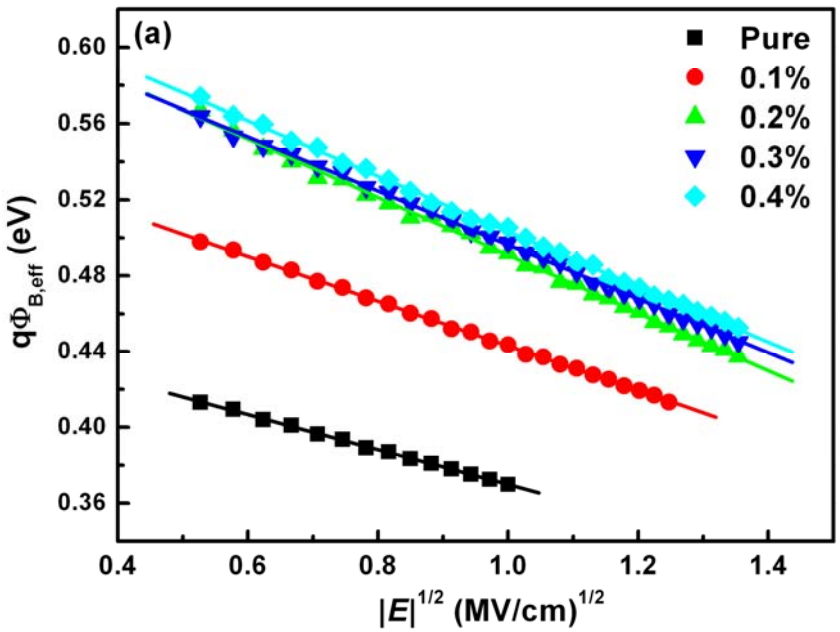

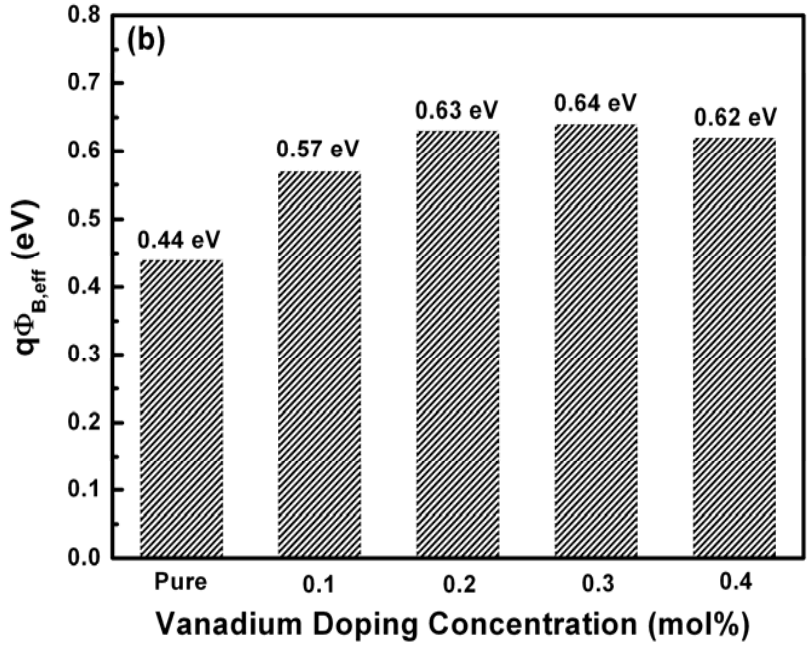

Plots of F-P emissions fitting of HRS currents. By extrapolation of above measurement data to zero electric field, barrier height of F-P defects obtained

Barrier height of F-P defects

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What is F-P defects?

Oxygen vacancies or electronic defects

It is important to identify the effect of vanadium doping on oxygen vacancies occurred in order to obtain better understanding of the effect of vanadium doping on the resistive switching characteristics of the devices

Zr site in the lattice substituted by high valence cation(V^{5+}) can be expressed as the followings:

$$2V_2O_5 \xleftrightarrow{5ZrO_2} 4V_{Zr}^{\bullet} + 10O_o^x + V_{Zr}^{''''}$$

$$ZrO_2 + 2O_o^x \leftrightarrow V_{Zr}^{''''} + 4V_o^{\bullet} + ZrO_2(surface) + O_2(g)\ ,\ K_{Schottky} = \left[V_{Zr}^{''''}\right]\left[V_o^{\bullet}\right]^4 P_{O_2}\ .$$

$$ZrO_2 \leftrightarrow V_{Zr}^{''''} + 2V_o^{\bullet\bullet} + ZrO_2(surface)\ ,\ K_{Schottky} = \left[V_{Zr}^{''''}\right]\left[V_o^{\bullet\bullet}\right]^2 .$$

$$O_o^x \leftrightarrow \frac{1}{2}O_2(g) + V_o^{\bullet} + e'\ ,\ K_{redox} = (P_{O_2})^{\frac{1}{2}}\left[V_o^{\bullet}\right] n$$

$$O_o^x \leftrightarrow \frac{1}{2}O_2(g) + V_o^{\bullet\bullet} + 2e'\ ,\ K_{redox} = (P_{O_2})^{\frac{1}{2}}\left[V_o^{\bullet\bullet}\right] n^2$$

As shown in above Figure, vanadium doped into SZO-based thin films can modulate barrier height of charge carriers which conduction electrons overcome from trapping level(i.e., oxygen vacancies) to conduction band, thereby further affecting resistive switching characteristics of the devices.

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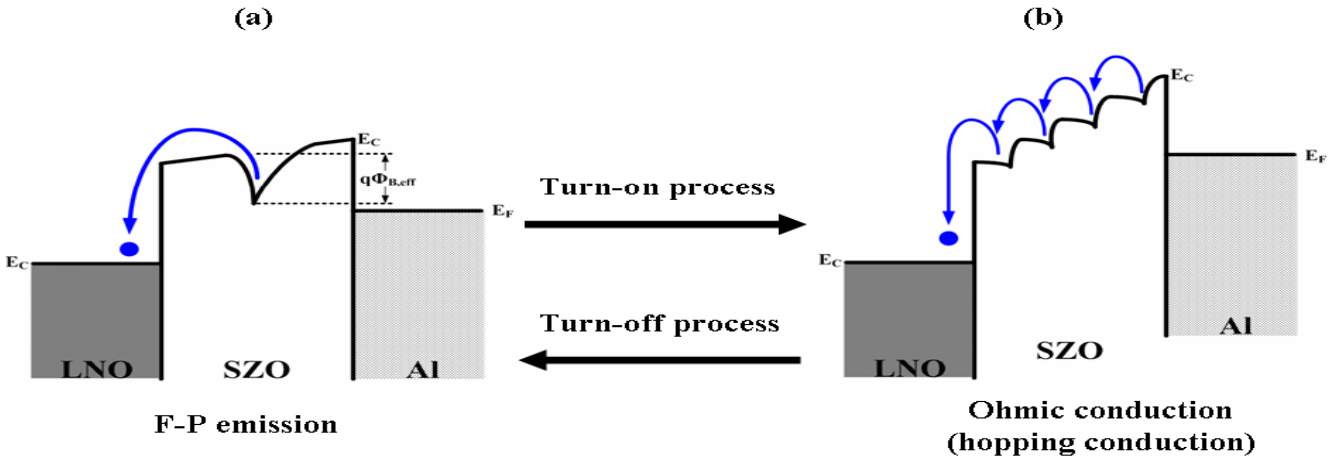

(a) Below turn-on voltage,it is field-enhanced thermal excitation of trapped electrons into the conduction band, indicating the conduction electrons hopping through the small amount of deep oxygen vacancies in SZO-based thin films.

(b) Above turn-on voltage, the charge carriers(i.e., oxygen vacancies) are aligned to form conducting filaments connecting TE and BE with the barrier height in the range of 0.10~0.13 eV, leading to the transition from F-P emission to Ohmic conduction, which is so called thermally excited and electron hopping in the SZO-based films.

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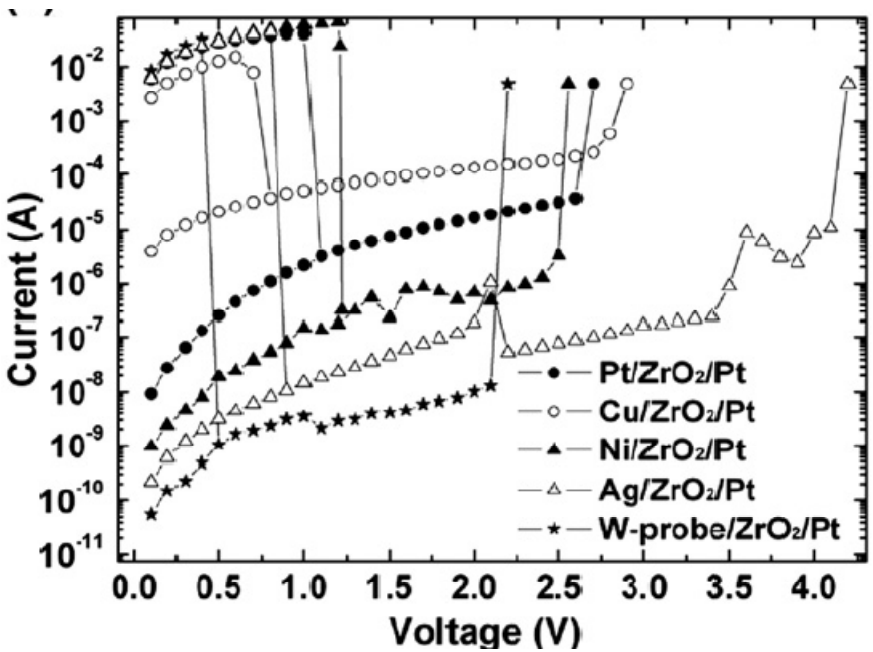
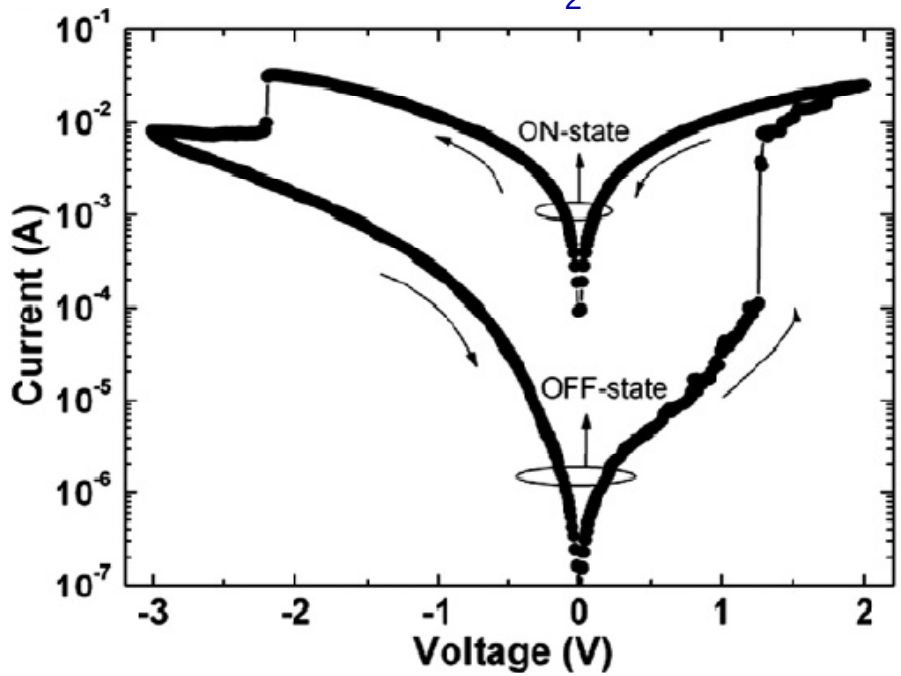
Top electrode effect

Resistive Switching of ZrO_2

- Work function of Pt, Ni, Ag, Cu, Al, and Ti: 5.65, 5.15, 4.73, 4.7, 4.3, and 4.3 eV, respectively
- Non-polar to bipolar resistive switching
- Work function effect neglected
- Oxygen gettering ability dominant



Ti/ZrO_2/Pt



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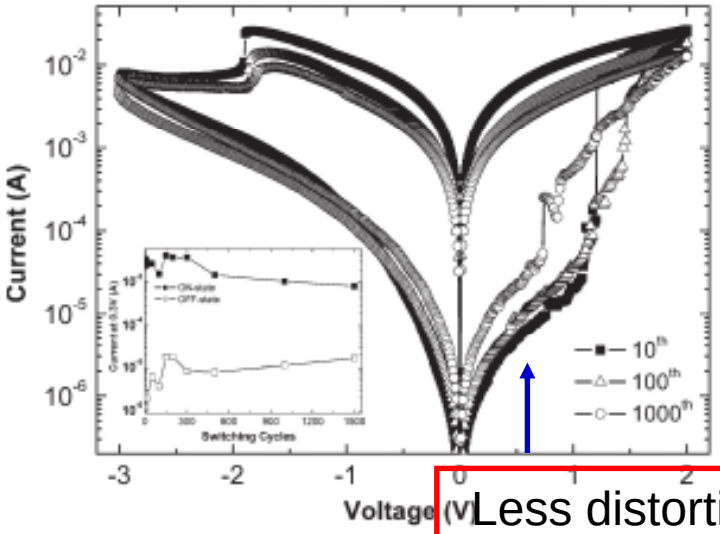
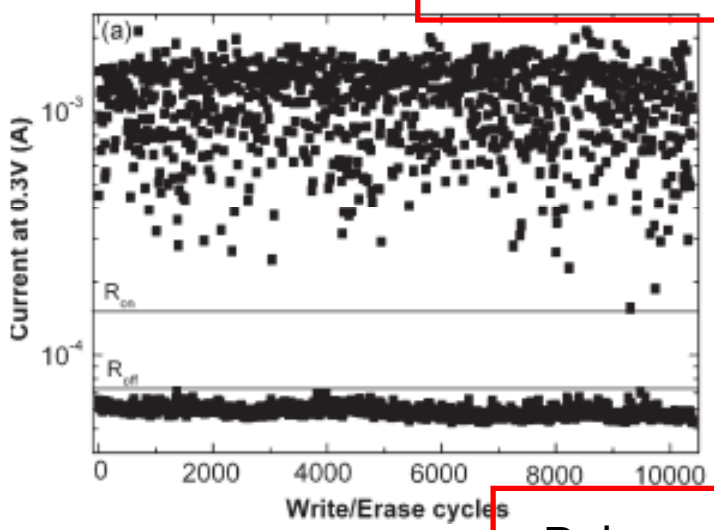
Top-electrode Ti

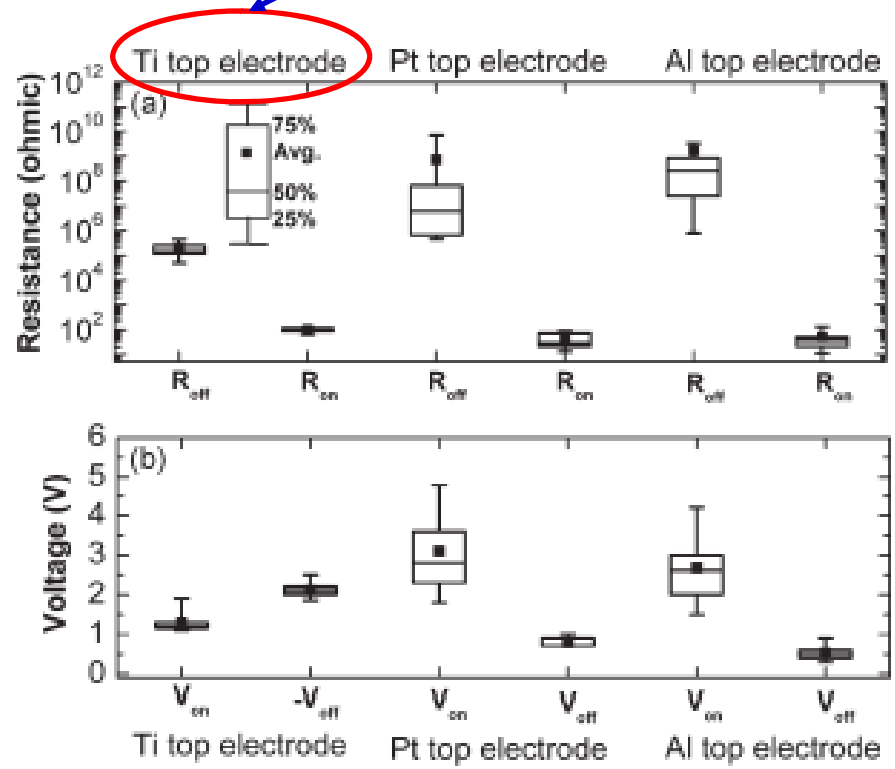
Binary metal oxides-ZrO_2



Less distortion



Uniformity



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Pulses more than 10000

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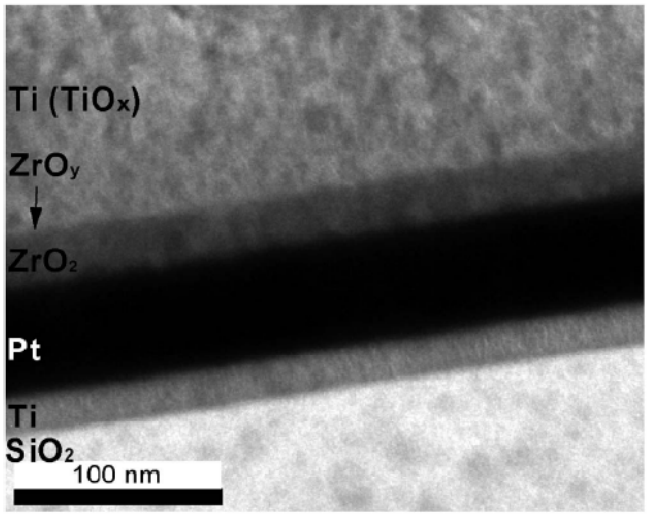
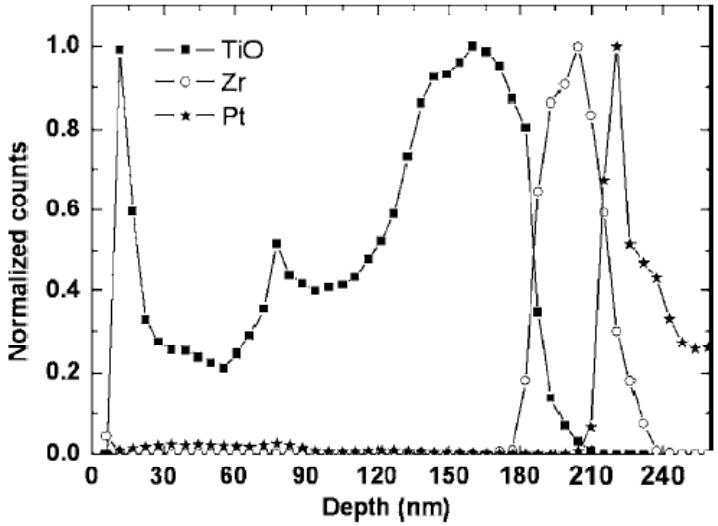
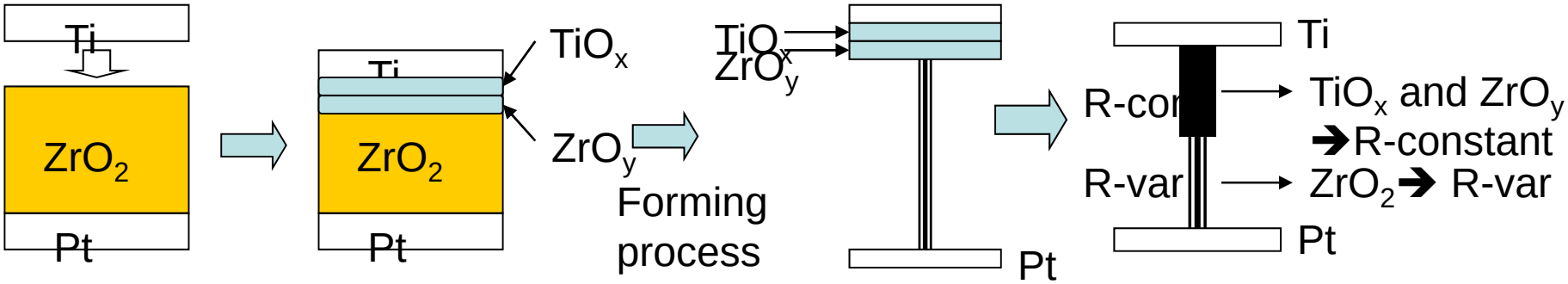
Top-electrode Ti

Binary metal oxides-ZrO_2

- Interface layer comprises of TiOx and ZrOy characterized by SIMS and TEM, respectively.







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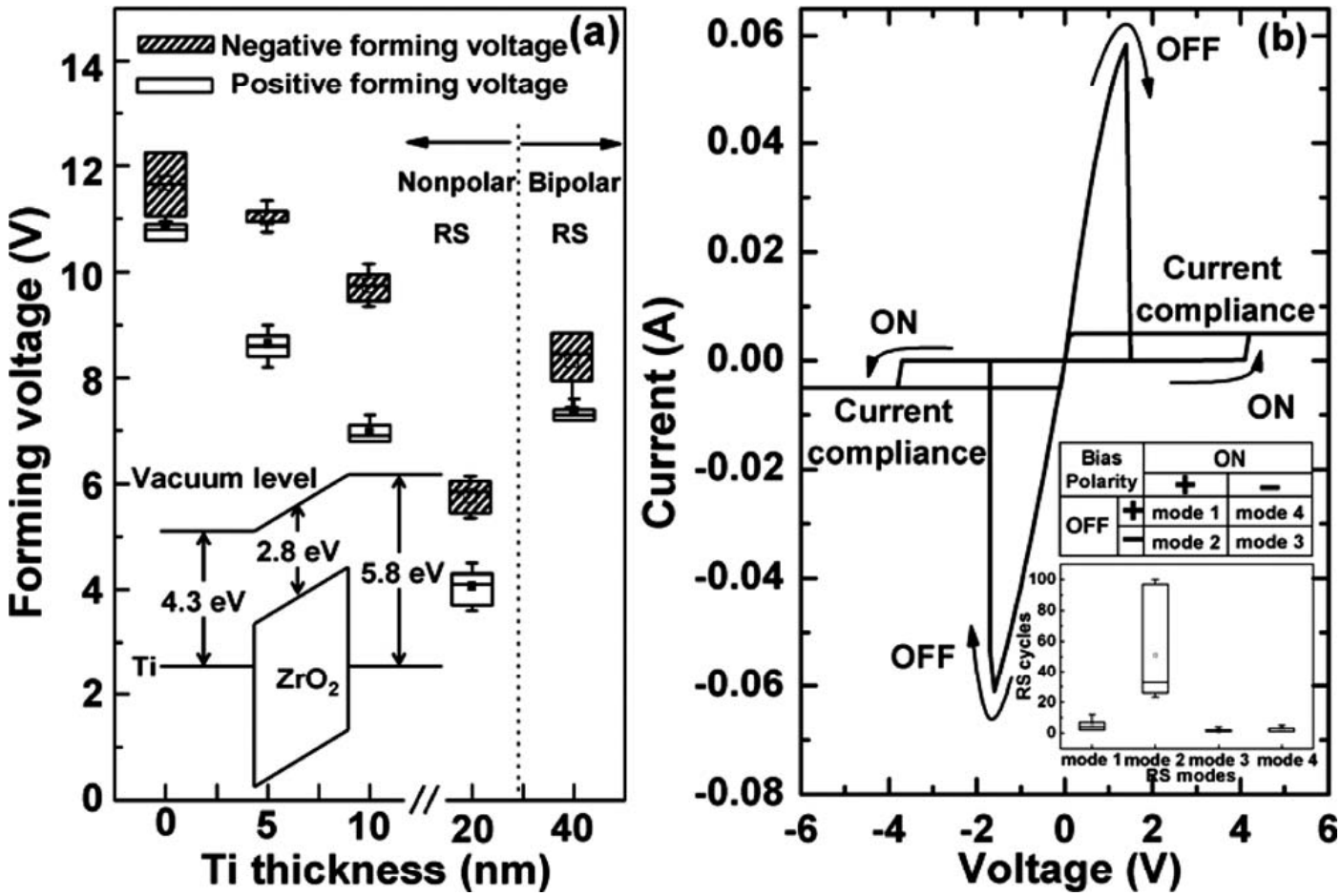
2007 JAP Lin&Tseng et al. **NCTU**

Top electrode thickness

Nonpolar resistive switching

Endurance test in 5T devices(inset)



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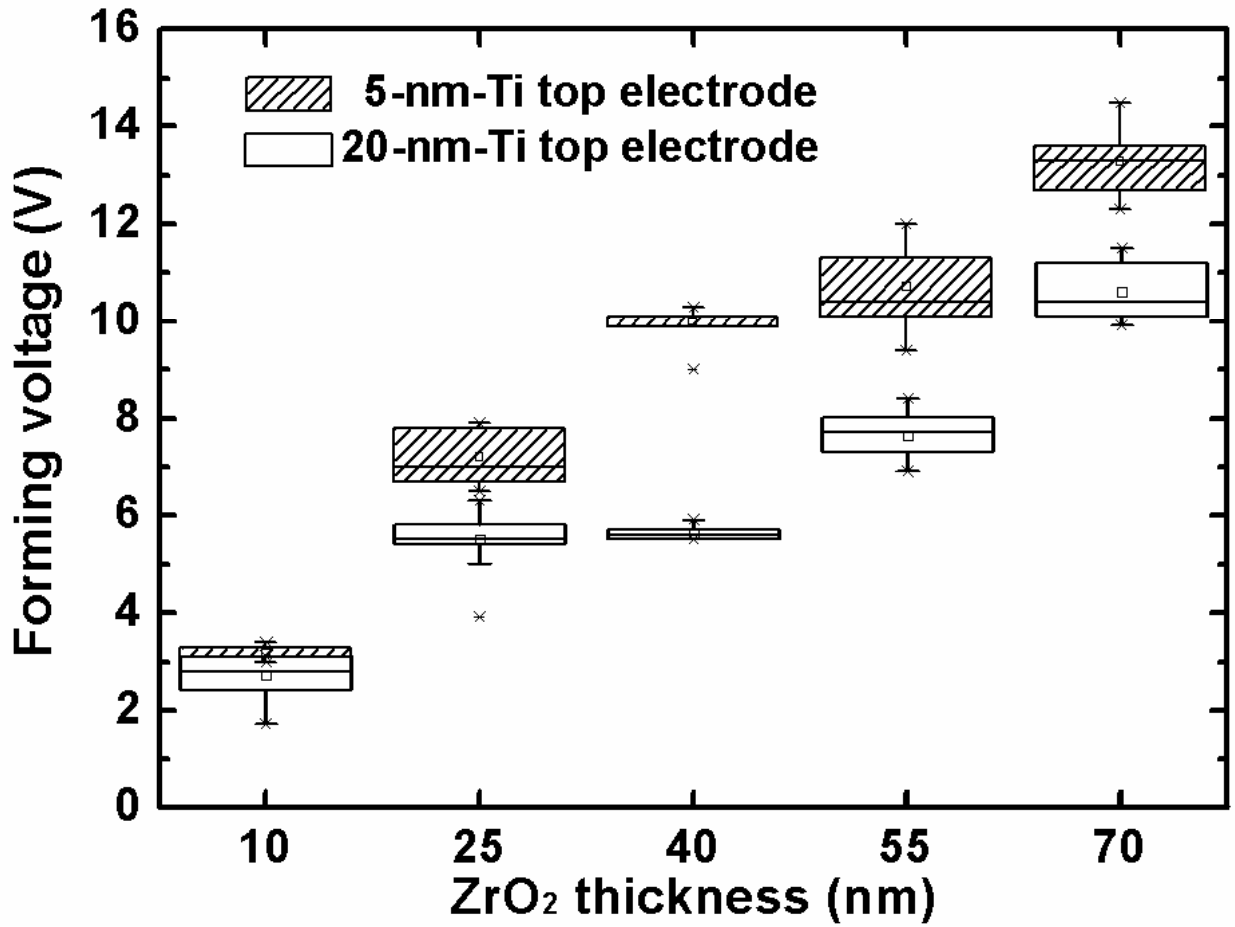
ZrO_2 thickness



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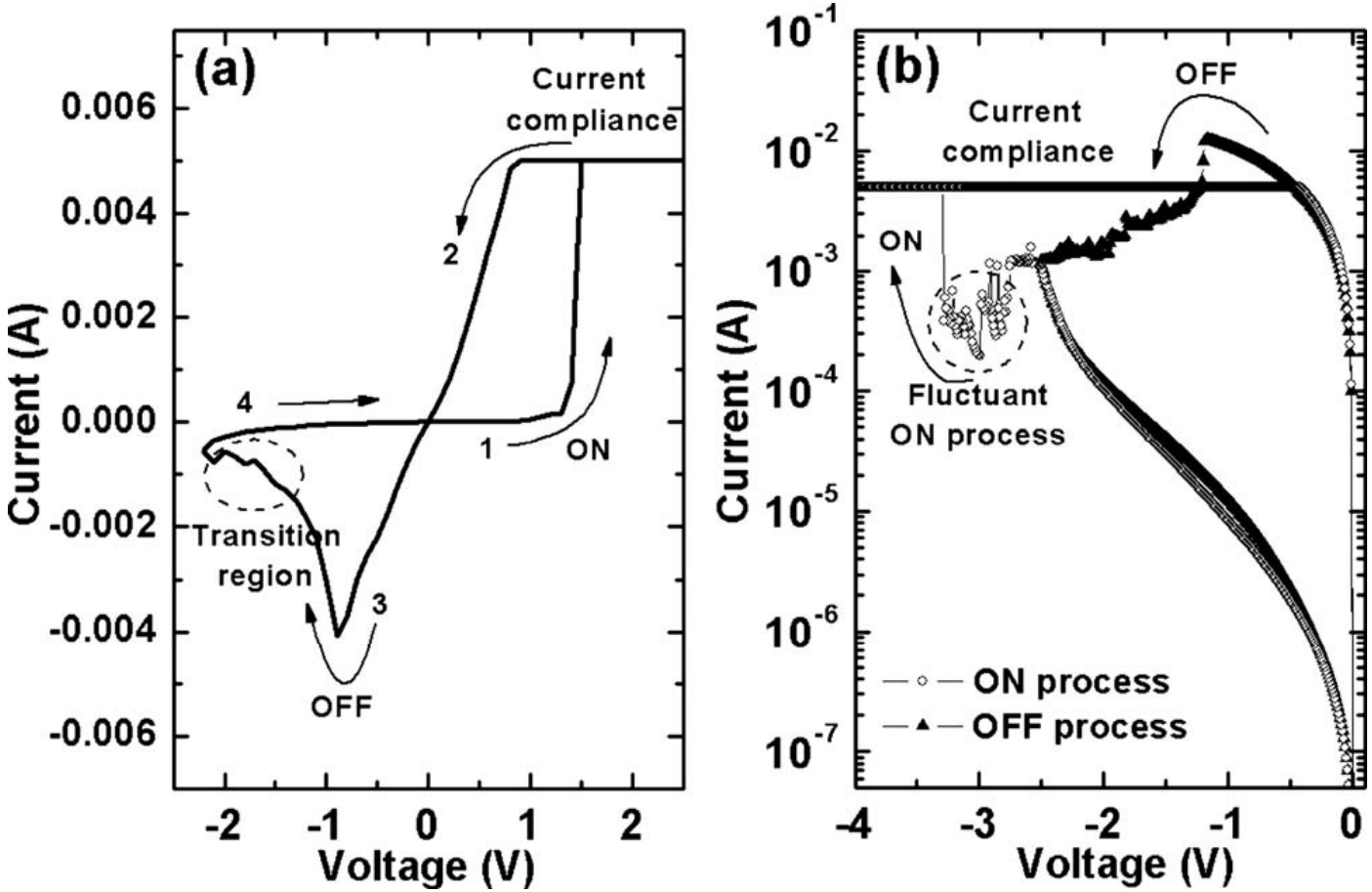
Bipolar RS behaviors of 40T devices

Fluctuant ON process



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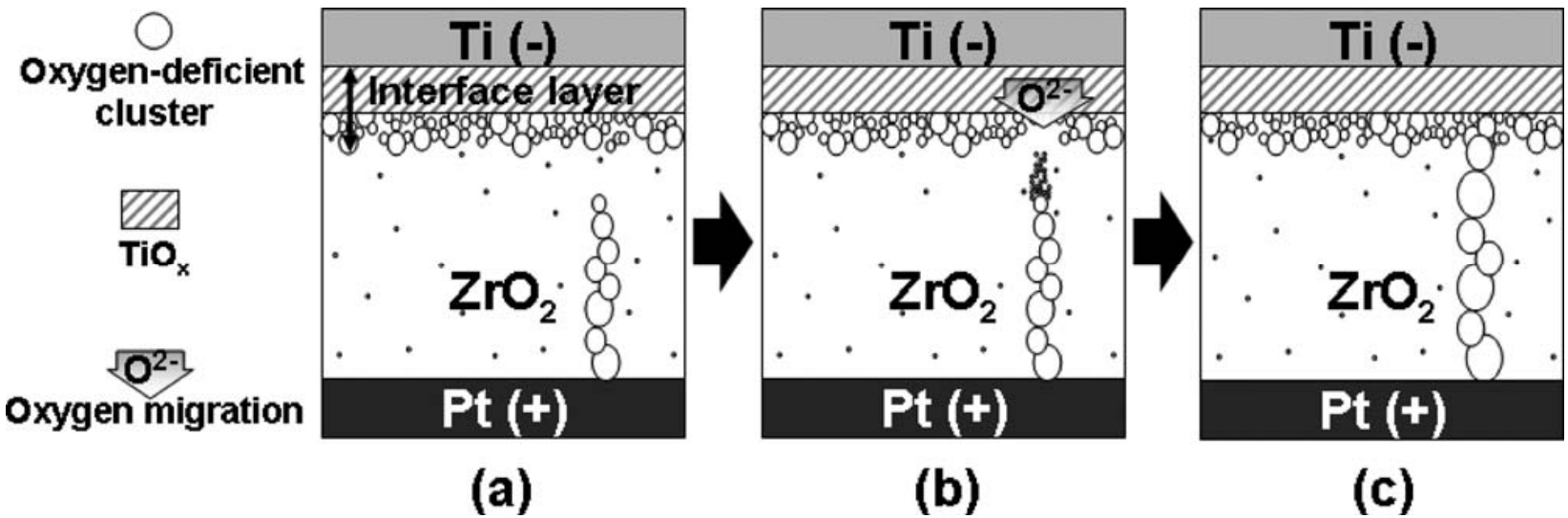
Conducting filament formation and rupture



Off state | Fluctuant on process | On state

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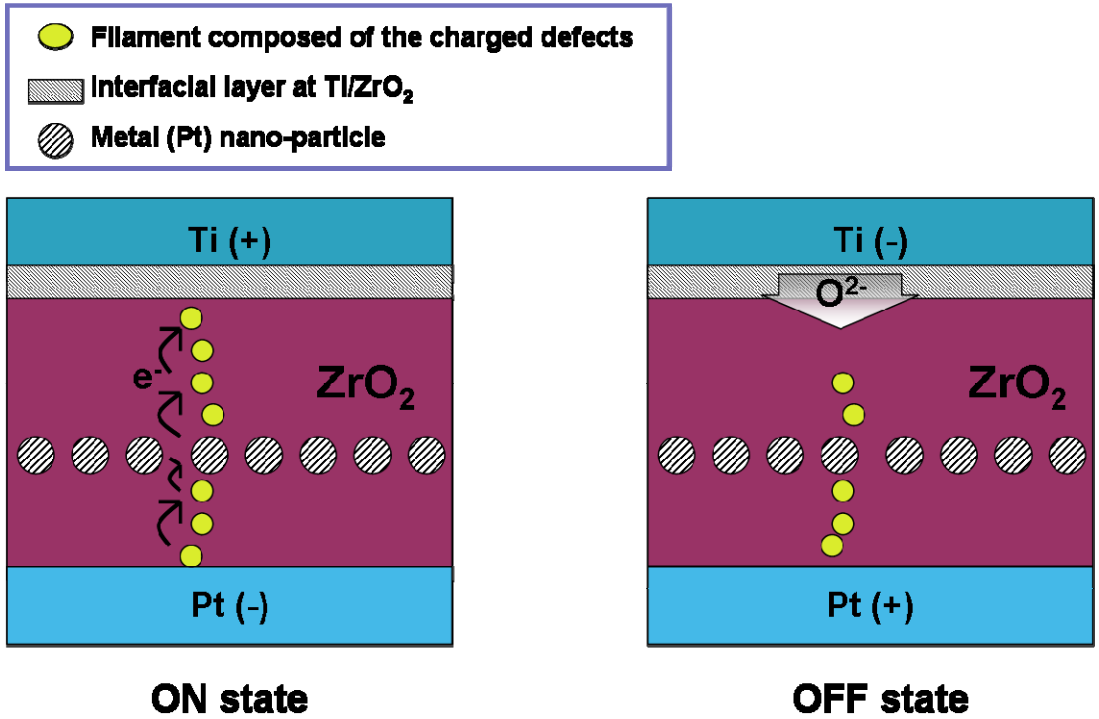
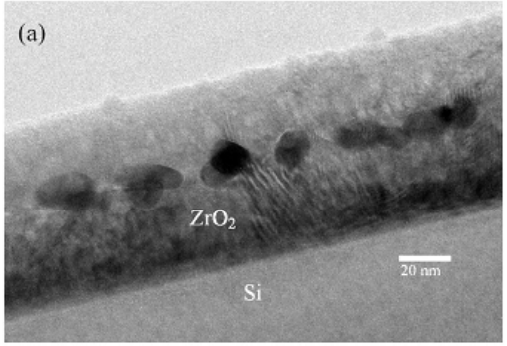
Performance of of the current reported ZrO2-based memory devices

Device structure *	R_{ON}	R_{OFF}	$\|V_{ON}\|$	$\|V_{OFF}\|$	RS cycles	$\|Pulse_{ON}\|$	$\|Pulse_{OFF}\|$	Device yield	Reference
Ti/ZrO_2/Pt	150~2kΩ	10k~100kΩ	~0.9V	~1.4V	10000	6V/50ns	3V/50ns	~100%	This work
Pt/ZrO_X/p^+-Si	~3kΩ	43kΩ	~1.6V	~1.1V	80	6V/100ns	2V/100ns	43%	[11-12]
TiN/ZrO_2/Pt	300~800Ω	4k~80kΩ	0.7~1.1V	0.5~0.8V	480	1.5V/1μs	2V/1μs	N.A.	[13]
Au/nc-Au ZrO_2/n^+-Si **	5k~166kΩ	9M~83MΩ	2.6~3.5V	1~3V	100	N.A.	N.A.	73%	[14]
Cr/Au-implanted ZrO_2/n^+-Si	70~30kΩ	2M~300MΩ	~8V	~2.2V	200	12V/50ns	6V/100ns	~100%	[15]
Cu/Cu-doped ZrO_2/Pt	100Ω	100MΩ	2.1~3.6V	0.8~1.5V	N.A.	N.A.	N.A.	Higher than that undoped	[16]
Cr/Zr^+-implanted ZrO_2/n^+-Si	~4kΩ	~200MΩ	~3.2V	~3.1V	N.A.	N.A.	N.A.	Higher than that unimplanted	[17]

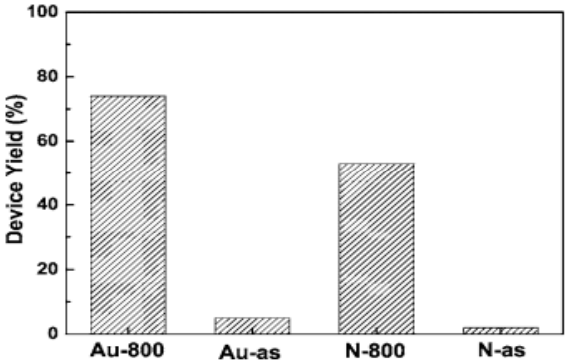
Tsai & Tseng, NCTU 2009

Nanocrystals-embedded RRAM



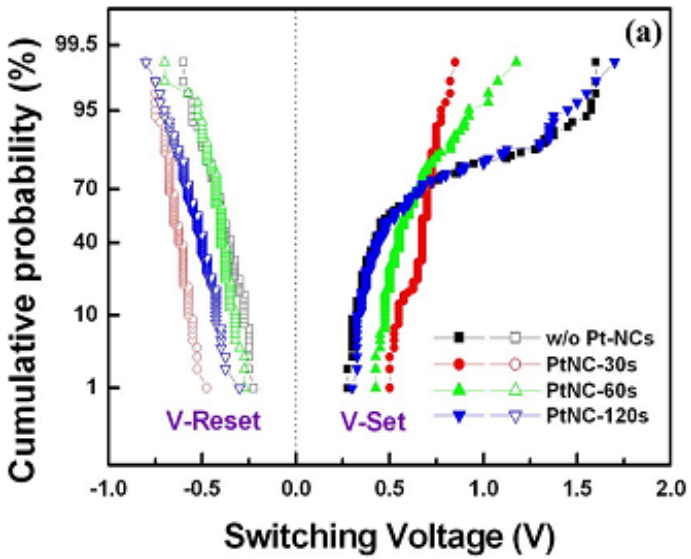


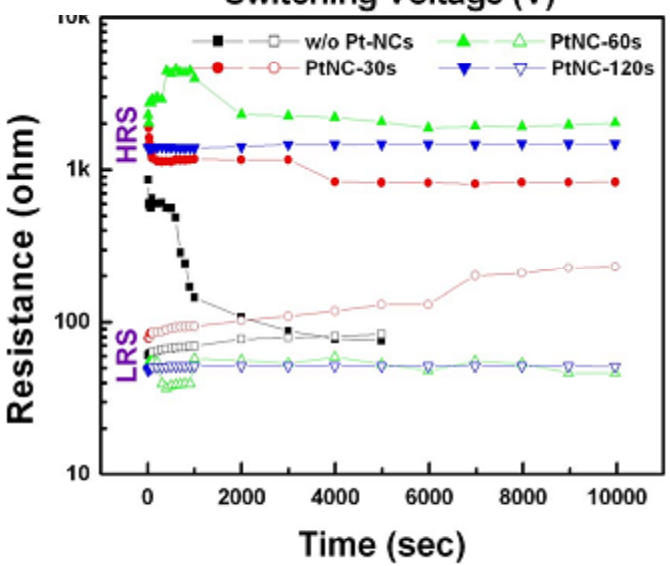
2007 APL W.Guan & S.Long

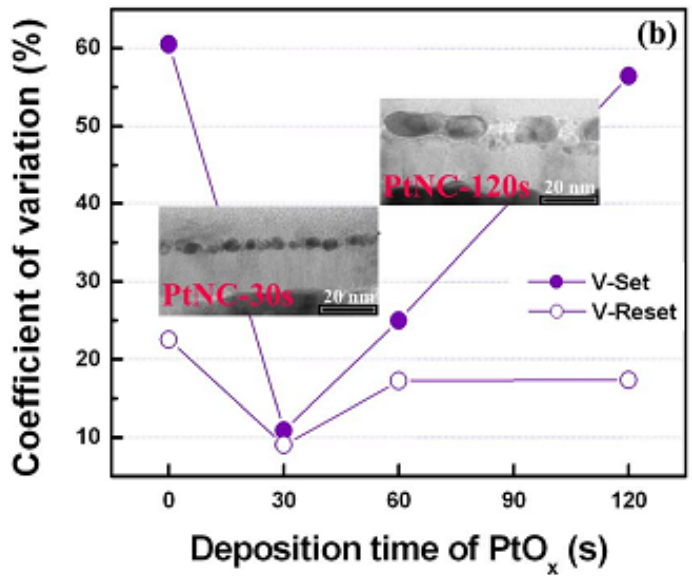


- Due to the higher electric field induced around the embedded nanocrystals within ZrO2, it expected that the localized conducting filaments would pass through the nanocrystals by external electric field driving. The modified intentional defects are believed to be easily altered and created while applying voltage bias on the memory device.

Embedded metal







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- Enhancement in electric field is in the thickness direction normal to Pt particle. providing easy path to form a fixed conducting filament in thin films. Therefore, fluctuationof switching parameters could be stabilized by the embedded particles.

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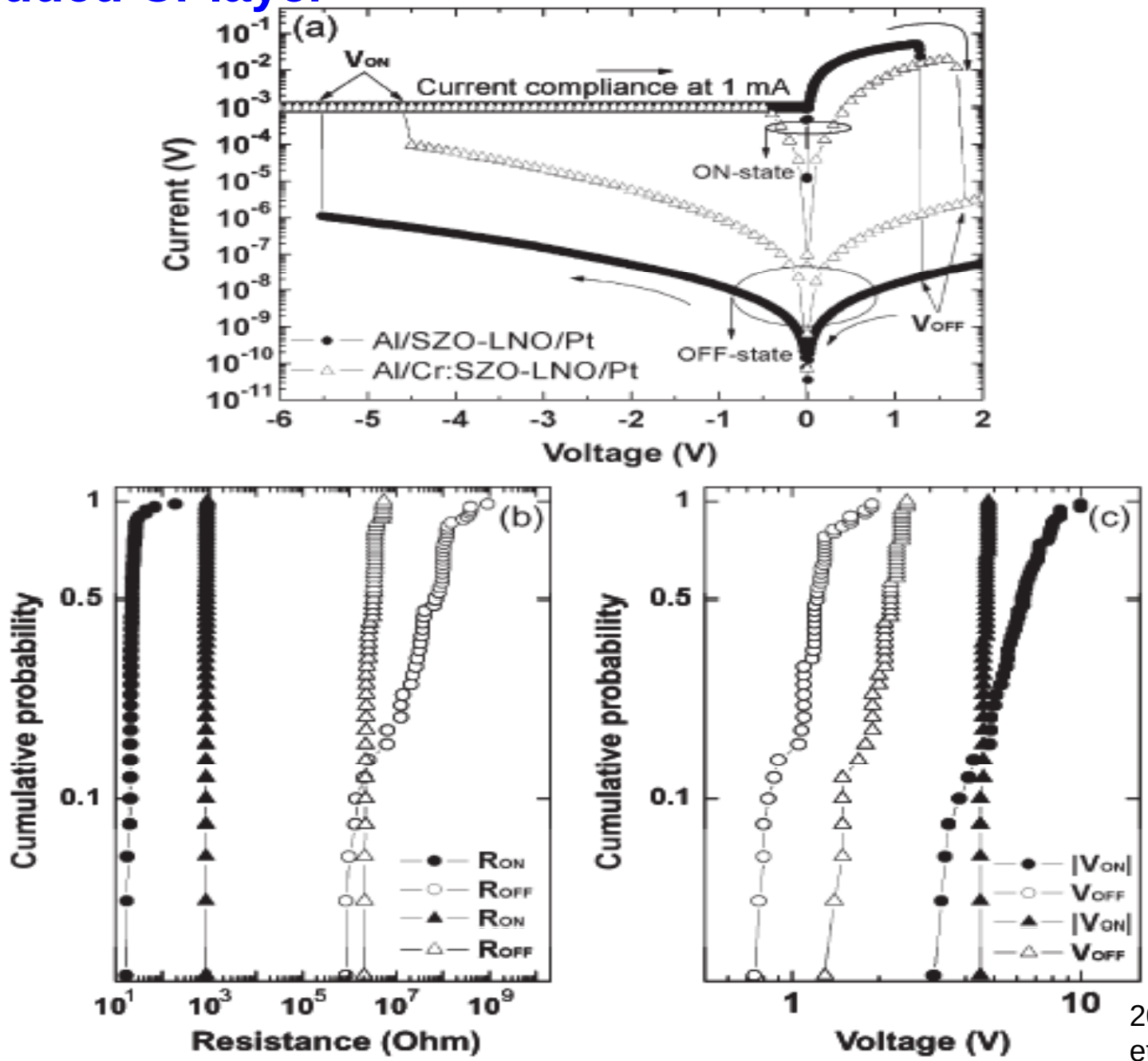
Embedded Cr layer



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Summary

- Ferroelectric materials in the gate and complex metal oxides materials are among the new materials being studied for future nonvolatile memory applications.

- The high-k materials with high crystallization temperature and low leakage current are a good candidate of buffer insulating layer in MFIS FETs, which foreshadow further retention time improvements of MFIS FETs.

- 3D ferroelectric capacitor structures, ferroelectric materials with a higher Pr, lowering crystallization temperature of ferroelectric films for avoiding the degradation of underlying transistor during annealing, and forming very thin ferroelectric films for realizing low voltage operation are being studied for fabricating high density ferroelectric memory.

- Effects of composition,nonstoichiometry,dopants,crystallization,and thickness of resistive switching films; electrode materials; and embedded nanocrystal and metal on the switching characteristics of RRAMs and their conduction mechanisms are being studied for enhancing their performance and reliability.

Thank you for your attention

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