Nano-ReRAM for Novel FPGA Architectures

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University at Albany State University of New York

CNSE: The $ 5 Billion Facilities

NanoFab 300S
$50M, 150K ft²
32K Cleanroom
Completed: 03/04

NanoFab 300N
$175M, 228K ft²
35K Cleanroom/Clean SubFab
Completion: 12/05

NanoFab 300E
$100M, 250K ft²
15K Cleanroom
Completion: 08/08

NanoFab 200
$16.5M, 70K ft²
4K Cleanroom
Completed: 06/02

- Integration of university and industry partners:
  - IBM and Global Foundries
  - International Sematech
  - Applied Materials, Tokyo Electronics

College of Nanoscale Science & Engineering
University at Albany State University of New York

Acknowledgment:
NSF, AF, SRC, Sematech

NanoDevice and Circuit Group

Prof. Wei Wang
CNSE, State University of New York

Memory and

vices (NSF)
ano hybrid

L crossnet
4) Multi-value RRAM

unction-
gic

IEEE ELECTRON DEVICE LETTERS, VOL. 29, NO. 5, MAY 2008

Nonpolar Nonvolatile Resistive Switching in Cu Doped ZrO_2

Weihua Guan, *Student Member, IEEE*, Shibing Long, *Member, IEEE*, Qi Liu, Ming Liu, *Member, IEEE*, and Wei Wang, *Member, IEEE*

APPLIED PHYSICS LETTERS **94**, 233106 (2009)

Multilevel resistive switching with ionic and metallic filaments

Ming Liu,[1] Z. Abid,[2] Wei Wang,[2,a)] Xiaoli He,[2] Qi Liu,[1] and Weihua Guan[1]
[1]*Laboratory of Nanofabrication and Novel Device Integration, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China*
[2]*College of Nanoscale Science and Engineering (CNSE), University at Albany, New York 12203, USA*

APPLIED PHYSICS LETTERS **95**, 023501 (2009)

Formation of multiple conductive filaments in the $Cu/ZrO_2:Cu/Pt$ device

Qi Liu,[1,2] Chunmeng Dou,[1] Yan Wang,[1] Shibing Long,[1] Wei Wang,[3] Ming Liu,[1,a)] Manhong Zhang,[1] and Junning Chen[2]
[1]*Laboratory of Nano-fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China*
[2]*College of Electronics and Technology, Anhui University, Hefei 230039, People's Republic of China*
[3]*College of Nanoscale Science and Engineering (CNSE), University at Albany, New York 12203, USA*

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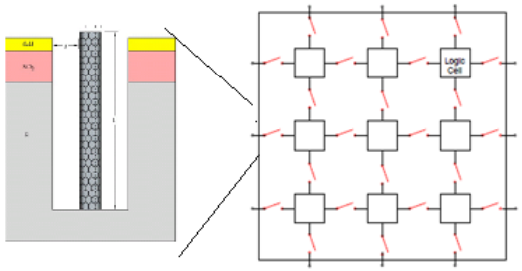
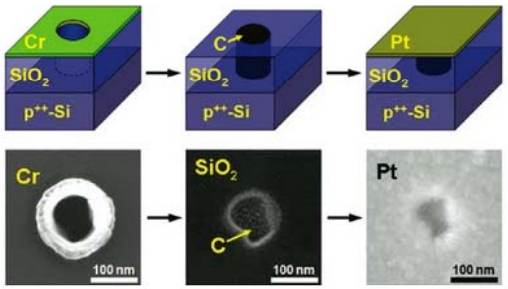
Emerging Memory for FPGA

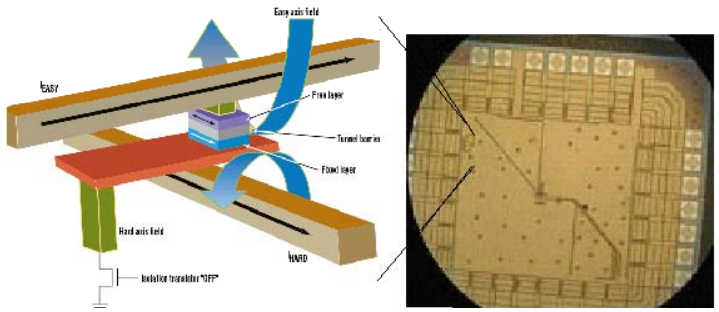
CNT Memory for FPGA



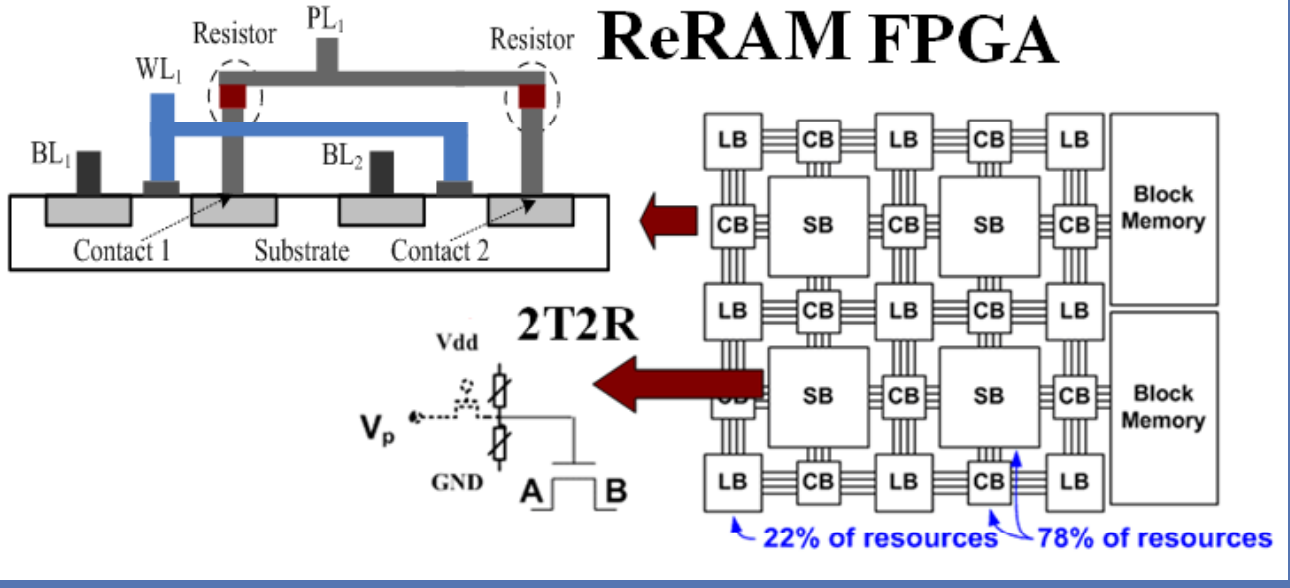
Graphene FPGA



MRAM FPGA

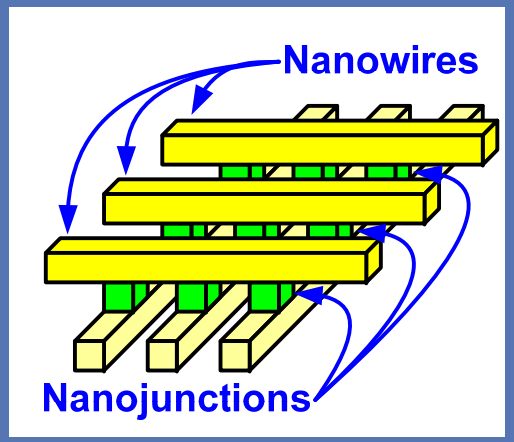


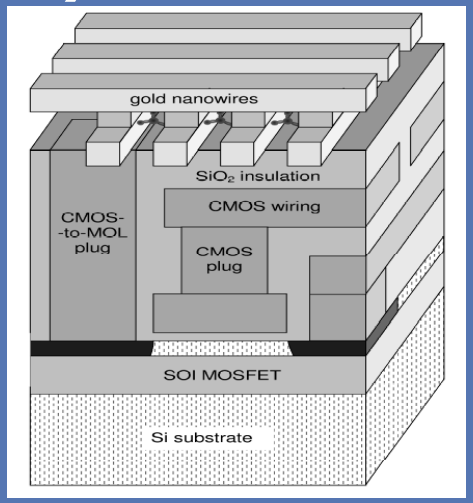
ReRAM FPGA

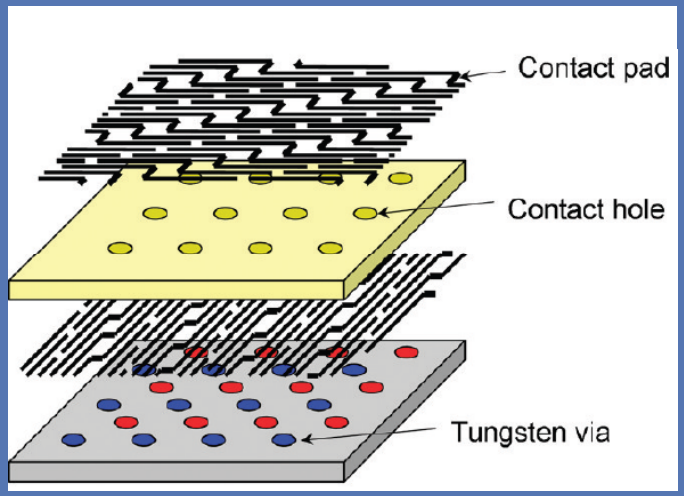


ReRAM FPGAs Based on Crossbar and 1T1R

Crossbar (1D1R)

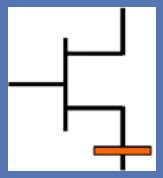


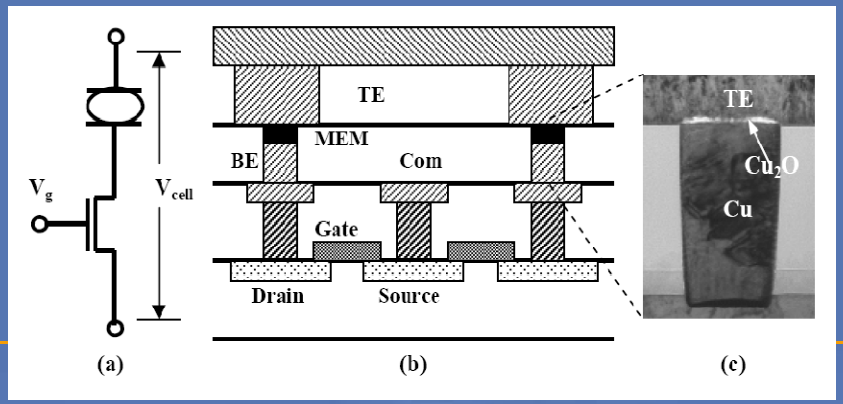




NanoPLA, CMOL, 3D CMOL, FPNI, NanoASIC, 3D nFPGA, NanoBox…

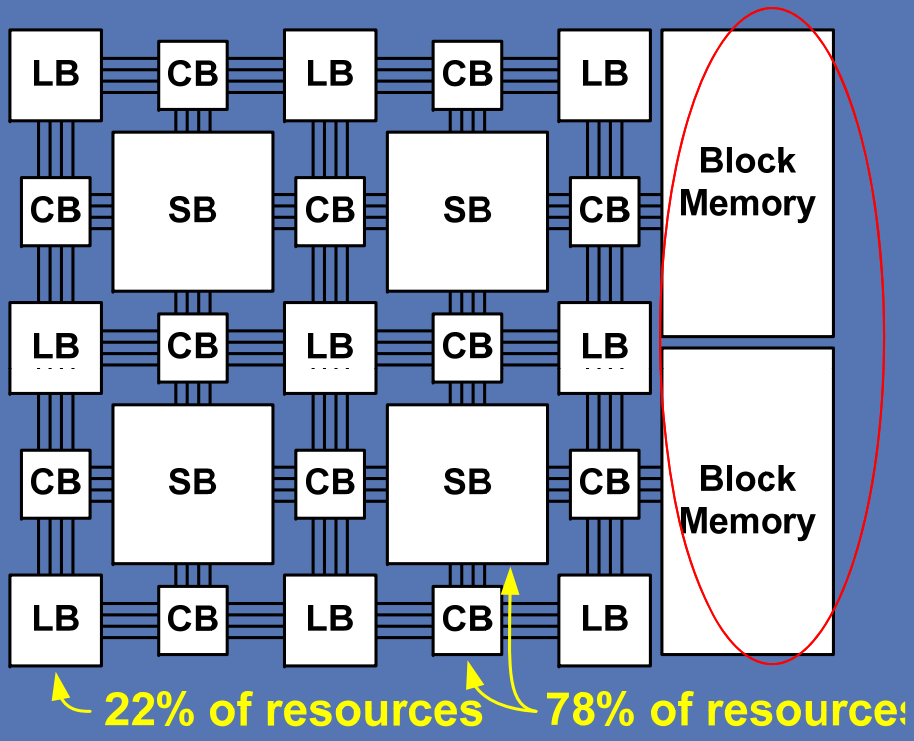
1T1R





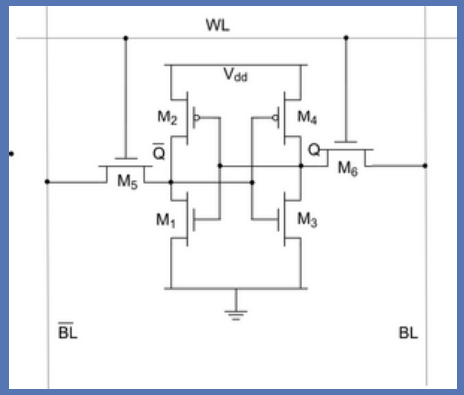
Spansion 2005

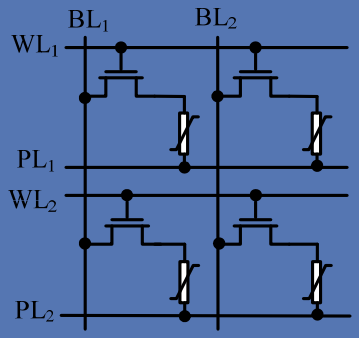
ReRAM for FPGA Memory, Routing, and Logic



1 bit SRAM: 6 transistors

1-bit NOR ReRAM: 1 transistor





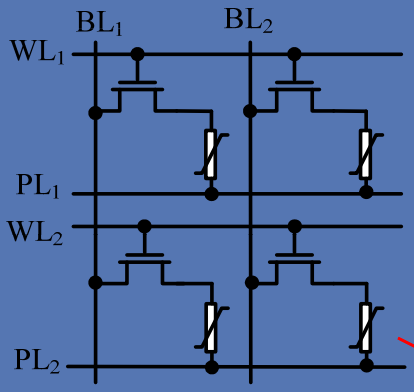
Using NOR ReRAM to replace SRAM

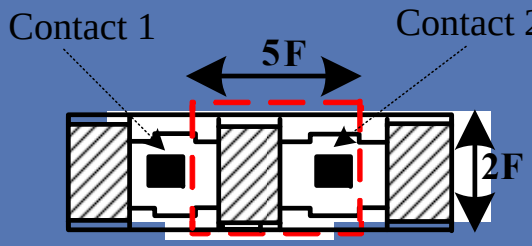
ReRAM can provide 4X-6X density and power improvement over SRAM!

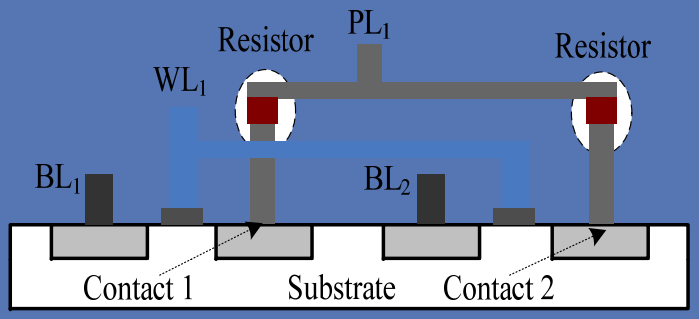
Micro and Nano Letters 2008

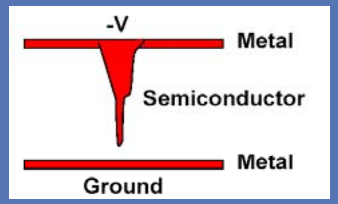
NOR ReRAM as Block Memory

- **NOR**



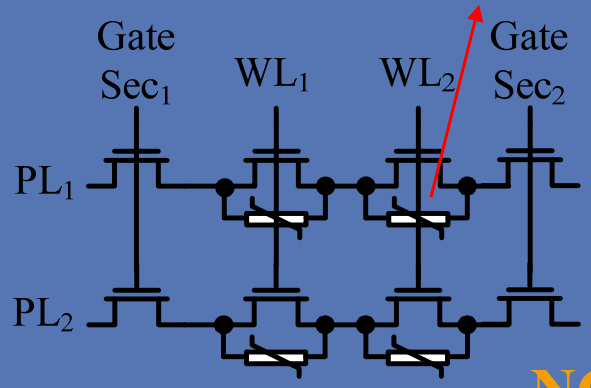


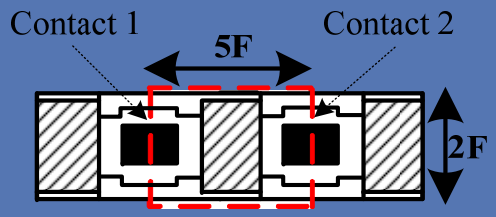


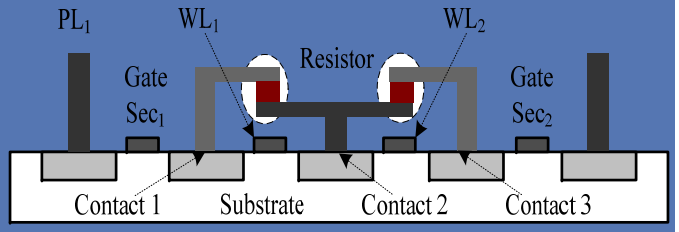


- **NAND**

Both cells are $10F^2$!

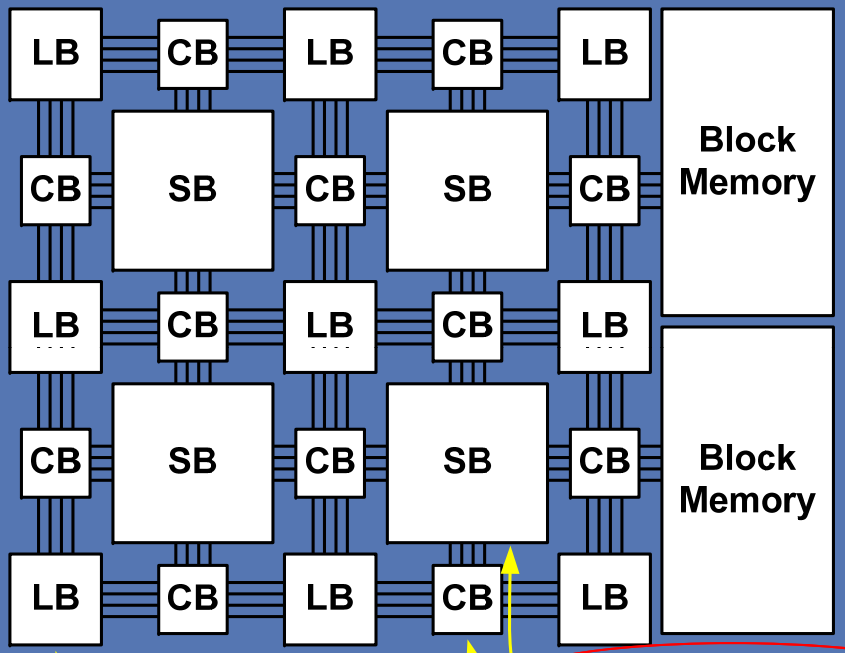






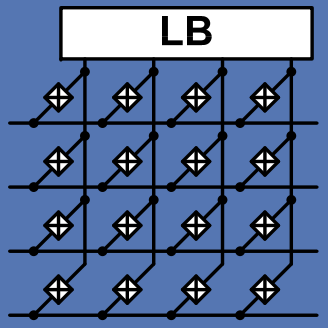
NOR ReRAM is better than NAND ReRAM.

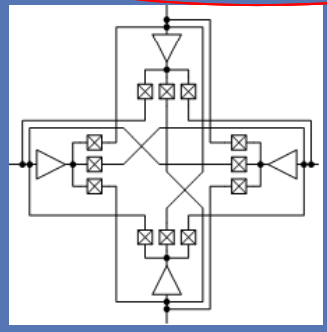
ReRAM for FPGA Memory, Routing, and Logic

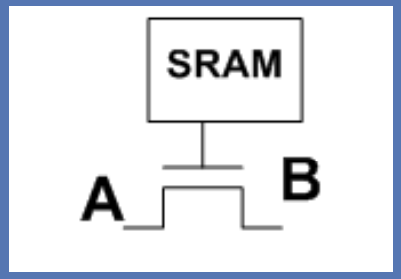


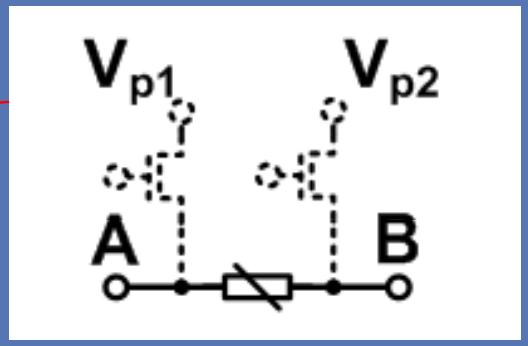
22% of resources

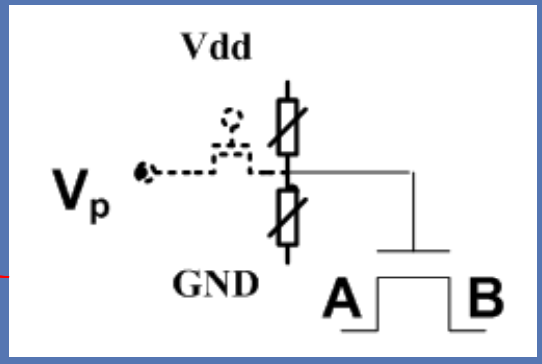
78% of resources







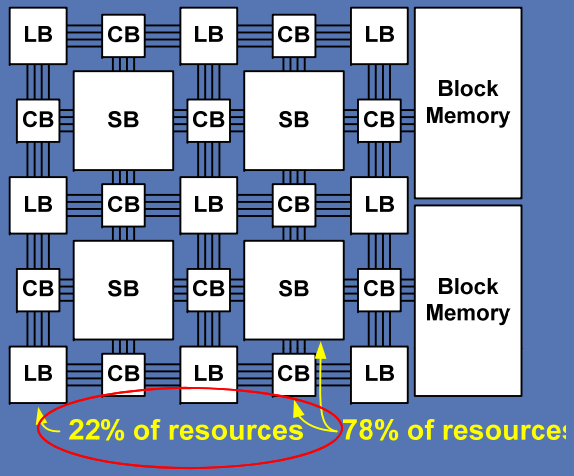


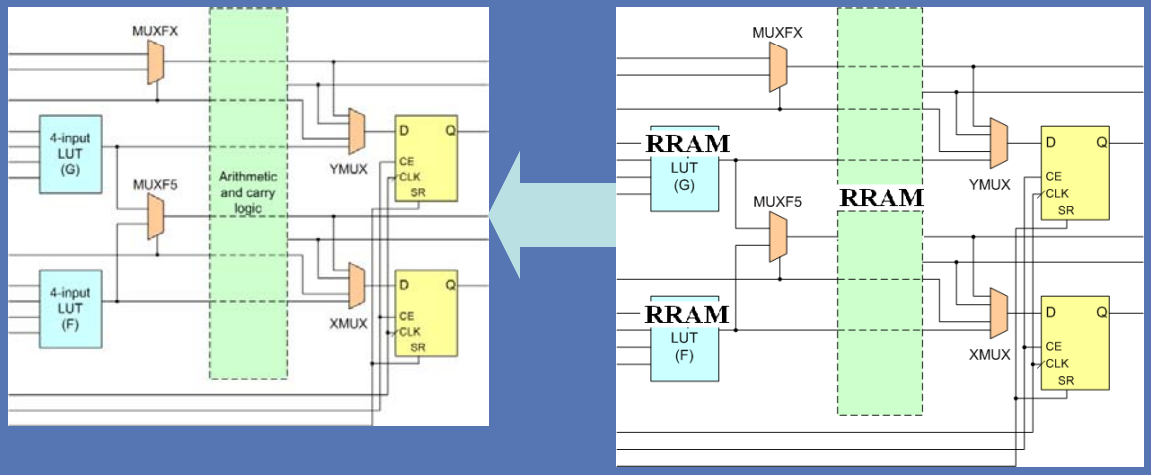


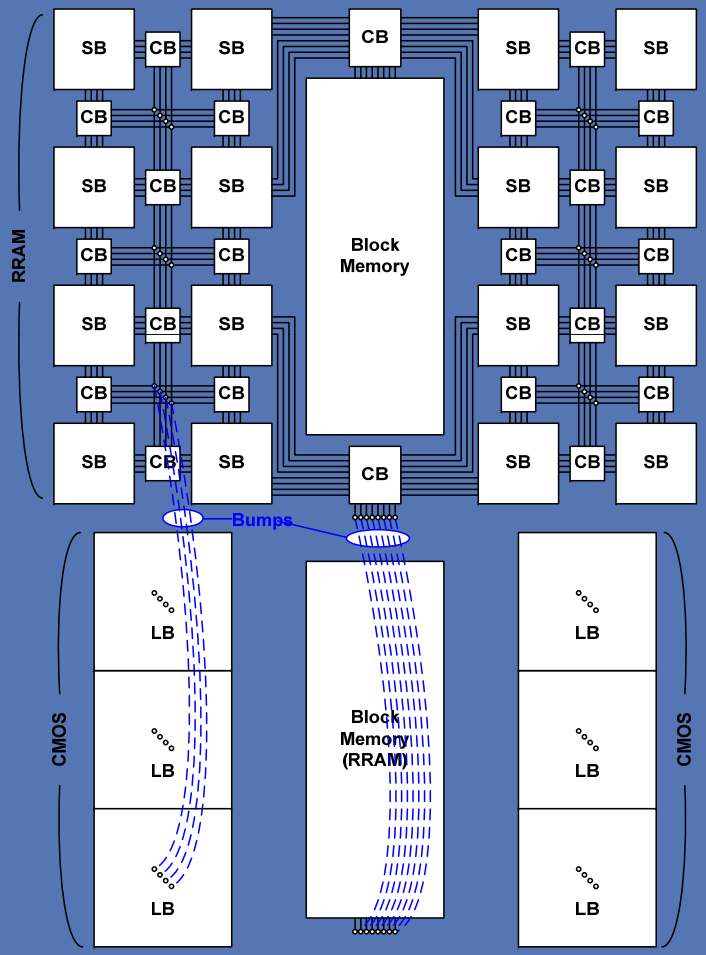
2X-3X Reduction in Routing.

IEEE NanoArch 2008

ReRAM for FPGA Memory, Routing, and Logic







2X Reduction in Logic.

3D rFPGA.

IEEE TVLSI, under review

Results Based on Toronto 20 Benchmarks

	Area (μm^2)		Critical path delay (ns)		Dynamic power (mW)	
	2D CMOS [6]	2D rFPGA	2D CMOS [6]	2D rFPGA	2D CMOS [6]	2D rFPGA
alu4	137700	55080	5.1	4.19	0.062	0.056
apex	166050	66420	6	5.4	0.067	0.060
ape4	414619	165848	5.5	4.05	0.042	0.038
clma	623194	249278	13.1	11.09	0.2	0.180
pdc	369056	147622	9.6	8.14	0.101	0.091
s298	166050	66420	10.7	9.23	0.042	0.038
seq	151369	60548	5.4	4.86	0.065	0.059
spla	326025	130410	7.3	6.07	0.087	0.078
tseng	78469	31388	6.3	5.07	0.029	0.026
Avg.	264381	105752	7.43	6.187	0.1	0.08

Area improvement is 2X-3X. Static power improvement is 10X.

Delay and dynamic power improvement is around 20%.

Summary

- **Emerging memory can improve FPGA performance**
  - **Density**
  - **Energy consumption**
  - **Reliability/Radiation harden**

- **Hybrid structure and CMOS-nano integration**
  - **Reconfigurable structure and defect tolerance**
  - **Applications to programmable analog/neuromorphic ICs**

Acknowledgment: NSF, AF, Sematech/CNSE