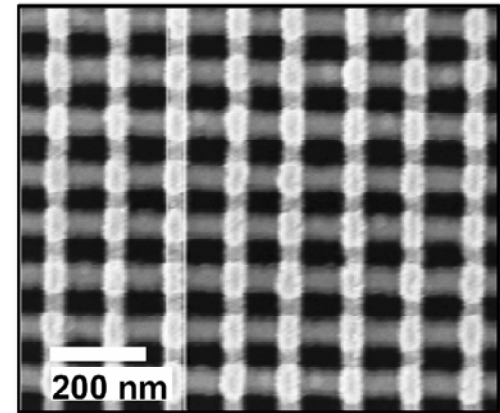




# Memory Cell Selection Device Enabling High Density Memory



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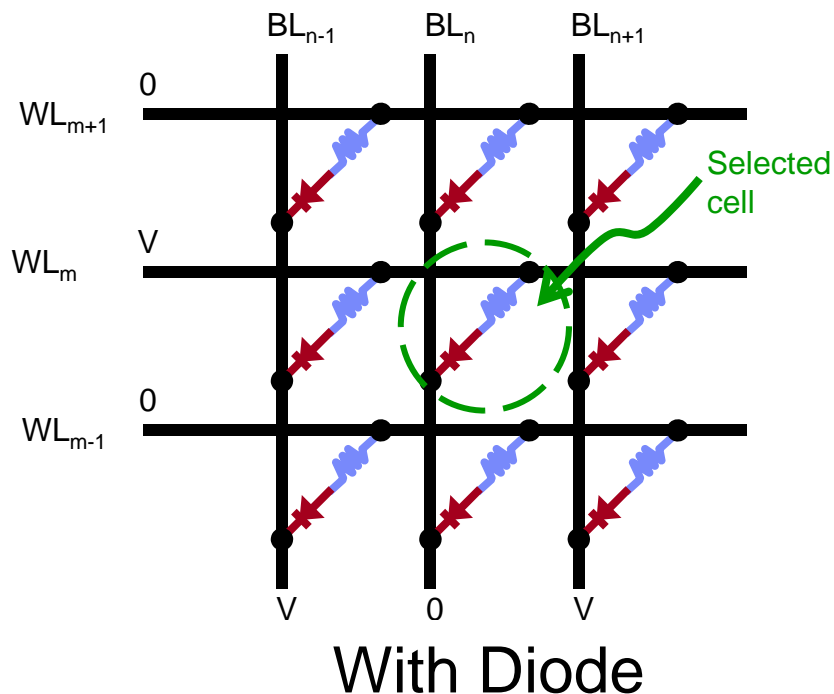
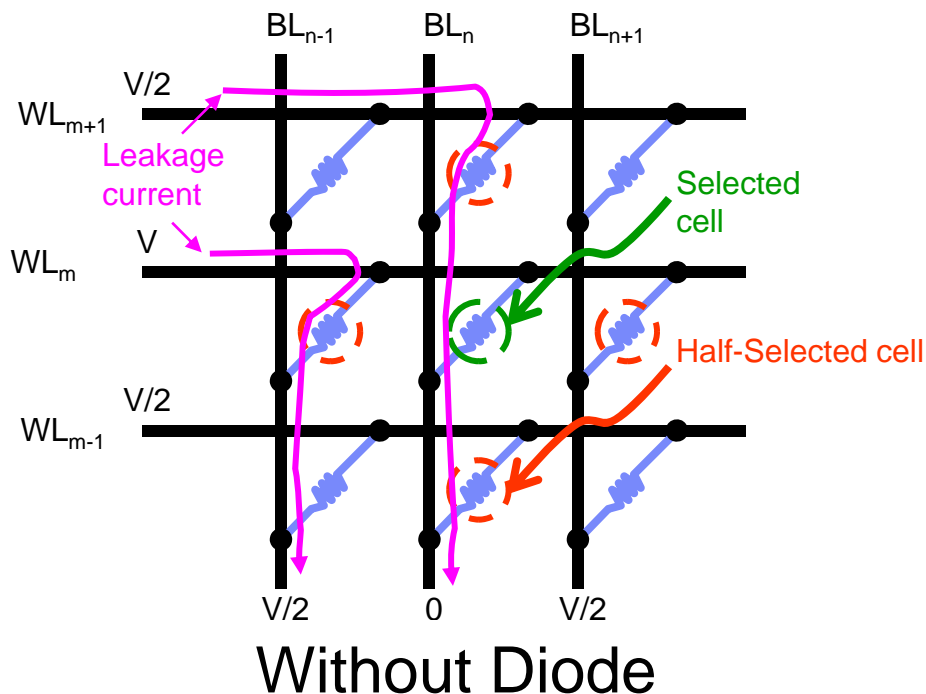
<http://www.stanford.edu/~hspwong>

<http://nano.stanford.edu>

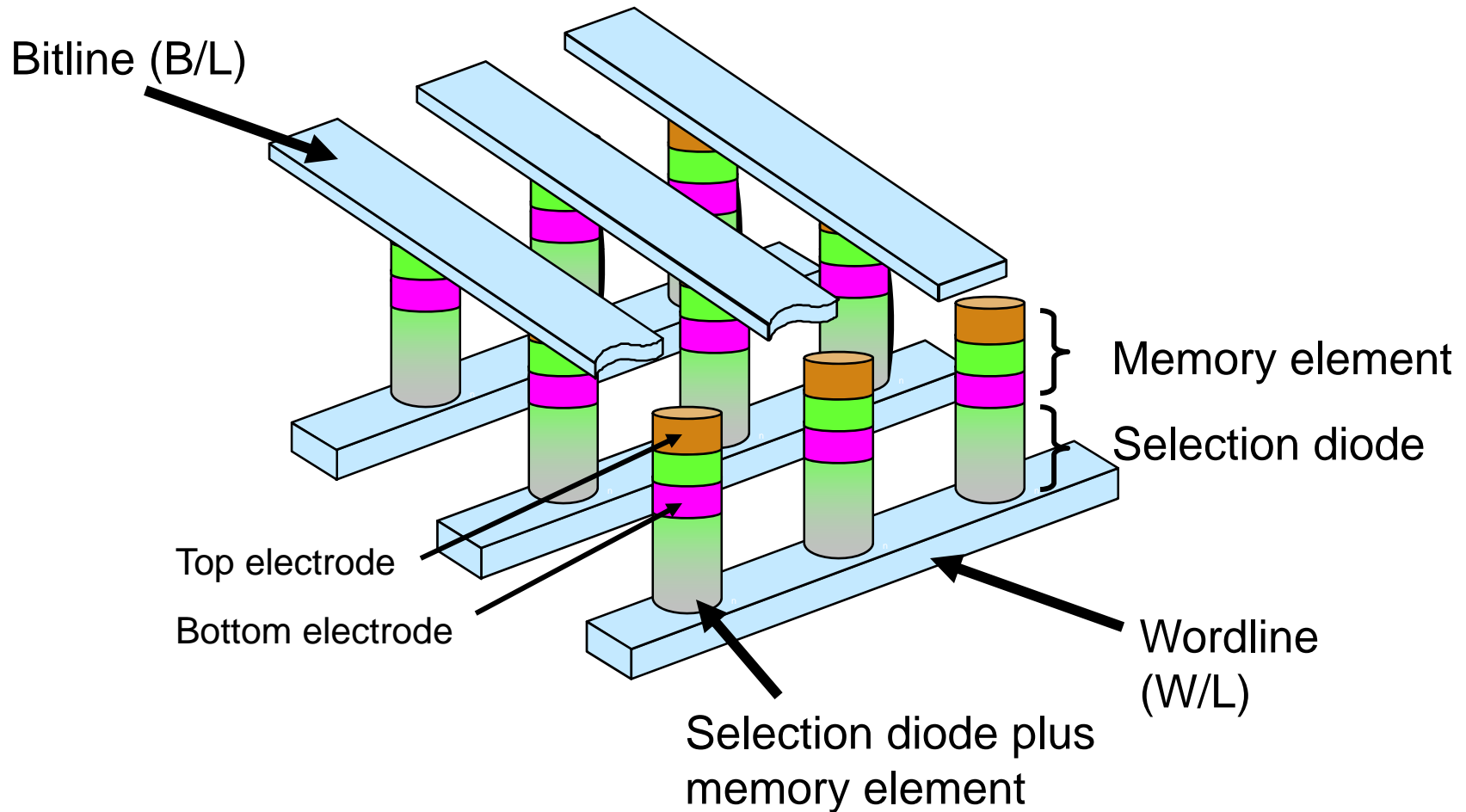
# Cross-Point Memory Cell Selection Device

## Required for:

- Read signal to noise margin
- Write-ability
- Power dissipation



# Cross-Point Memory Array with Selection Diode



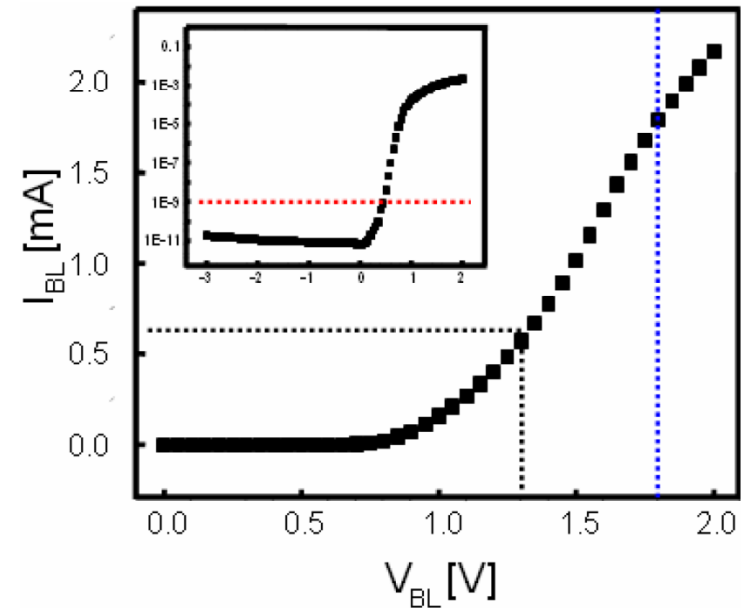
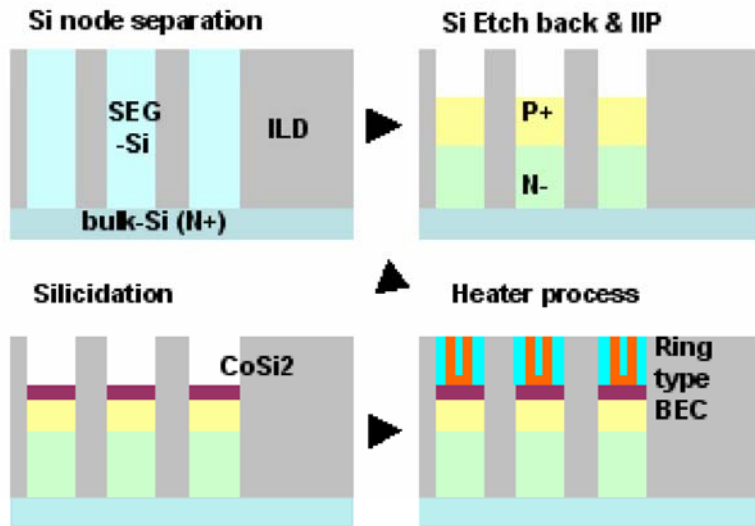
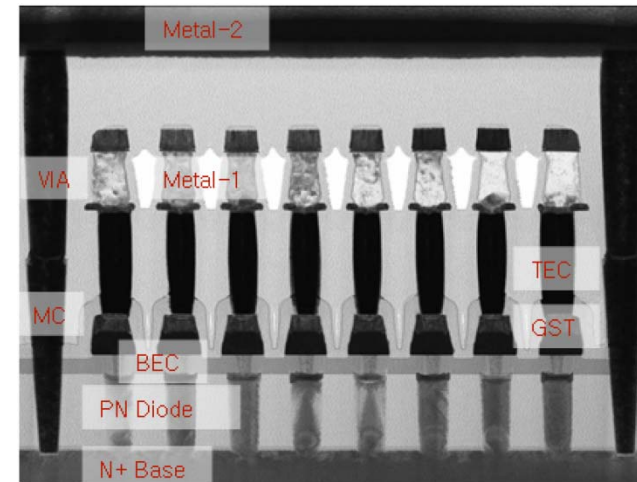


# Memory Cell Selection Diode Specifications

- **Small size (scalable as  $4F^2$ )**
- **Large current density**
- **Large  $I_{\text{on}}/I_{\text{off}}$  ratio,  $> 10^4$**
- **Low temperature process**
  - Integration with Si CMOS
  - 3D structure for embedded system

# Diode Example: Epi Si

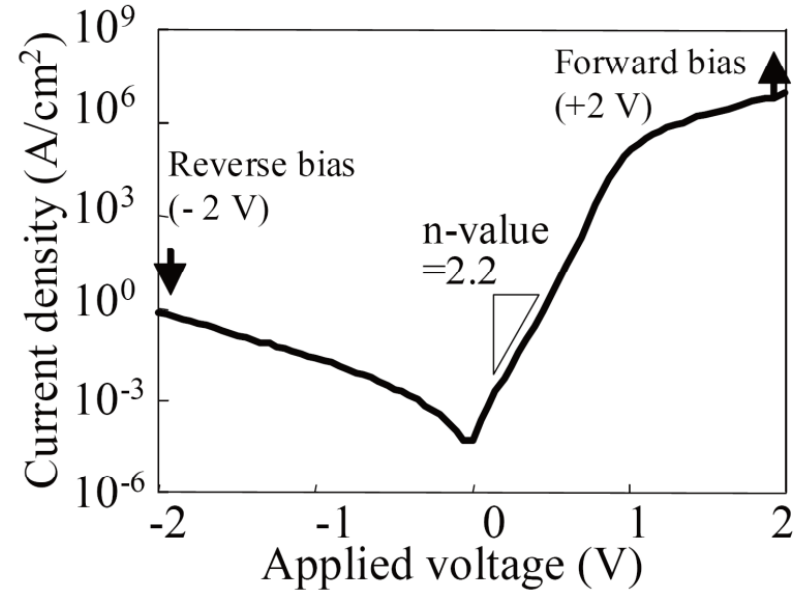
- 512 Mb PRAM with  $0.047\mu\text{m}^2(5.8F^2)$  cell, 90nm diode technology
- Current density 26 MA/cm<sup>2</sup> at 2V
- Single crystalline Si vertical diode by selective-epitaxial-growth



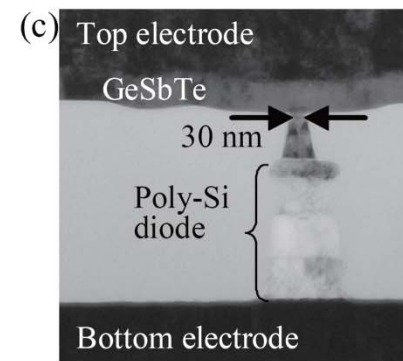
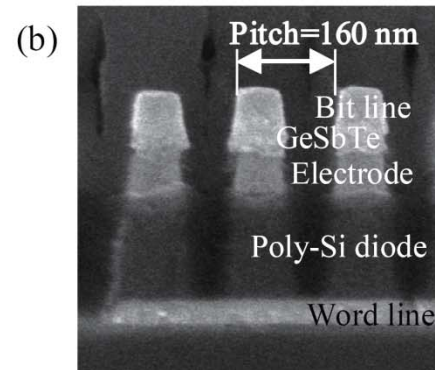
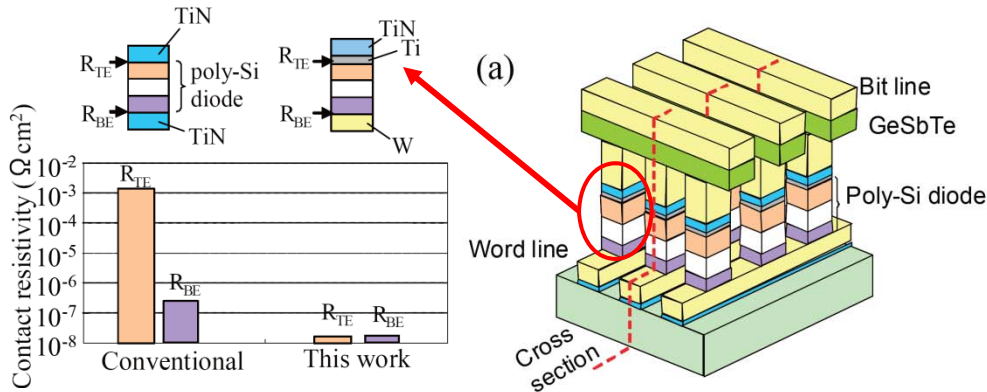
J.H. Oh et al., IEDM, p. 49, 2006. (Samsung)

# Diode Example: Poly-Si

- **High on current: 8MA/cm<sup>2</sup>**
- **Low off current: 100A/cm<sup>2</sup>**
- **Low contact resistivity and low temperature budget poly-Si p-i-n structure**



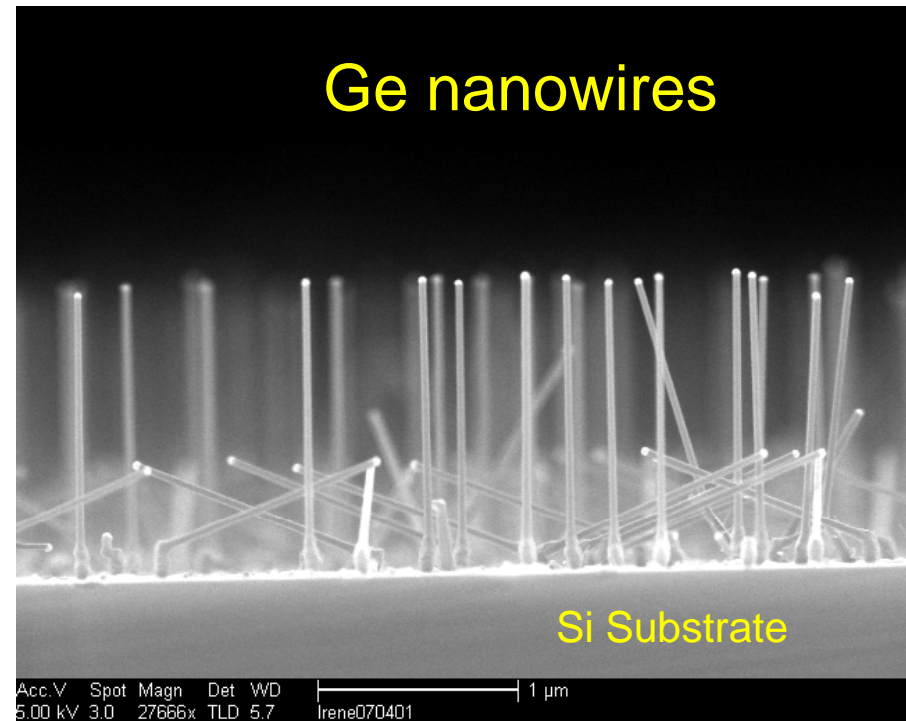
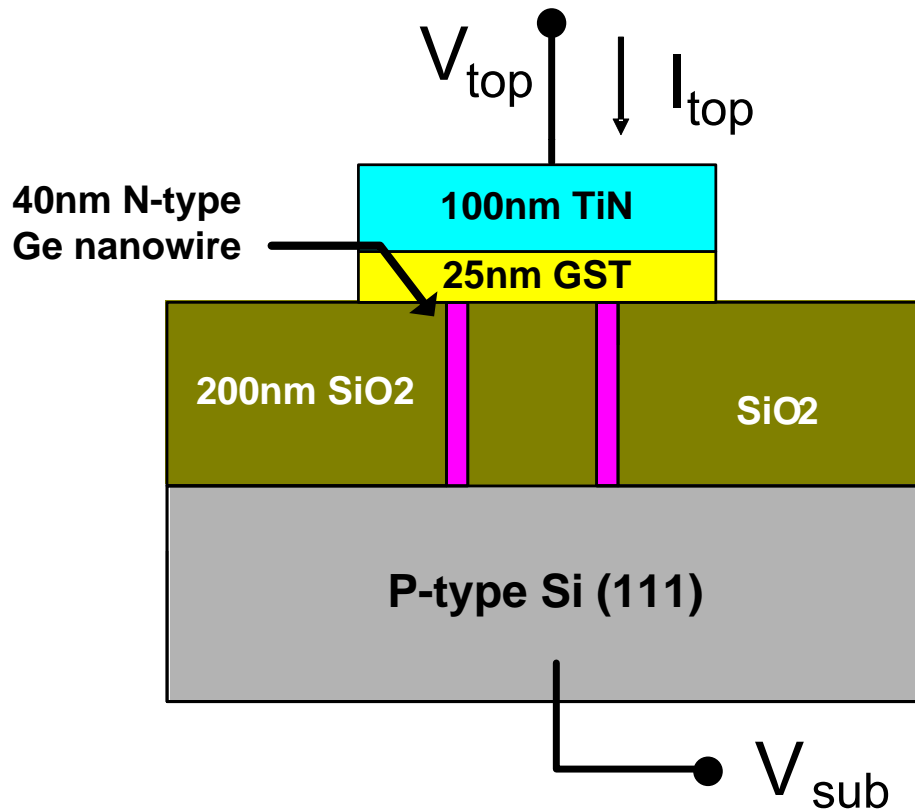
Insert Ti between TiN and Si to reduce  $R_{\text{contact}}$



Y.Sasago et al., Symp. VLSI Technology, p. 24, 2009. (Hitachi)

# Diode Example: Ge Nanowire

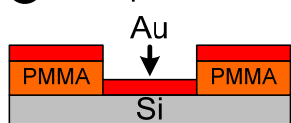
- Small diameter electrode, reduces programming current
- Route to pn-junction diode selection device
- Low-temperature (<350C) nanowire synthesis



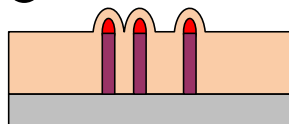
Y. Zhang, S. Kim, J.P. McVittie, H. Jagannathan, J.B. Ratchford, C.E.D. Chidsey, Y. Nishi, and H.-S. P. Wong, "An Integrated Phase Change Memory Cell With Ge Nanowire Diode For Cross-Point Memory," Symp. VLSI Technology, pp. 98 – 99, June 12 – 14, 2007, Kyoto, Japan. (Stanford)

# Nanowire Diode + Phase Change Memory

① Au deposition



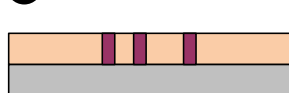
⑤ Oxide deposition



② Lift-off



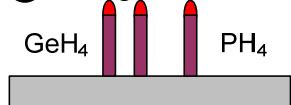
⑥ CMP



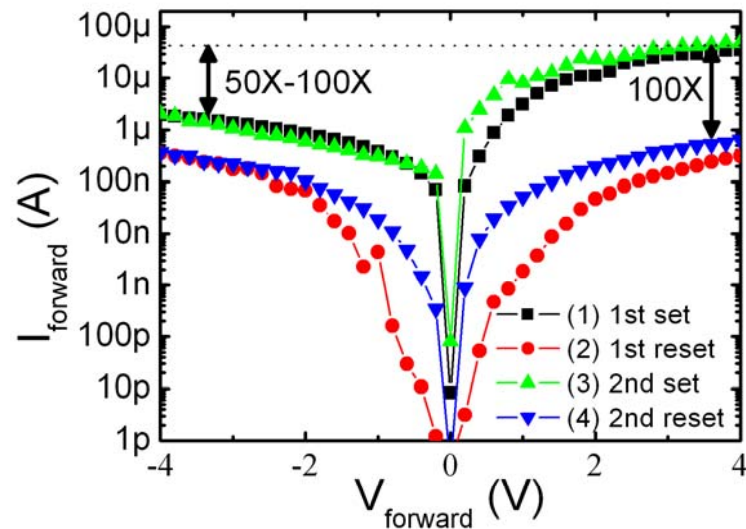
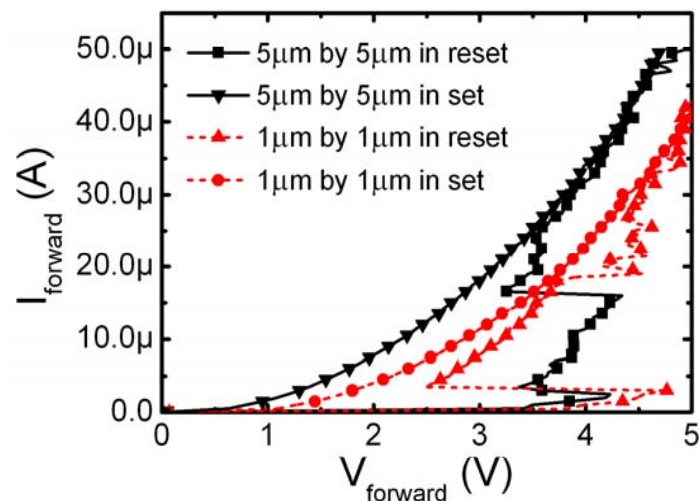
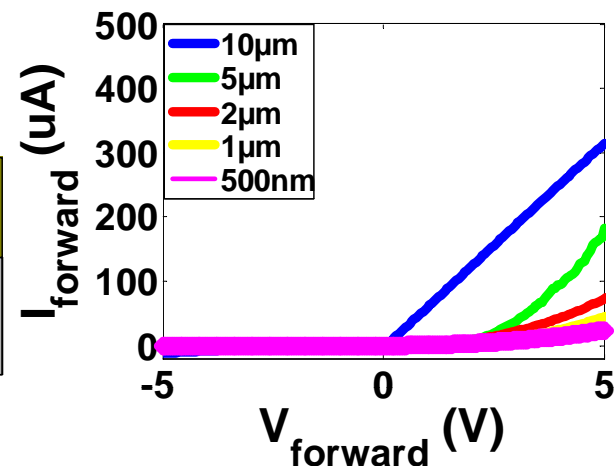
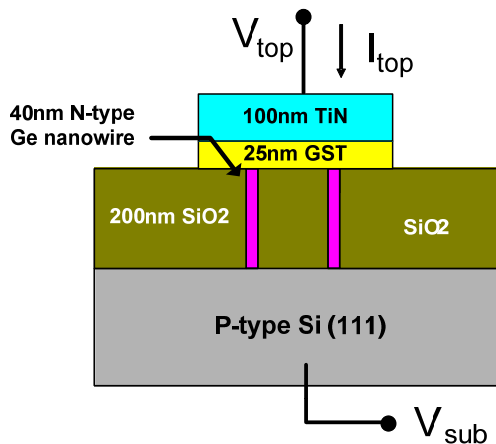
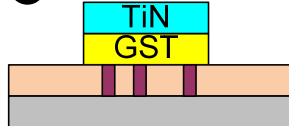
③ Au-Ge droplet



④ VLS growth



⑦ PVD+Lift-off



S. Kim, Y. Zhang, J. McVittie, H. Jagannathan, Y. Nishi, H.-S. P. Wong, "Integrating Phase Change Memory Cell with Ge Nanowire Diode for Cross-Point Memory – Experimental Demonstration and Analysis," *IEEE Trans. Electron Devices*, vol. 55, No. 9, pp. 2307 – 2313, September, 2008. (Stanford)





# Non-Volatile Memory Technology Research Initiative (NMTRI) at Stanford University





# Sponsors and Collaborators



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