Low-Power and High-Performance SRAMs in Nano-Scale CMOS Technology

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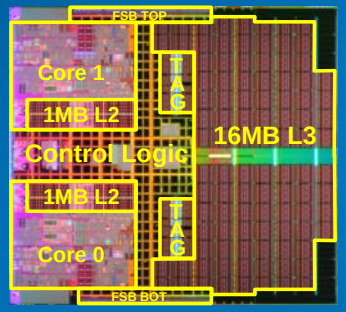
Outline

- Why SRAM?
- Scaling Challenges & Solutions
- Summary

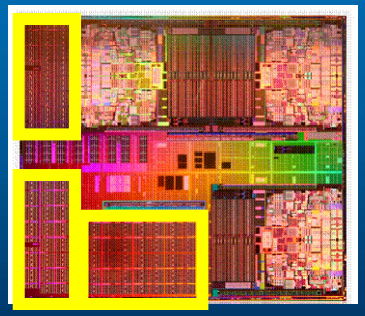
SRAM for High-Performance Computing

- Number of computing engines will continue to grow, as memory bandwidth requirements become increasingly challenging
- SRAM continues to play essential role in memory hierarchy

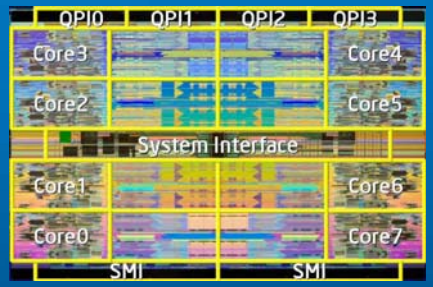
Intel Xeon© Processors



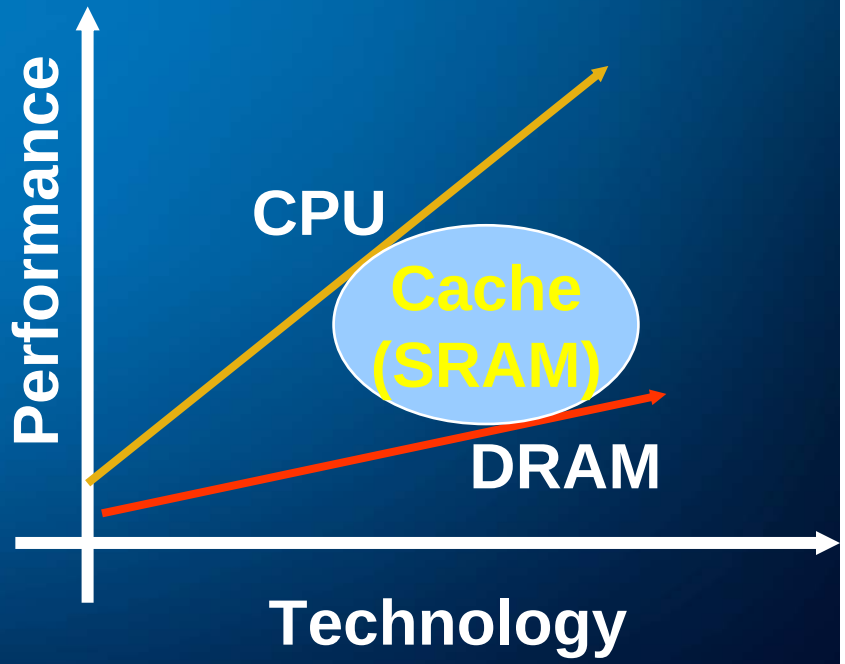
2 Core/16MB LLC



6 Core/16MB LLC

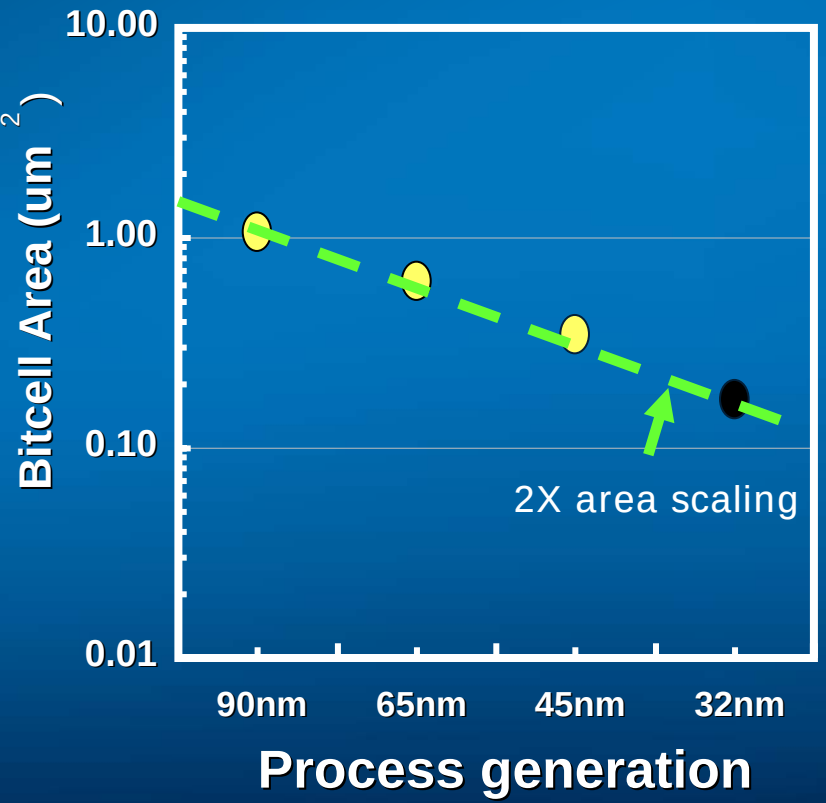


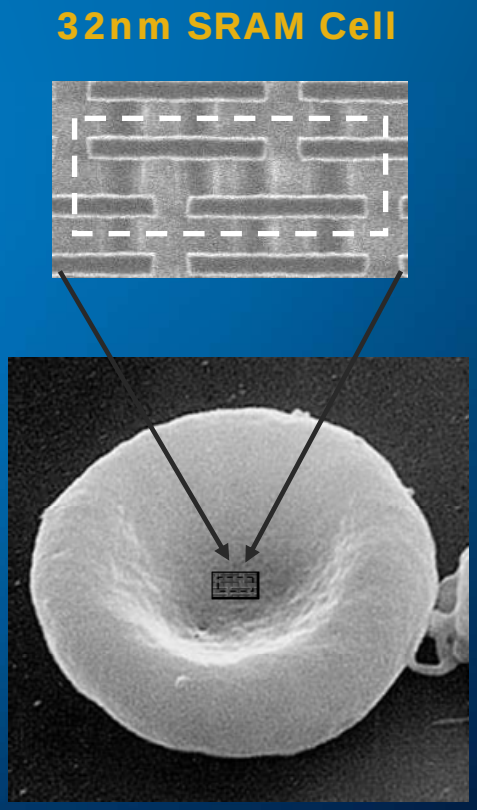
8 Core/24MB LLC



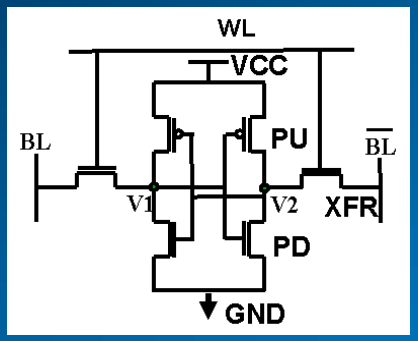
SRAM Scaling Trend

- SRAM scaling exemplifies Moore's Law in technology scaling
  - Full-compatibility with Logic process continues to make SRAM the choice for embedded memory

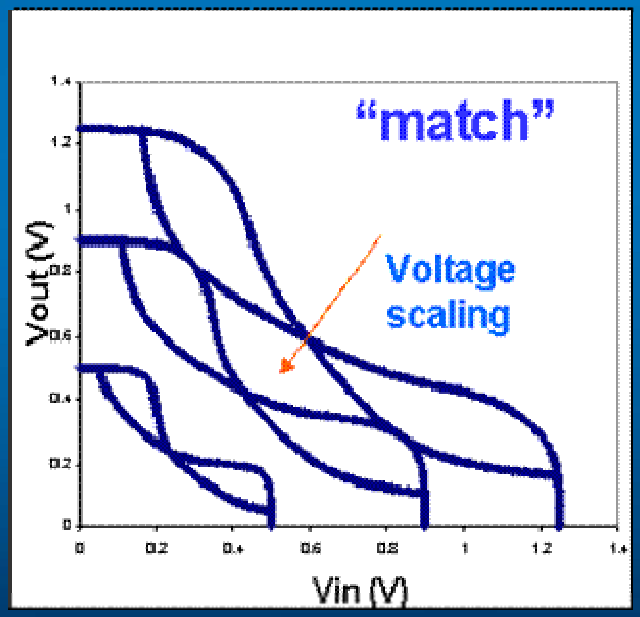


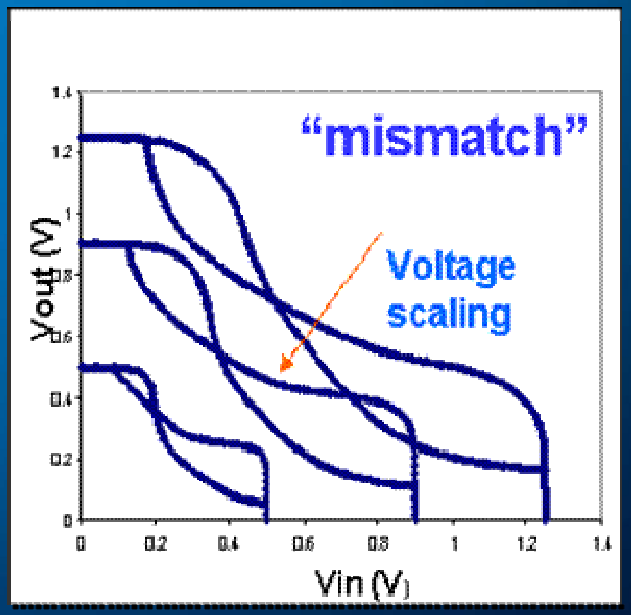


SRAM Scaling Challenge: Device Matching



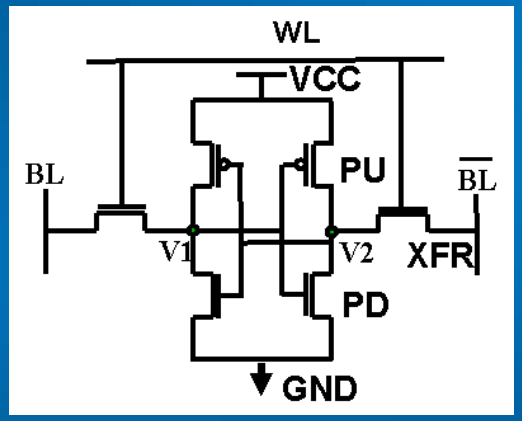
- SRAM stability depends on transistor matching, which is degraded by scaling

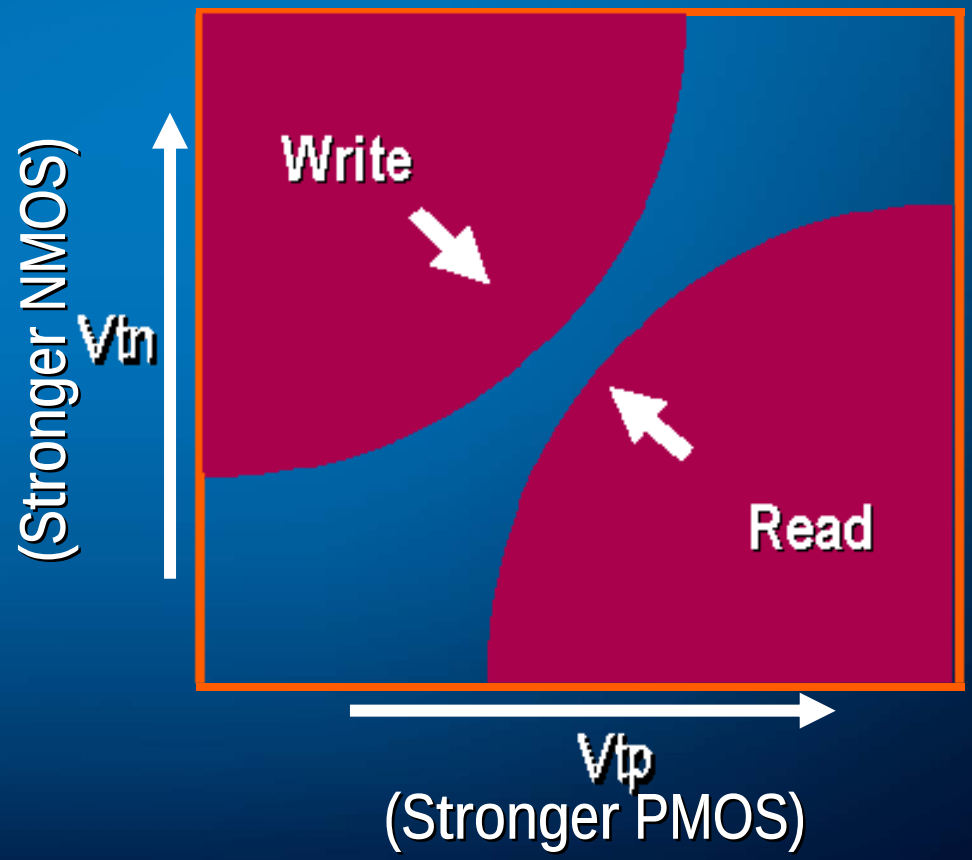




SRAM Design Paradox: Read vs. Write

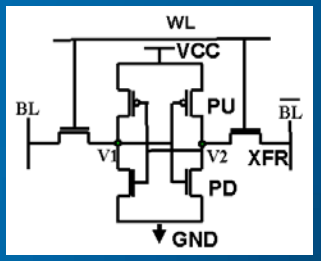
- Read-Write window is shrinking fast with conventional scaling
  - Adding more transistor has a steep area overhead

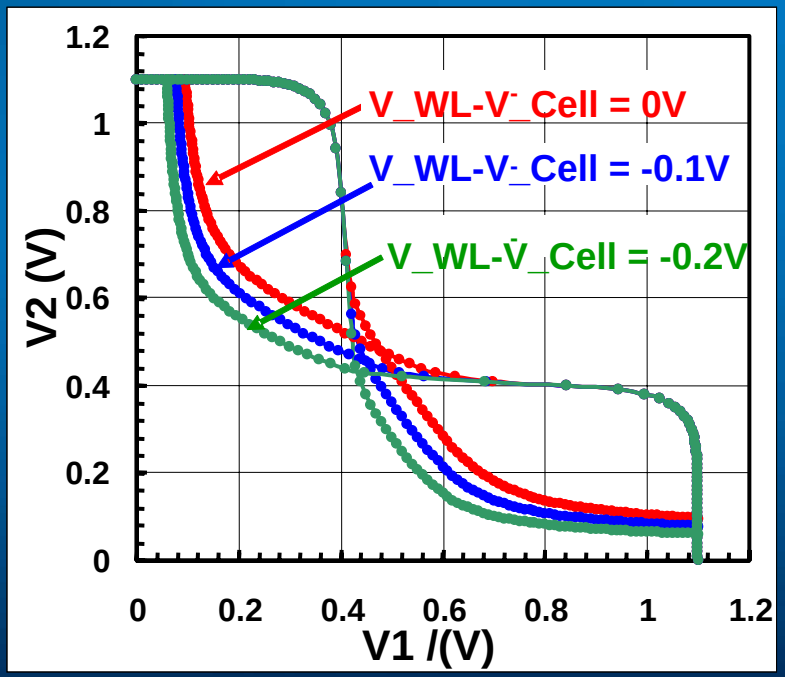


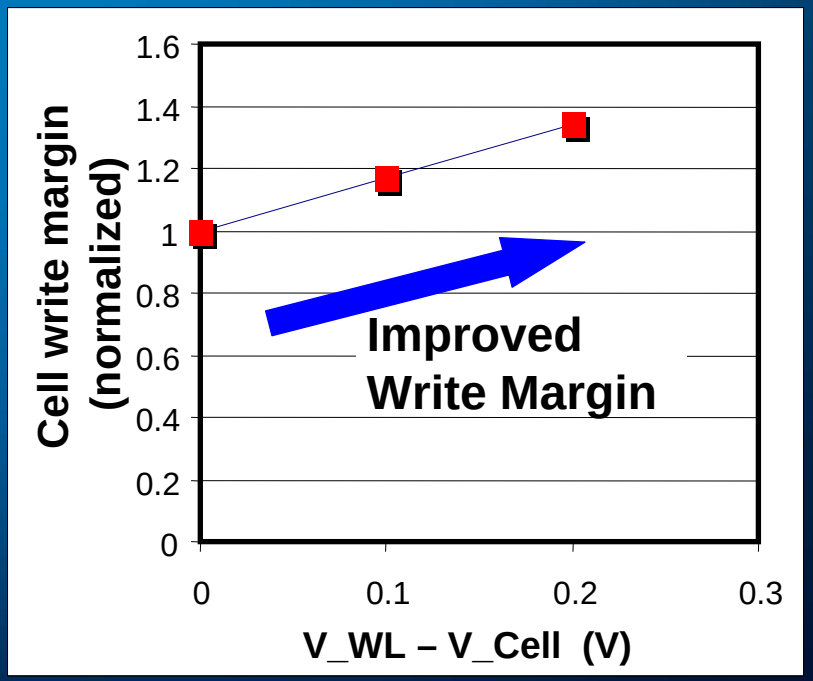


Multi-VCC: Enabling Future SRAM Scaling

- Creating a differential voltage between WL and Cell VCC opens-up Read & Write design window
  - Write: V_WL > V_Cell
  - Read: V_WL < V_Cell

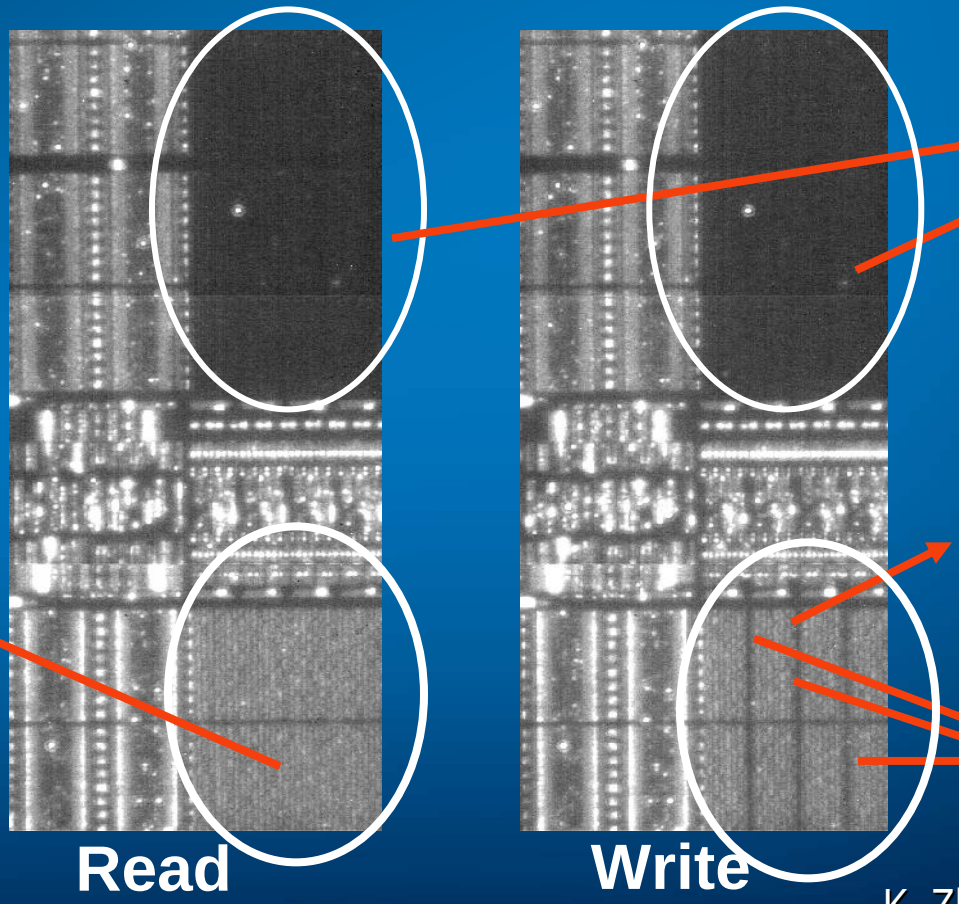






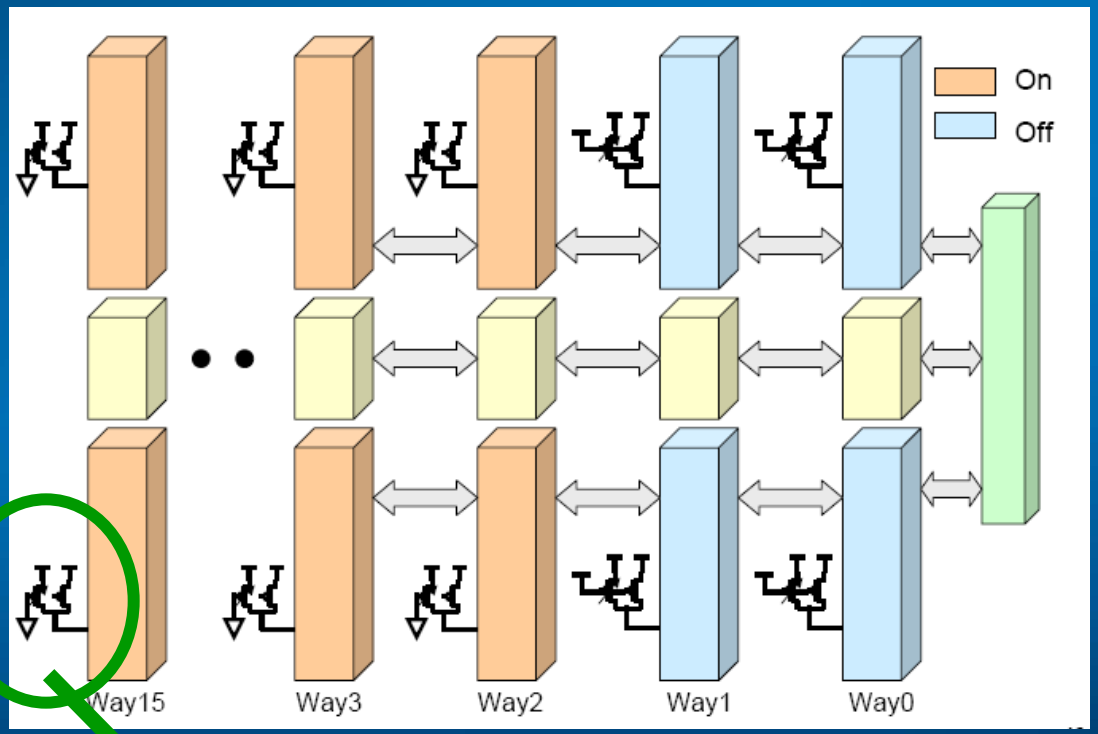
Dynamic Multi-VCC Design
(Infrared Pictures)

- Multi-VCC reduces leakage/standby power



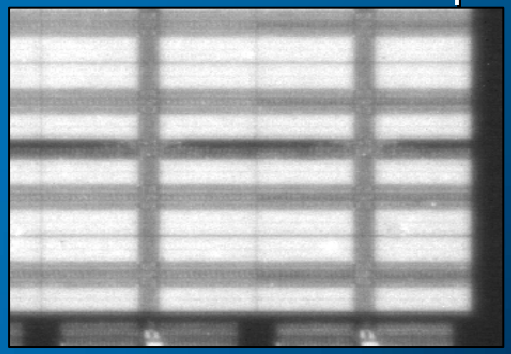
K. Zhang et. al,
ISSCC'05

Dynamic VCC for Power Management - Smart Cache Memory

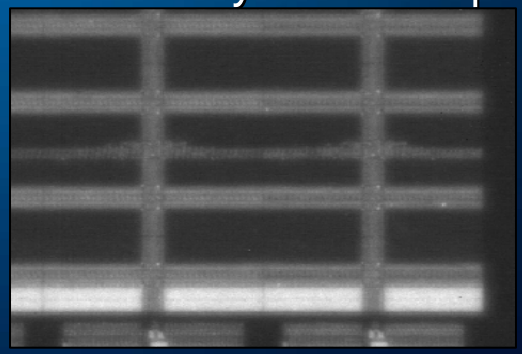


Dynamic Control

without sleep



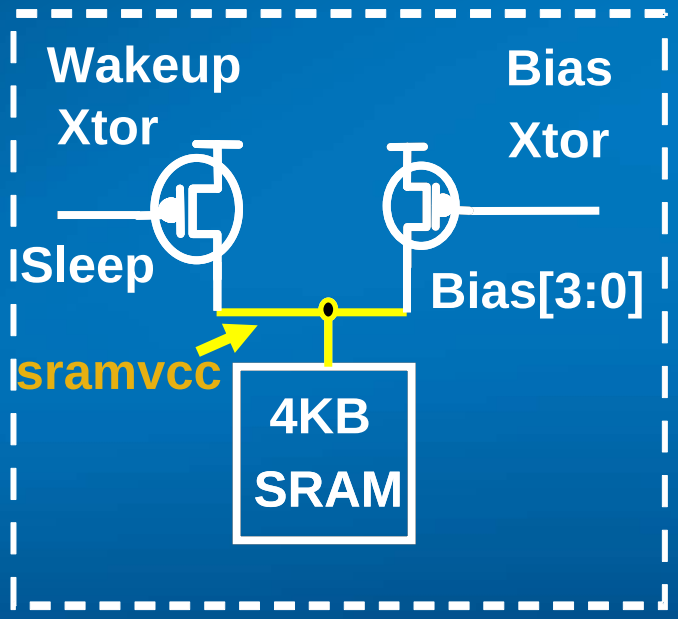
Dynamic Sleep



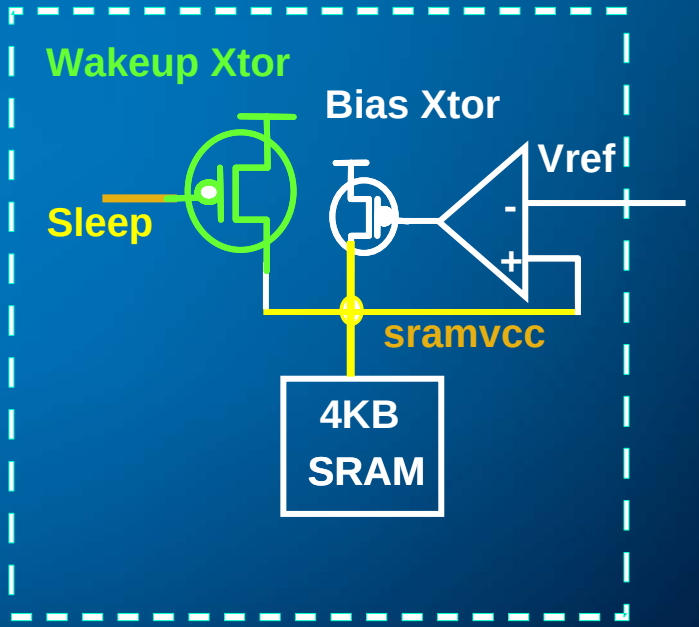
K. Zhang et al., VLSI' 04

Adaptive Design in SRAM

- Adaptive design has become increasingly important to overcome variations and achieve optimal design benefits



Passive Control



Active Control

Y. Wang et al, ISSCC'09

Summary

- SRAM remains the main workhorse in embedded memory for logic applications
  - Balanced power/performance/cost
- Process-Circuit innovations are expected to help the SRAM scaling well into the future