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NRI TPG Teleconference
Wednesday, November 10, 2010
4:00-6:00p Eastern / 3:00-5:00p Central / 2:00-4:00p Mountain / 1:00-3:00p Pacific

Attendees:
Jeff Welser (NRI)
Allison Hilbert (NRI)
Steve Kramer (Micron)
Gurtej Sandhu (Micron)
Luigi Colombo (TI)
Bob Doering (TI)
C.Y Sung (IBM)
Tak Ning (IBM)
George Bourianoff (Intel)
Zoran Krivokapic (GF)

*****Please refer to charts shown in WebEx. They are on the NRI website. From My SRC page, go to the bottom and click NRI Technical Program Group, then click on Meeting Results tab*****

Agenda:

Discuss Revised Phase 1.5 Proposals

WIN:
Revised device categories and plans to account for the lack of UC Discovery matching funds. Replaced the original Theme 4 work on RT devices with work on Wang's DMS SpinFET, and eliminated the Stanford work on the spin-torque "rabbit-ear" device and circuits. Note this means Stanford is not in WIN any longer; Awschalom will still be a part of the spin wave work, doing imaging of the spinwaves. Details on the revised budget are in the charts.

MIND:
Primary adjustments made to meet the budget: Eliminated Appenzeller's Exciton FET; reduced Notre Dame management costs (more in line with the other centers); small cut in PSU budget. Carry-over and additional matching from ND and the state covered the rest of the shortfall (including the management costs) for ND.

Okay with the budget/plan overall, but some concerns / feedback for Jeff to give to MIND:

- Large amount of architecture/circuit folks in NML – will they be able to actually build demonstrations, or just doing modeling? Be sure they focus on demonstrating the key circuit elements (e.g. clocking, full system energy measurements, etc.). Also be sure they choose demonstration circuits which are relevant to an important application space – and that show clear advantage for NML (low-power, competitive performance, etc). [Note: this is also what they need to be doing for the DARPA program, so hopefully will be good synergy.]
- Continued concern about whether the TFETs (particularly the III-V TFETs) really below in NRI. Re-iterate that they are only acceptable in Phase 1.5 because we want to see –

once and for all – if they can really compete with CMOS or not. Even if they do show good results, they will likely move to FCRP or GRC after that – will not be a part of Phase 2.0, so keep that in mind.

- Encourage them to focus on the more revolutionary tunneling devices – graphene and nanowires – as more in line with NRI, as well as other novel uses of tunneling. Really want to see clear results on the graphene device in particular.

→ Jeff will give feedback to Seabaugh directly on these points.

Side Topic:
Luigi: How are we going to mentor these programs to make sure we guide what's going on.
Jeff: We should assign one assignee to each device. Not just to keep us (TPG) abreast of what's going on, but also to keep the professors on track and make sure they are making progress toward gathering the key data we want to see in Phase 1.5.
All: We need to be clear with the assignees that they are liaisons and facilitators – not project managers, per se. They should be helping the projects – acting as additional (free) researchers – not judging/reviewing them. In particular, if a project hits a snag, they should be finding ways to help get over the snag – fabrication / characterization help including in industry or NIST labs, if it makes sense.
→ Jeff will be meeting with the assignees in January to "sign them up" to different devices and kick this effort off.

INDEX:
Revised proposal maintains the primary focus on the two devices (Graphene pn junctions and All-Spin-Logic) plus the Graphene fabrication and metrology work, but with much more streamlined teams. In particular, reduced the number of people working on characterization, fabrication, materials development, and architecture, but maintained a core group in each area to address the primary areas of need for the two devices.

Okay with the budget/plan overall, but some concerns / feedback for Jeff to give to INDEX:

- Be sure to focus any graphene materials work just on material needed for the devices (not too many different kinds). Noted that deHeer's epi work at GIT had been cut, but P. Ye's epi work would still be used for the ASL devices, while CVD-graphene and flakes are more likely to be used for the pn-junction devices. So haven't narrowed down to just one graphene type, but at least have focused on just making material for the devices themselves (not just for materials exploration).
- Questions on whether some of the PI's in the revised budget will really be focused on advancing the device efforts:
    - P. First (GIT) – is this metrology crucial for the devices? And is he doing it or NIST? (Clarified: it is done largely at NIST, but with First's students who are funded by NRI). Work does seem to be important for understanding transport in graphene – and is planning to focus on spin transport in particular for ASL
    - C. Marcus – great physics work, but will it really advance the device work? It was pointed out that his p-n work has formed the basis of the interconnect and device concepts up to now, so it should be well linked – but do want to be sure he is focused on overcoming the specific hurdles for getting a working device.
    - P. Kim – similar comments to Marcus.

- On ASL device, continued concern about whether it can be scaled down enough that the currents required aren't too high. The PI's indicate that they think going to smaller magnets (fewer spins to flip) will allow scaling to reasonable currents, but must also worry about the inefficiency of converting from the direct current (which flips the input MTJ) to spin diffusion current (to flip the output). Need to focus on demonstrating that these currents can be low enough to be reasonable.

→ Jeff will give feedback to Lee directly on these points. In particular, will ask him to make sure the SOW's for First/Marcus/Kim (and any others) clearly show how they are working on specific topics to overcome one or more of the primary "obstacles" to the device demonstrations. Should have a clear list of the top 5 or so obstacles the center needs to attack.

Summary & Next Steps:
The TPG is now comfortable with all of the proposals for Phase 1.5, the comments above notwithstanding. The consensus is that the Directors have done a good job of responding to our requests – and staying within the stated budgets – so we should give them the final feedback above and let them proceed to run their centers. TPG is happy with the balance NRI has been striking between giving clear direction while not micro-managing, so that the PI's have sufficient autonomy as well.
The proposals will be sent to the GC for their final approval at the December meeting. The TPG reps should be ready to answer questions from their GC member.

Summary of 2010 Member Satisfaction Survey
Median Scores were GC 5; TPG 4.5
Planned actions for next year:

- In Phase 1.5 balance focusing on the current most-promising while maintaining a search for new device ideas in parallel (since no clear winner)
- Ensure focus is on demonstrating key attributes needed by any "new switch" (e.g. low energy) without limiting the search only to non-charge-based devices.
- Increase the effort on experimental verification of promising theoretical predictions and be sure industry assignees stay closely involved.
- Continue and expand the benchmarking work to consider new device attributes (e.g. non-volatility) that could be exploited not only for improved computation performance, but also for other spin off technology areas, including memory. Increase focus on IP creation for any interesting device or circuit applications that are discovered.
- Continue to look for expanded government partnerships to maintain high leverage for the program.

George: What's the status of government funding for new tools and infrastructure – this seems like an increasing limitation in the U.S. (compared to other countries) for some of these new device and materials (e.g. magnetic material etching)?
Jeff: Nanoelectronics 2020 and Beyond has this as one of its primary goals, but the budget realities make it uncertain. Met with the NIST director earlier this week and are trying to use the Nanofab at Gaithersburg as a way to meet some of the fab needs for NRI. He was very positive on continuing – and expanding – the NRI partnership (budgets allowing), so it appears to be a good potential for us.

→ Jeff will talk to the Directors, and the assignees, in January about coming up with a list of specific areas where new tools are needed to enable us to do the critical device demonstrations.

Will need strong SIA support with Congress to convince them that research is an "investment" not an "expense".

Bob: I guess each of us has to go to a Tea Party meeting!

IP Review Process Discussion
Heard from 3 of 5 companies. Having the TPG review it and use the Power Point rating seems effective, and we will continue to look for ways to improve the PPT content to make it as helpful as possible for facilitating reviews.
→ Jeff will also encourage the assignees to look for more IP disclosure opportunities for the specific devices they are monitoring.

Open Mic
No comments

Meeting adjourned.

Next NRI TPG meeting is currently scheduled for:
Date: Wednesday, December 1, 2010
Time: 4-6p Eastern / 3-5p Central / 2-4p Mountain / 1-3p Pacific