

## **Onsite Review: Midwest Institute for Nanoelectronics Discovery (MIND)**

Tuesday, August 10, 2010 • University of Notre Dame, McKenna Hall

8:00 Continental breakfast

8:30 Welcome and opening remarks – Alan Seabaugh (ND) and Jeff Welser (NRI)

### **Session I – INTERBAND TUNNEL TRANSISTORS**

9:00 Lateral field-effect tunnel transistors, P. Fay, T. Kosel, A. Seabaugh, and G. Xing, ND

9:30 Vertical heterostructure tunnel transistors, S. Datta, T. Mayer, and D. Schlom, PSU/Cornell

10:00 1-D nanowire tunnel transistors, T. Mayer, S. Datta, and V. Narayanan, PSU

10:30 Break

### **Session II – GRAPHENE TRANSISTORS - THERMAL . SPIN . TUNNEL**

11:00 Thermal transport and thermal logic gates, Y. Chen and Z. Jiang, Purdue/Georgia Tech

11:30 Epitaxial spinFETs on Si, P. Ye, M. Capano, R. Wallace, and J. Kim, Purdue/UTD

12:00 Extremely scaled gated tunnel transistors, D. Jena and G. Xing, ND

12:30 Lunch – Irish Courtyard at Morris Inn

### **Session III – MODELING / MEASUREMENTS IN NONEQUILIBRIUM SYSTEMS**

1:45 Energy dissipation in nonequilibrium systems, E. Pop, Illinois

2:15 3-D quantum transport modeling, G. Klimeck, Purdue

### **Session IV – NANOARCHITECTURES**

2:45 Nanomagnet logic devices, M. Niemier, G. Bernstein, S. Hu, and W. Porod, ND

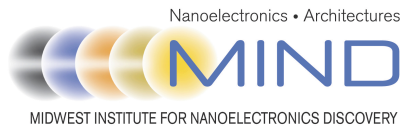
3:15 Break

3:45 THz logic using plasmonics, P. Mazumder, MI

4:15 Review of NRI technology benchmarking, K. Bernstein, IBM

4:45 MIND: Going forward, A. Seabaugh, ND

**5:00-7:00 POSTER SESSION AND RECEPTION – Stinson-Remick Hall, 1<sup>st</sup> floor Commons**



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9:00 Industrial Advisors Caucus – Auditorium

PI Caucus – Room 100-104

9:15 Project planning meetings – Room 100-104 and foyer

Interband Tunnel Transistors – Alan Seabaugh

Graphene Transistors – Debdeep Jena

Nanoarchitectures – Wolfgang Porod

10:00 Review and Feedback – All PIs should attend

11:00 Adjourn