Design and Foundry Collaboration to Ensure Silicon Success (Abstract)

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Abstract

A new collaboration model between foundries and design teams is presented to ensure first-pass silicon success, which has been the corner stone of fabless design and foundry industry.

The necessity of the new model is introduced through reviewing the major sources of variations on silicon chips: Deep-submicron device variation resulting from performance enhancement processing steps; Optical photo lithographical limitations; Layout and pattern density dependency effects; Increased global & local variations due to larger chip size and smaller shapes; Spice modeling limitations.

Primary and practical solutions to these variability are enumerated into two categories, processing and design; and are explained using TSMC 28-nm technology node as example: including model accuracy improvement, new circuit design initiatives; Restrictive Design Rules (RDR) implementation and optimization; Chip integration and EDA tools enablement.

Brief summaries and conclusions show that increased variability in 28nm and 20nm nodes can be successfully corralled through the new co-design-based collaboration method and that the tradition of first-pass silicon success will continue in the fabless design and foundry industry in 20-nm node and beyond.