Variability Prediction via TCAD Tools
(Physical Variability Simulation)

A. Asenov

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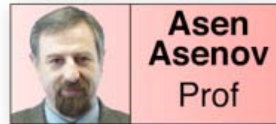
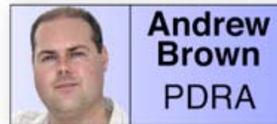
Device Modelling Group

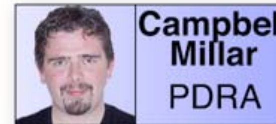
University *of* Glasgow

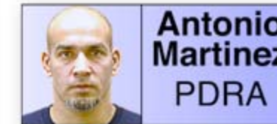
www.elec.gla.ac.uk/groups/dev_mo

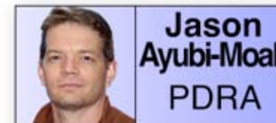
Staff

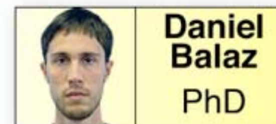












Summary

- Background
- Statistical variability
- Statistical reliability
- Statistical compact models
- Conclusions

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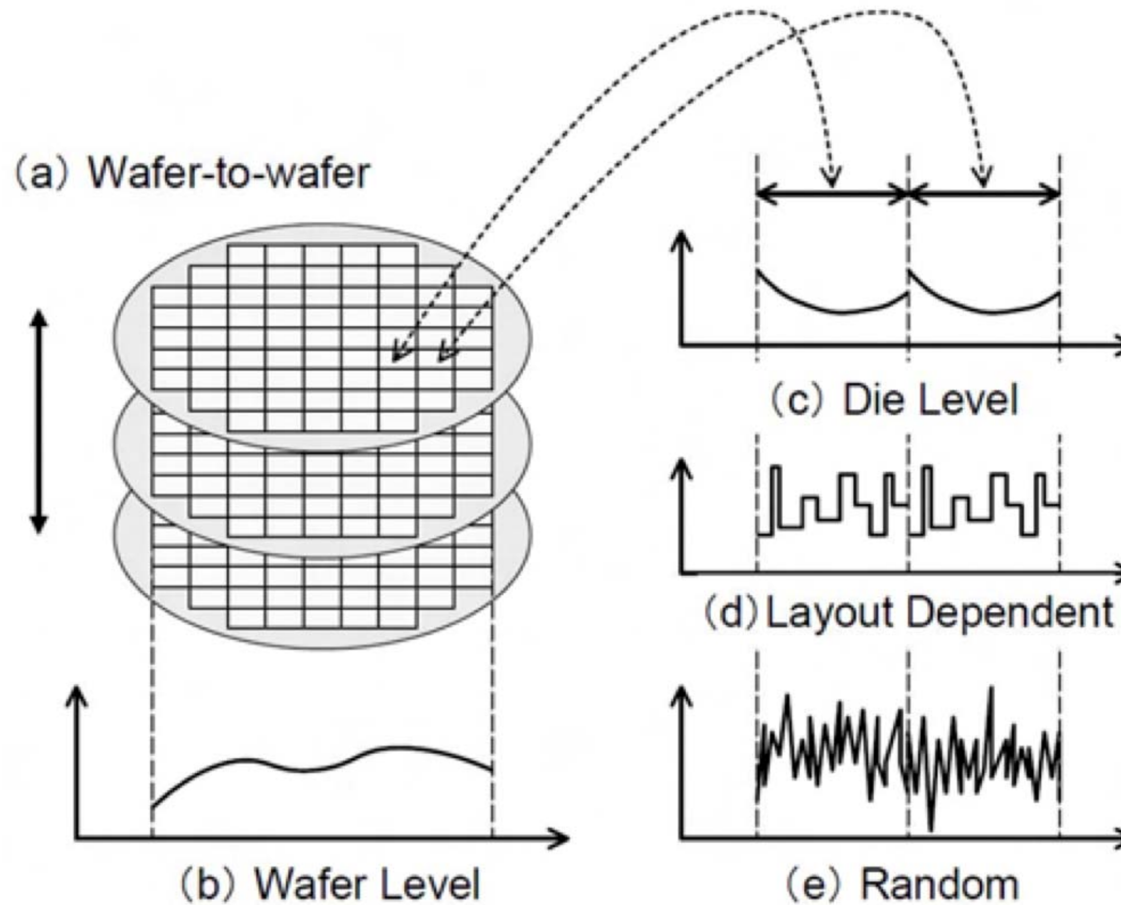
Variability classification



After K. Takeuchi (NEC)

Variability in 65 nm (L=60 nm, W=140 nm)

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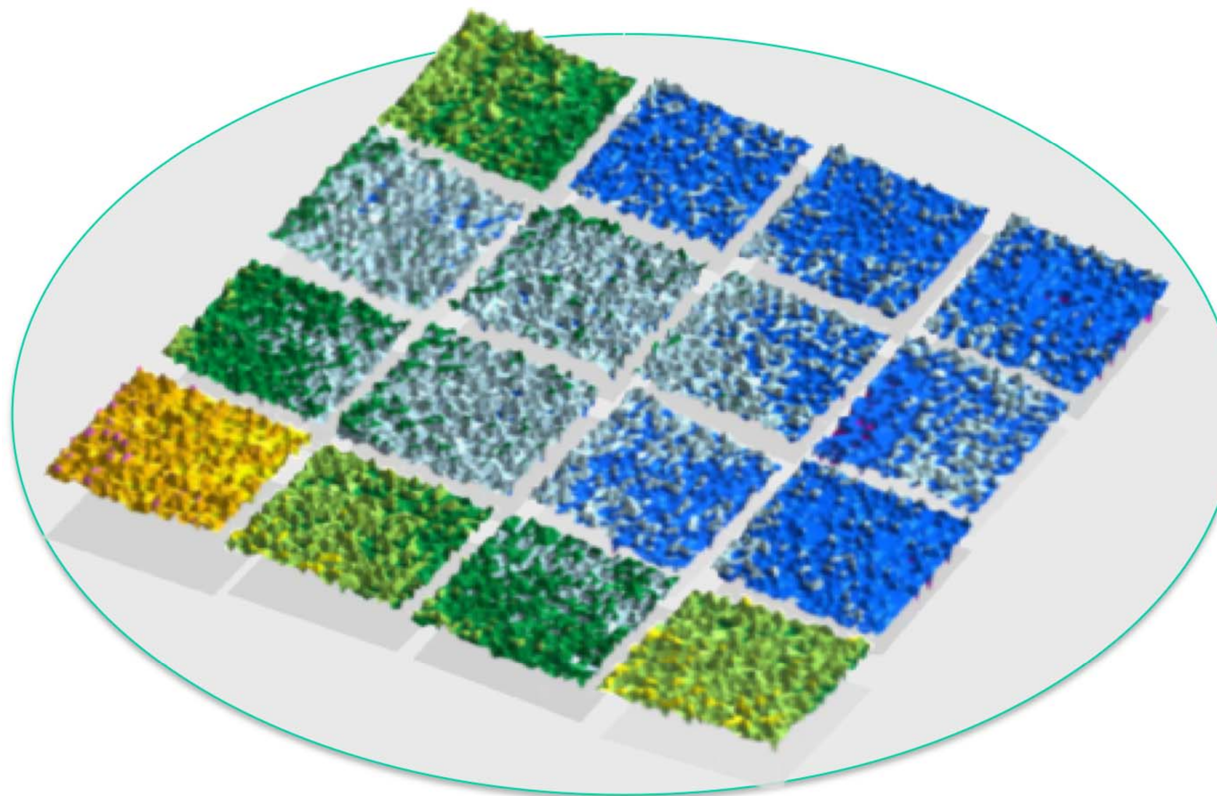
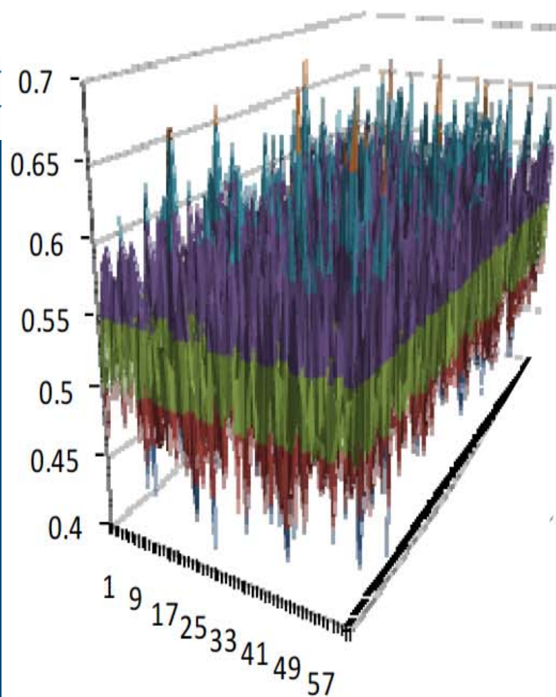
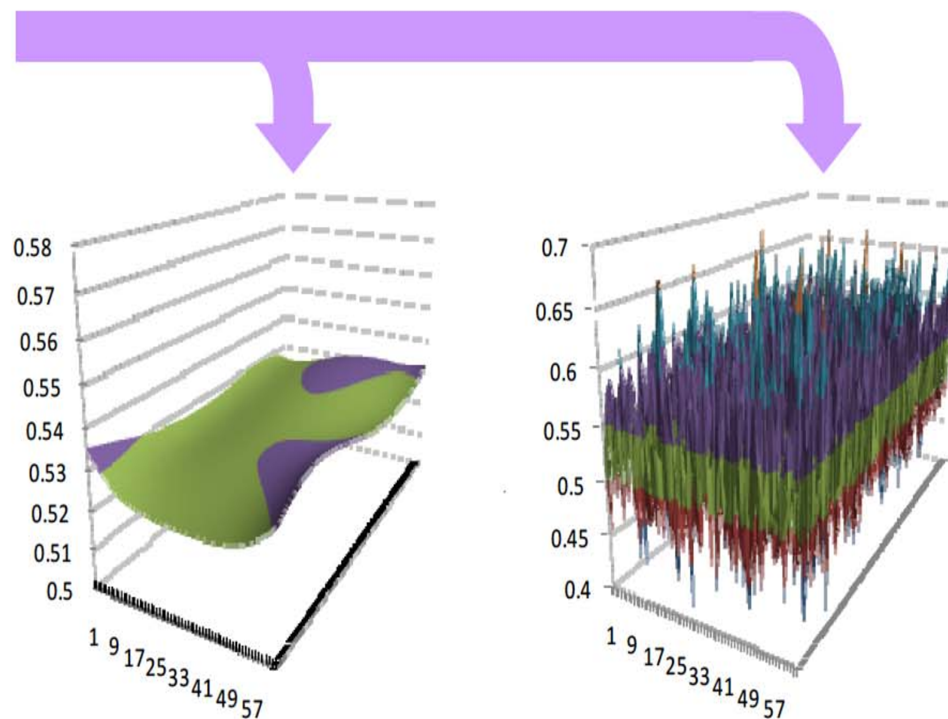


- 0.551-0.555
- 0.547-0.551
- 0.543-0.547
- 0.539-0.543
- 0.535-0.539
- 0.531-0.535
- 0.527-0.531
- 0.523-0.527
- 0.519-0.523
- 0.515-0.519

T. Hiramoto (Tokyo Univ)

Variability in 65 nm (L=60 nm, W=140 nm)





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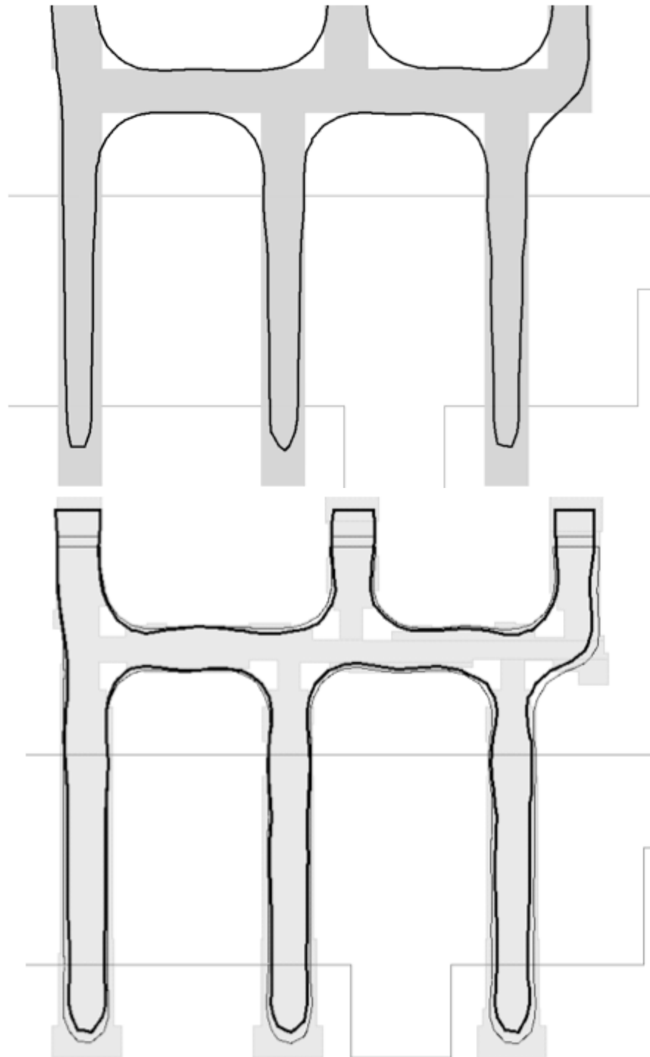
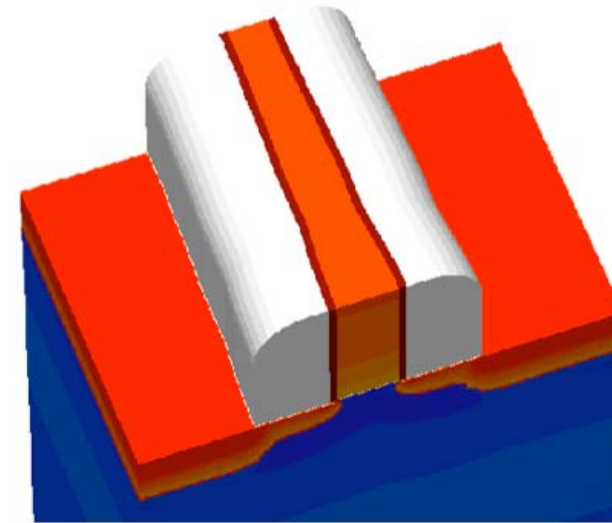
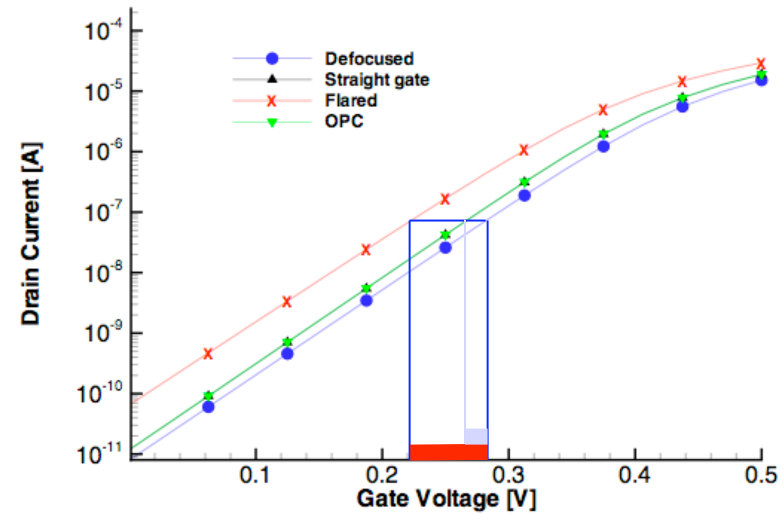
OPC and strain related variability

65 nm example Synopsys (SISPAD 06)







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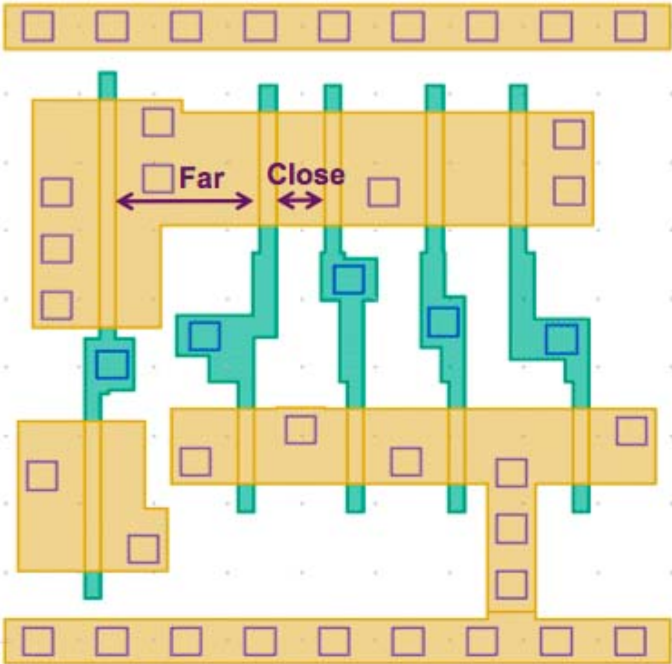
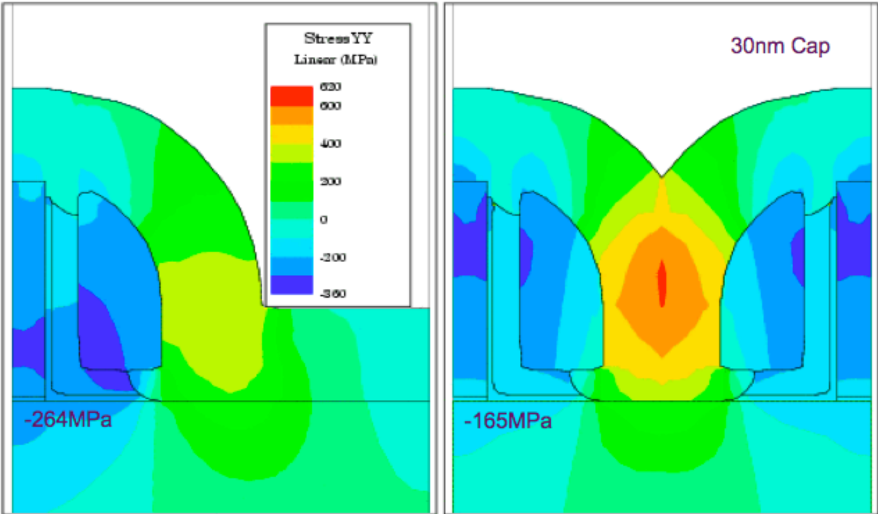
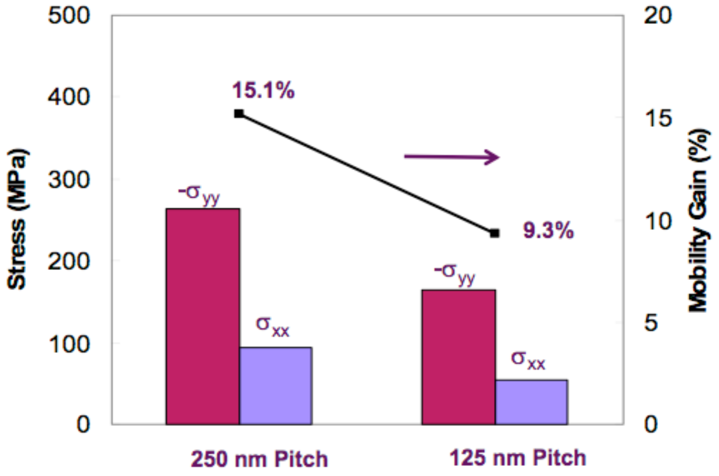
Strain induced variability

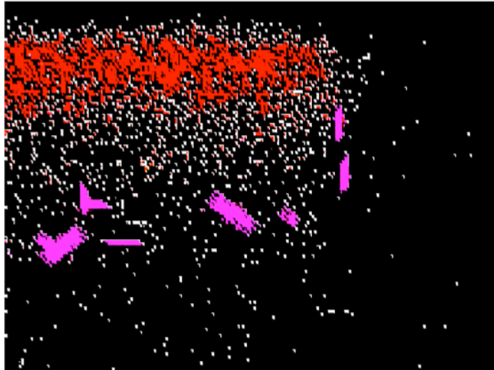
After W. Fichtner

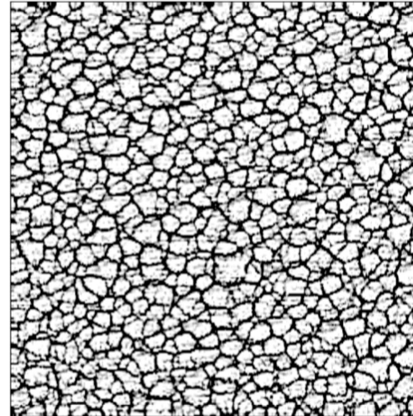


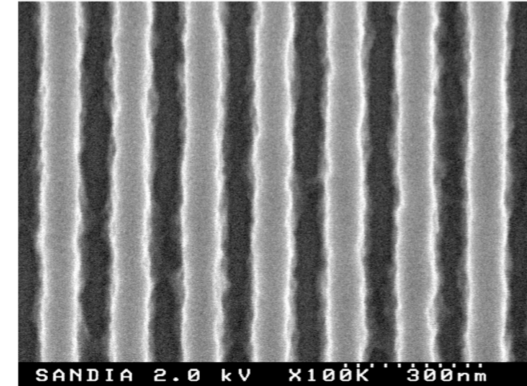


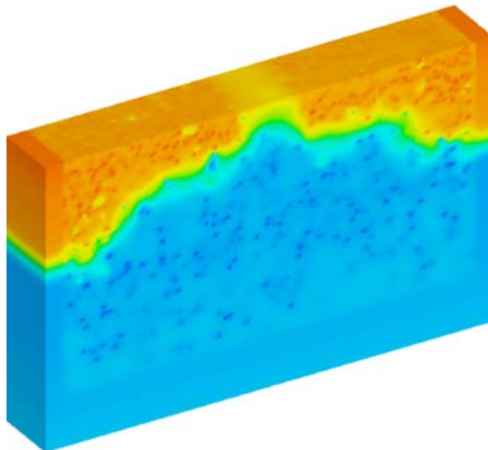


Statistical variability

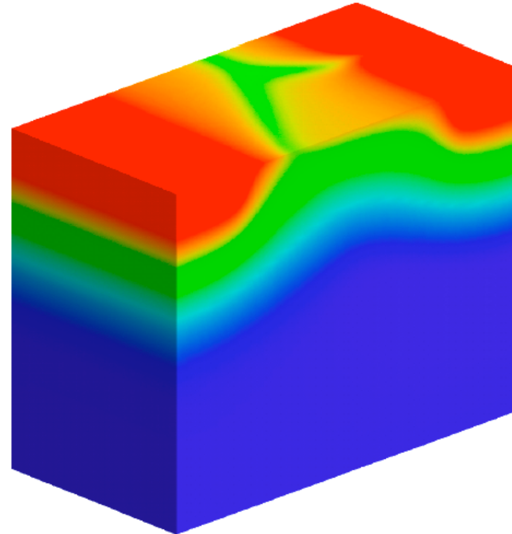




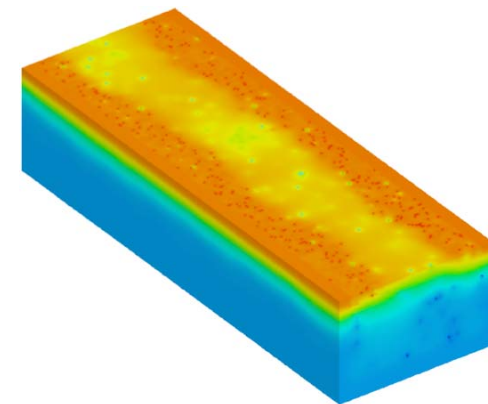




Random dopants

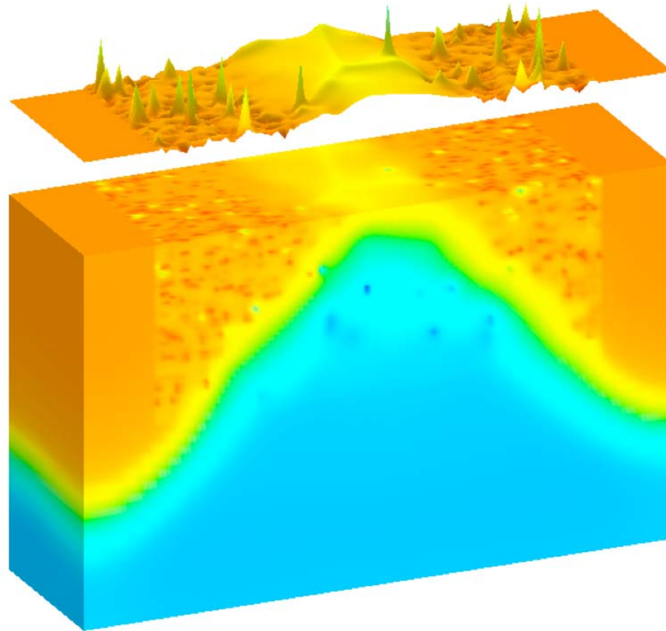


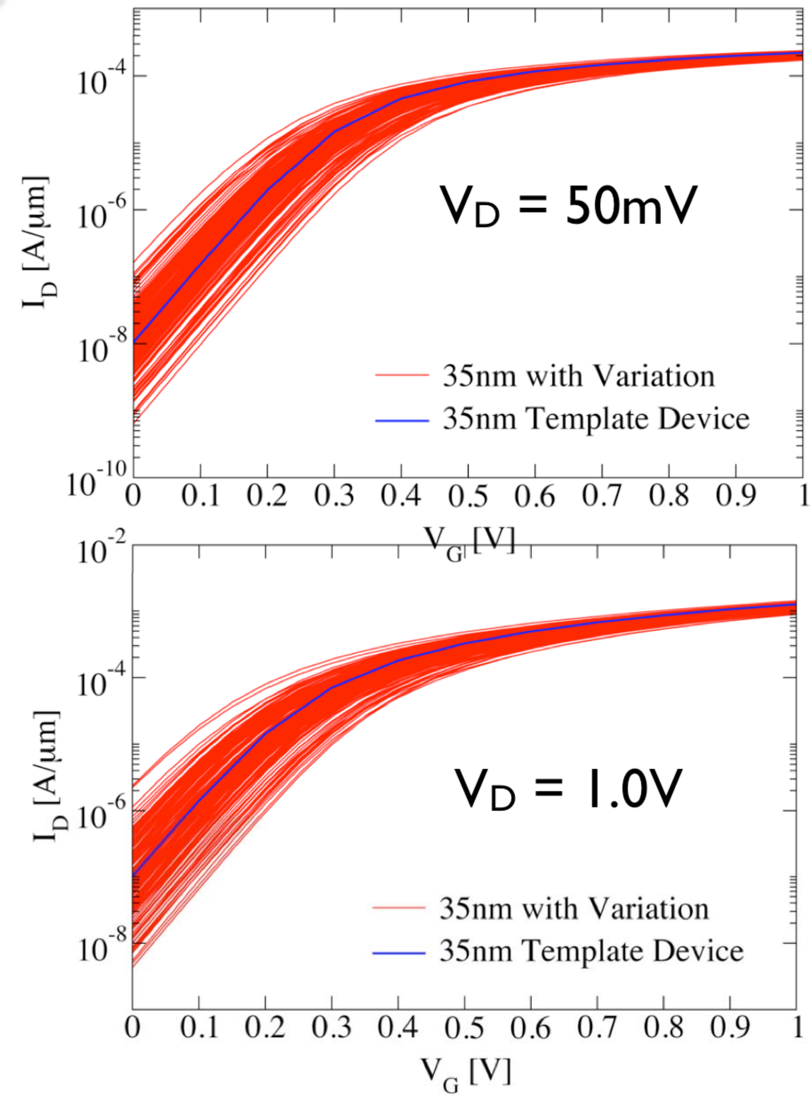
Polysilicon/high-k Granularity



Line edge roughness

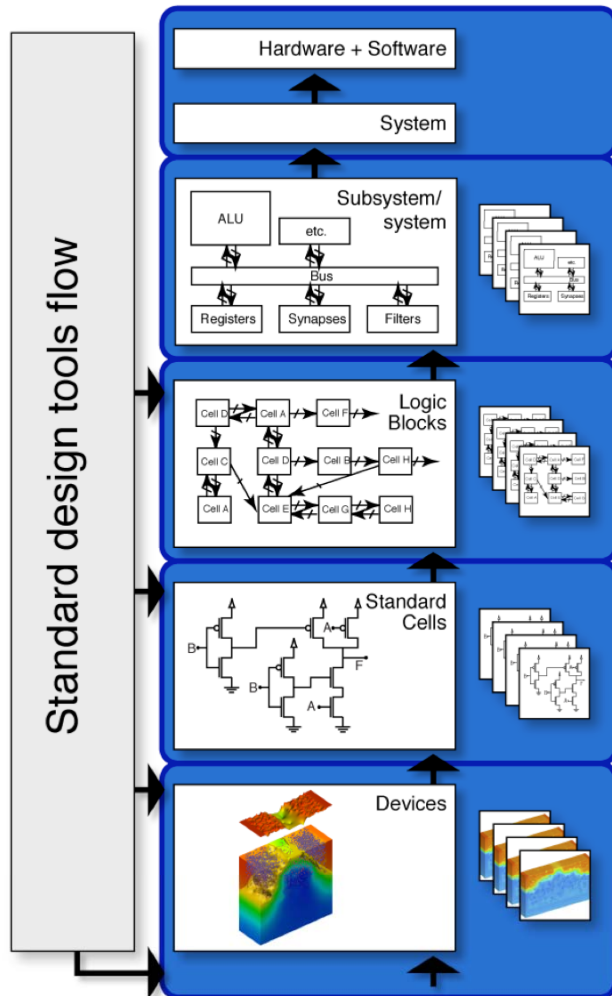
The most comprehensive technology available

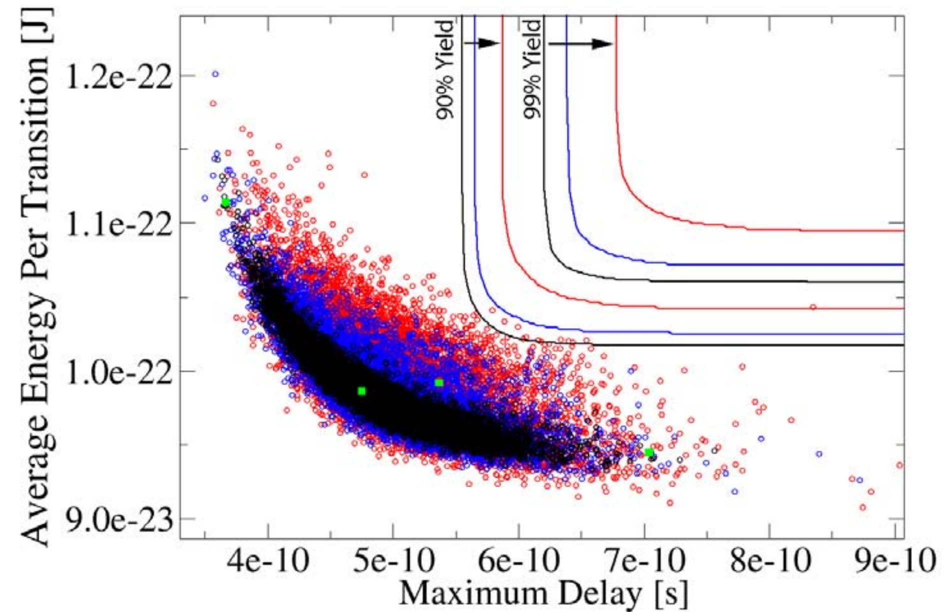




RDD+LER+PSG
Compact models

Hierarchical statistical simulation and verification





Performance/power/yield trade off is a necessity

Summary

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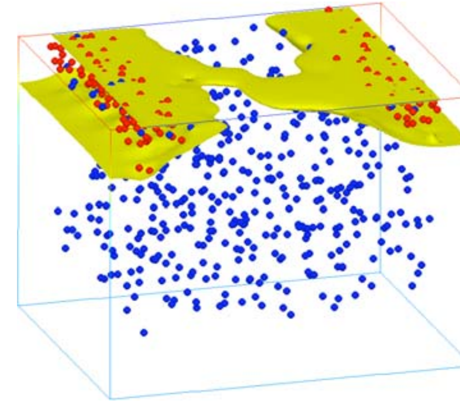
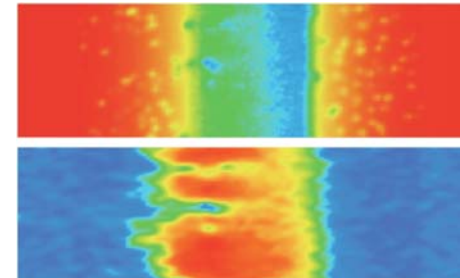
- Statistical compact models
- Conclusions

Glasgow statistical 3D simulation tools

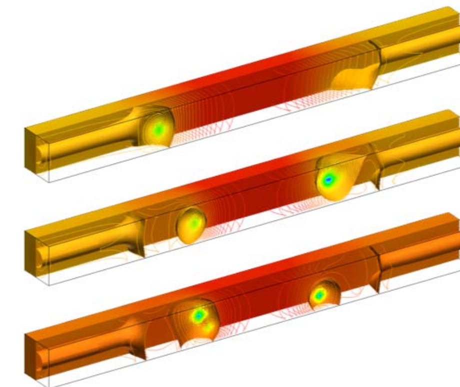
- Drift-Diffusion (DD) with quantum corrections.



- Ensemble Monte Carlo (MC) with *ab-initio* impurity scattering.



- Non-Equilibrium Green's Functions (NEGF).



Enabled by the power of cluster and grid computing

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VIA VERITAS VITA

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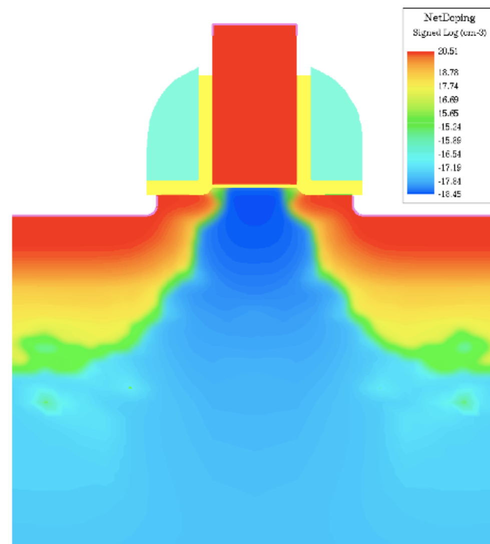
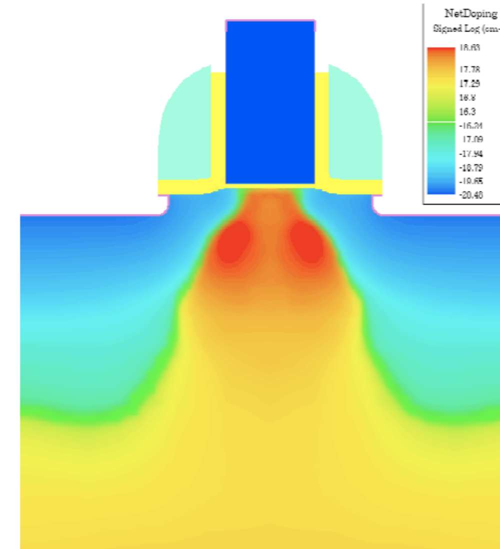
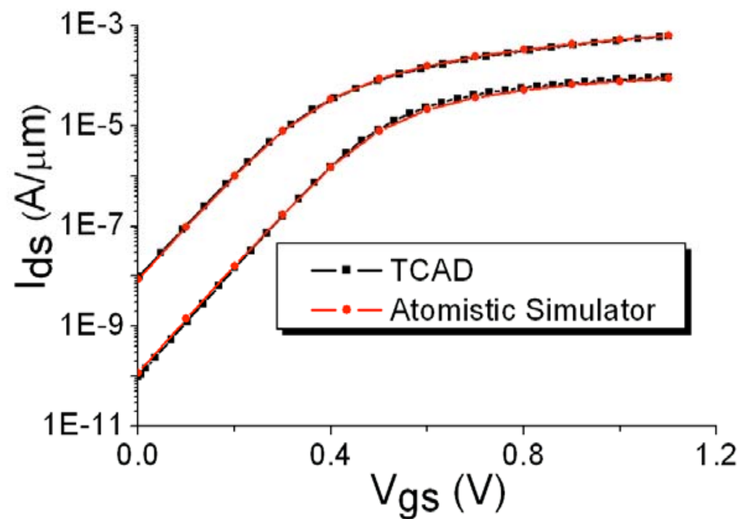
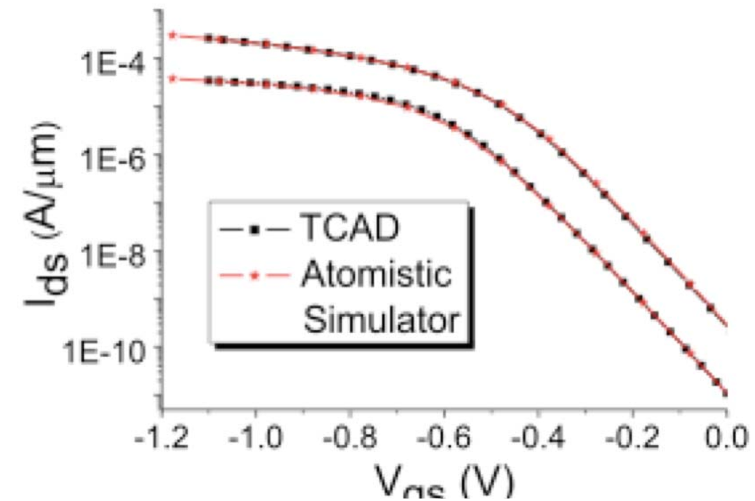
Variability in 45 nm LP transistors



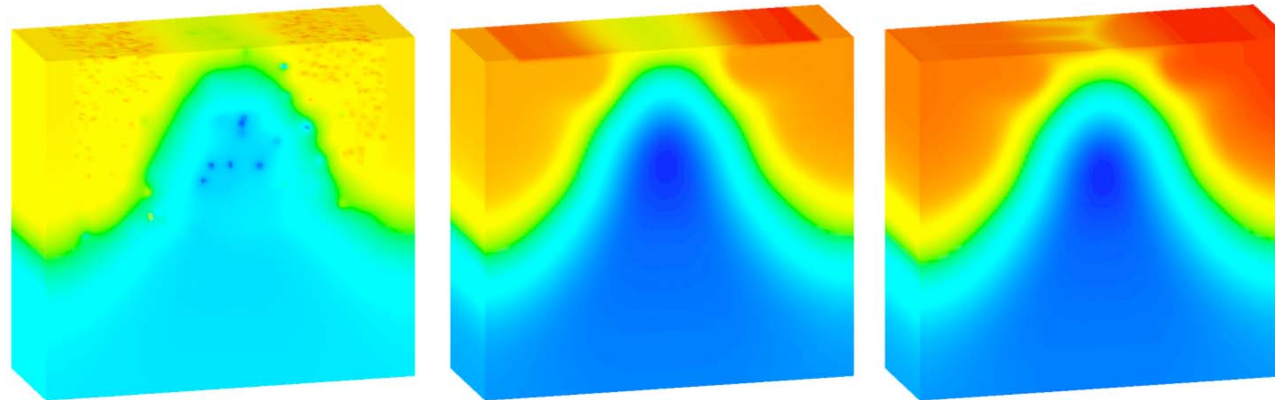






In collaboration with ST Microelectronics

Good agreement with measurements



	n-channel MOSFET		*p*-channel MOSFET	
	σV_T [mV] (V_{DS}=0.05 V)	σV_T [mV] (V_{DS}=1.1 V)	σV_T [mV] (V_{DS}=0.05 V)	σV_T [mV] (V_{DS}=1.1 V)
RDD	50	52	51	54
LER	20	33	13	22
PSG	30	26	-	-
Combined	62	69	53	59
Experimental	62	67	54	57

VIA VERITAS VITA
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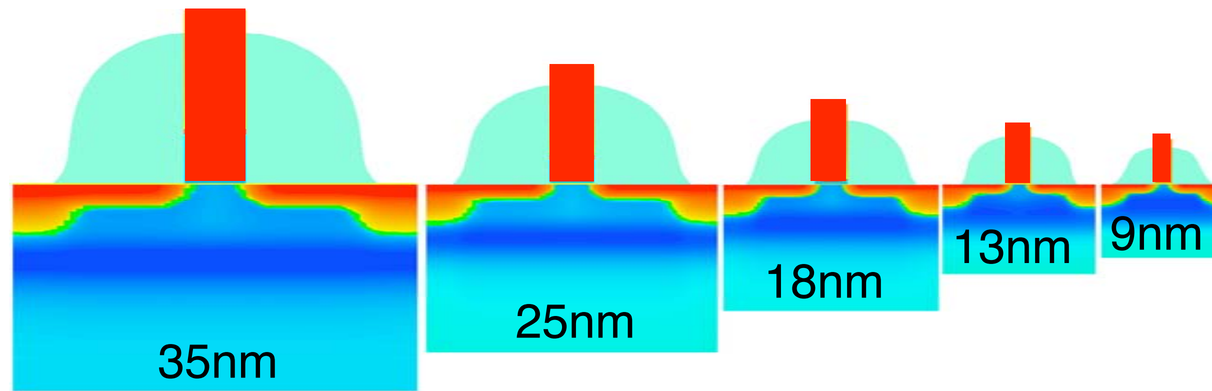
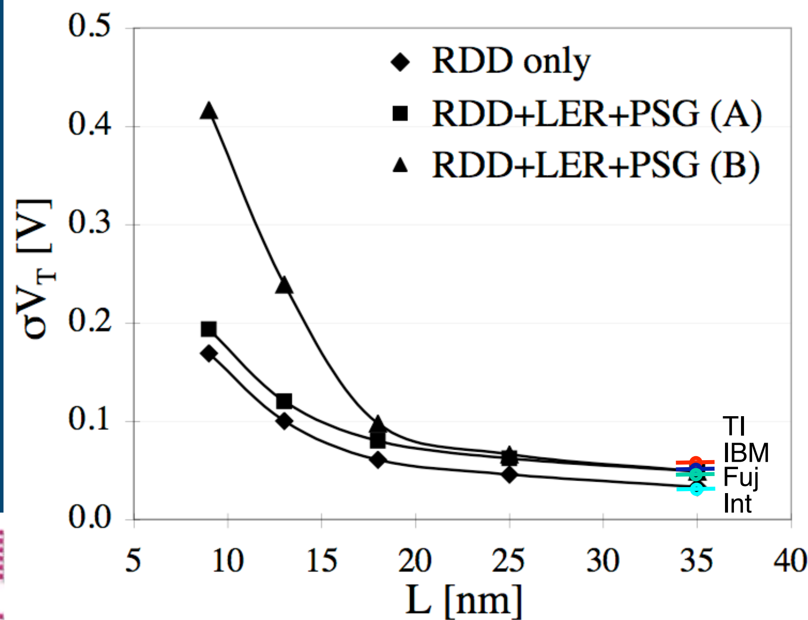
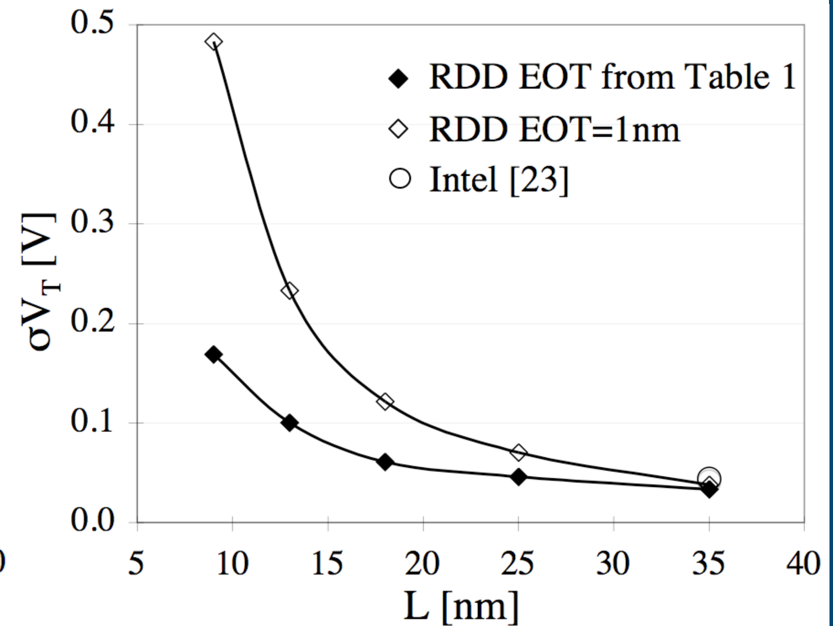
Potential distributions

Combined variability in bulk MOSFETs





t_{ox} scales according to ITRS



t_{ox} remains constant

Transport (scattering) related variability

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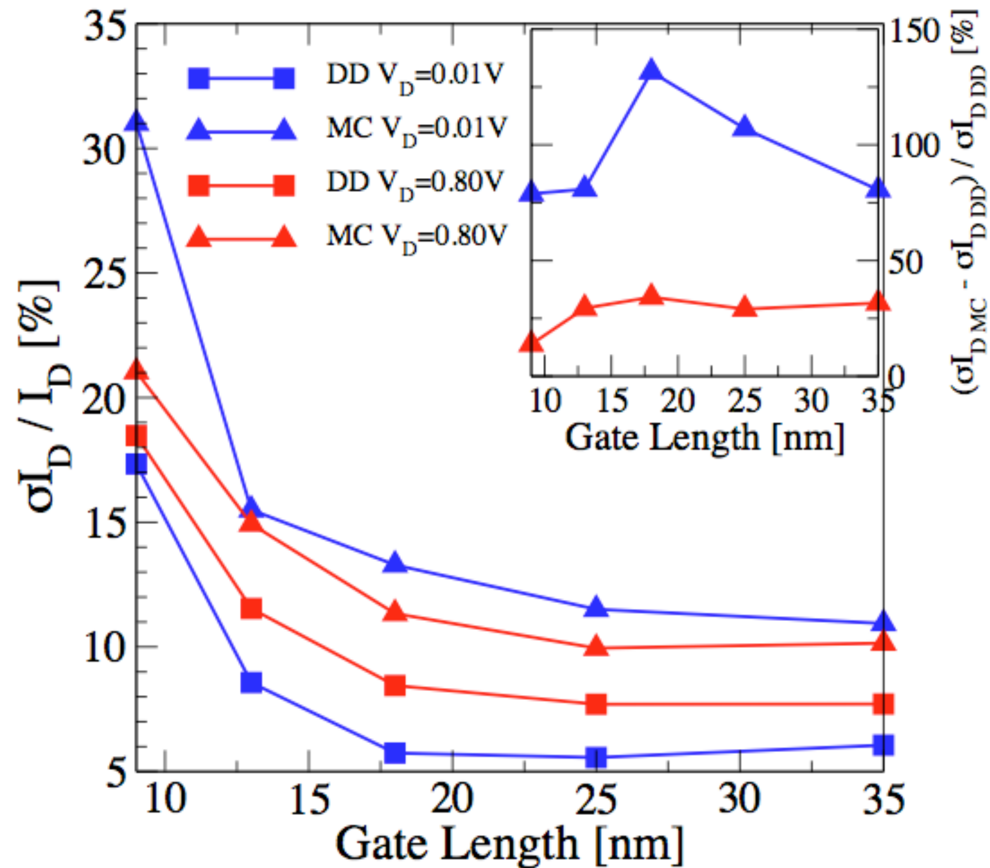

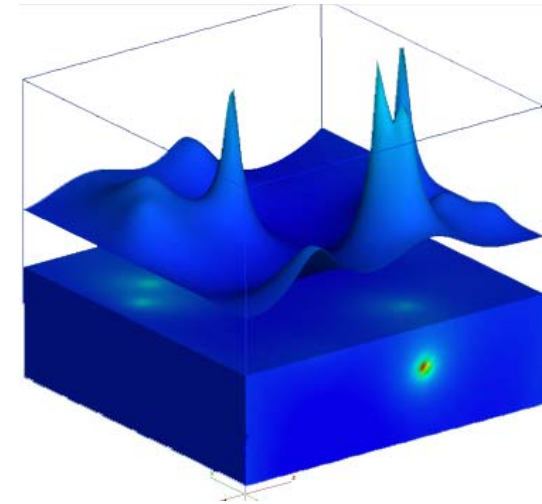

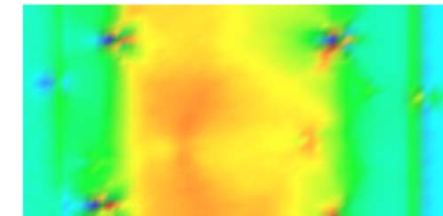

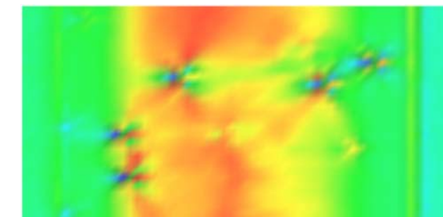

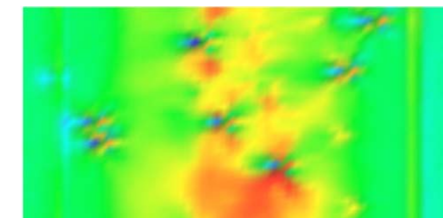

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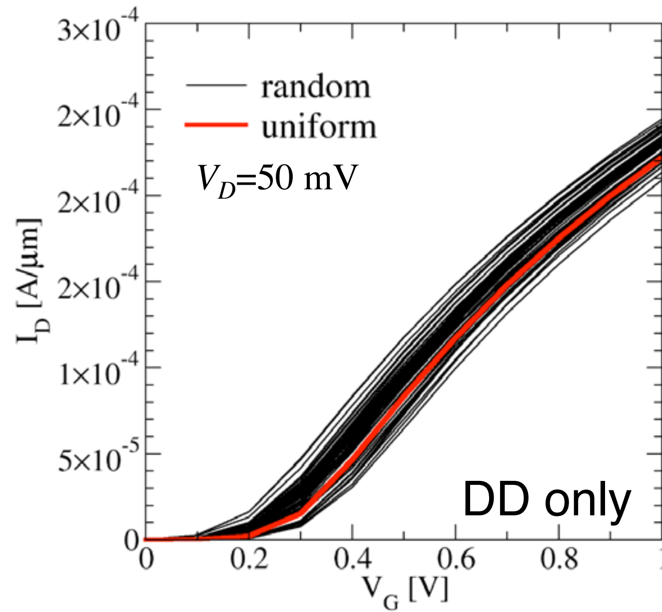
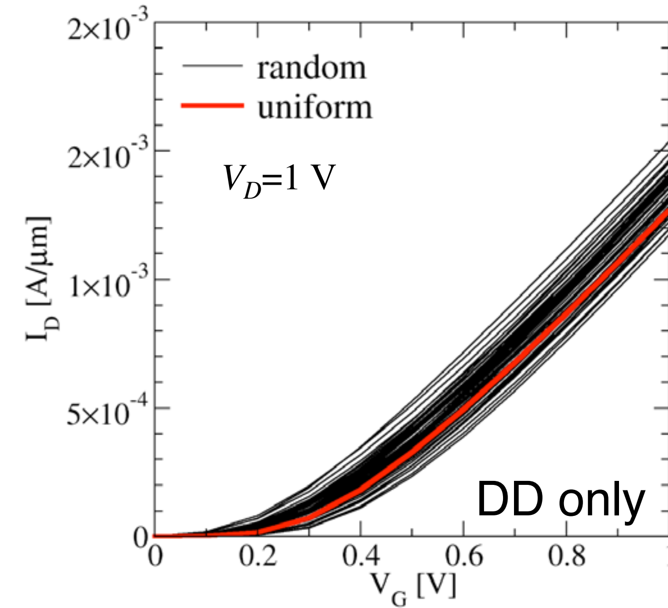
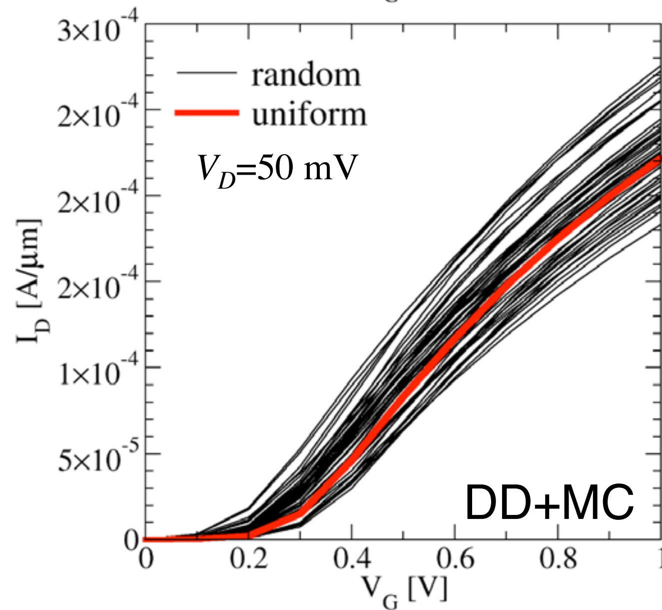
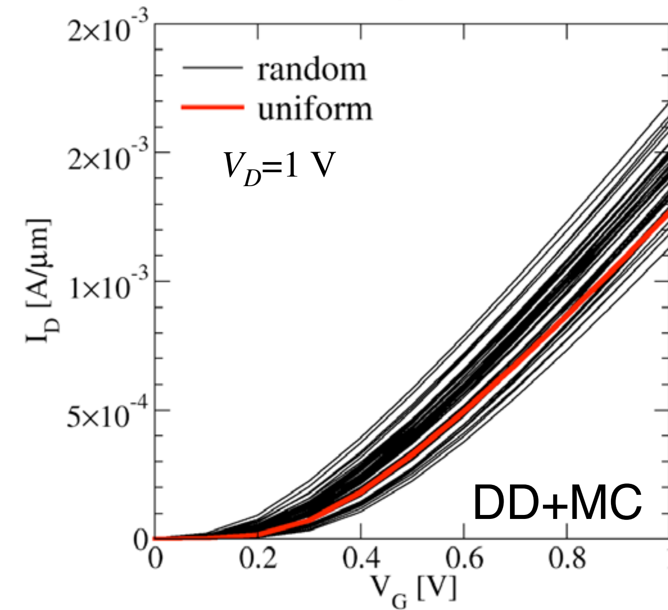
The impact of the transport related variability







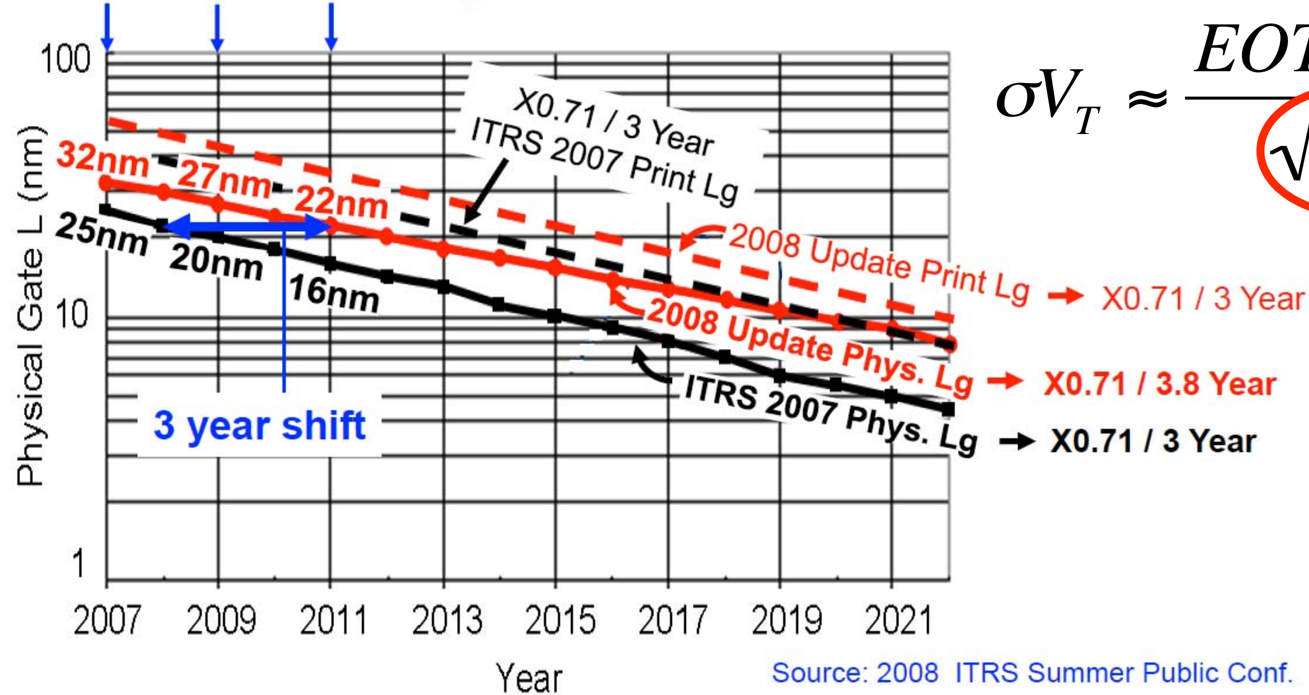


35 nm MOSFET

Bulk MOSFETs are here to stay longer: But they will be longer too

Physical gate length in past ITRS was too aggressive.
The dissociation from commercial product prediction will be adjusted.

Physical gate length of High-Performance logic will shift by 3-5 yrs.



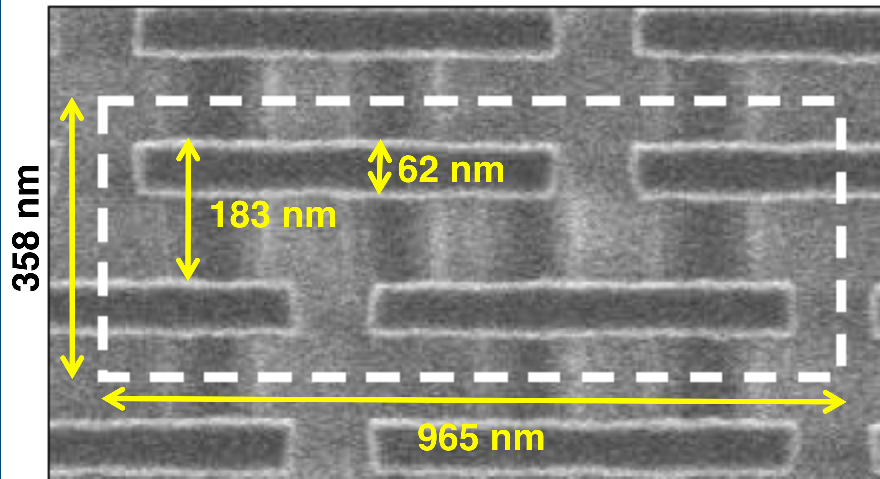
$$\sigma V_T \approx \frac{EOT \times N_D^{0.4}}{\sqrt{LW}}$$

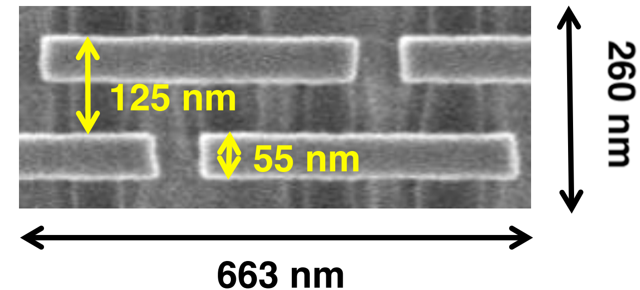
H. Ivai

SRAM on a relaxed scaling path

Intel on 45 nm node:
Logic gate pitch is 160 nm
Logic gate length is 35 nm
SRAM cell area is 0.346 μm²

Intel on 32 nm node:
Logic gate pitch is 112.5 nm
Logic gate length is 30 nm
SRAM cell area is 0.172 μm²



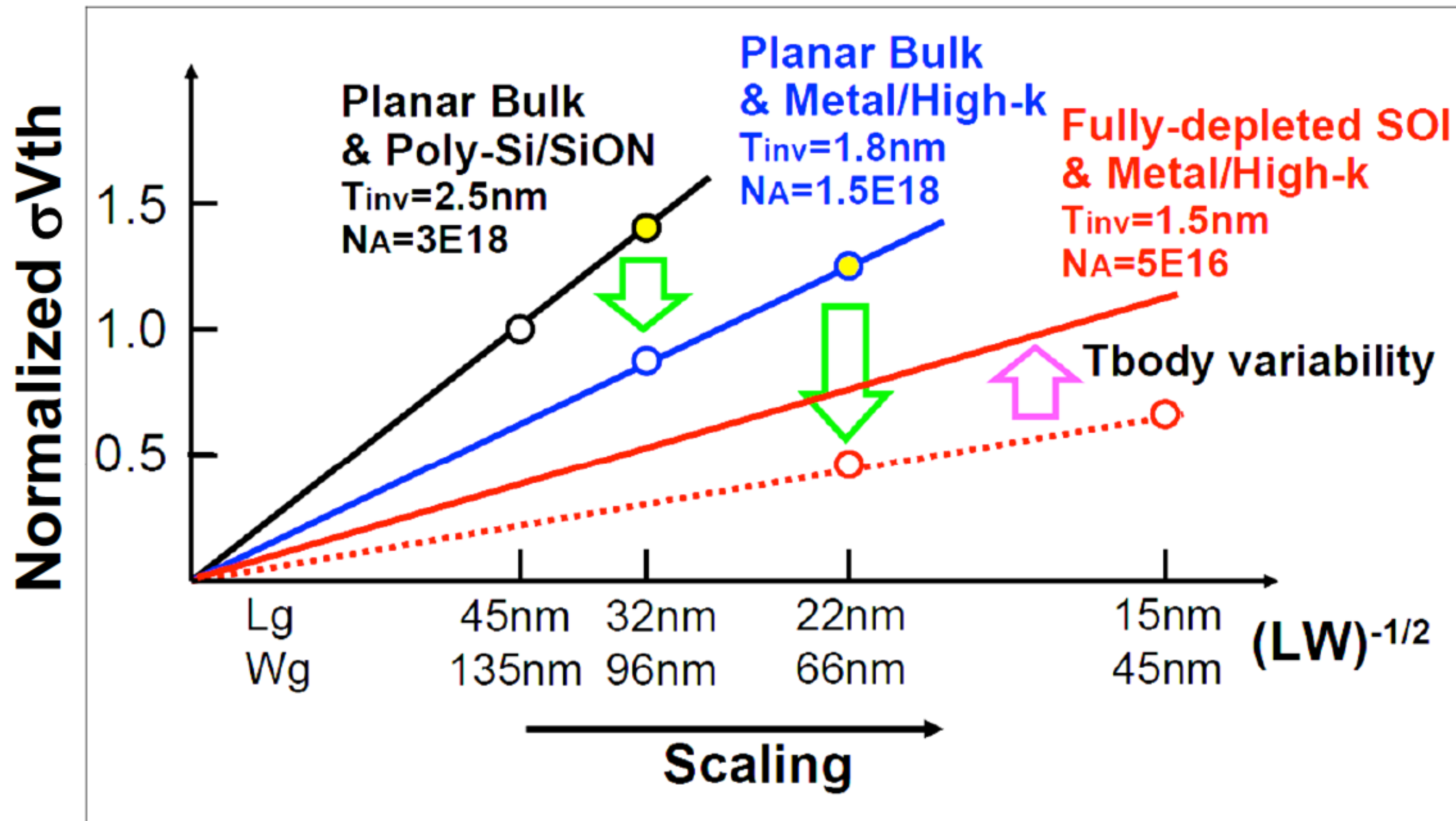


Same scale

Gate length @SRAM is almost twice as big as in logic

There's almost no SRAM channel length scaling from 45nm to 32nm

ITRS variability reduction scenarios in

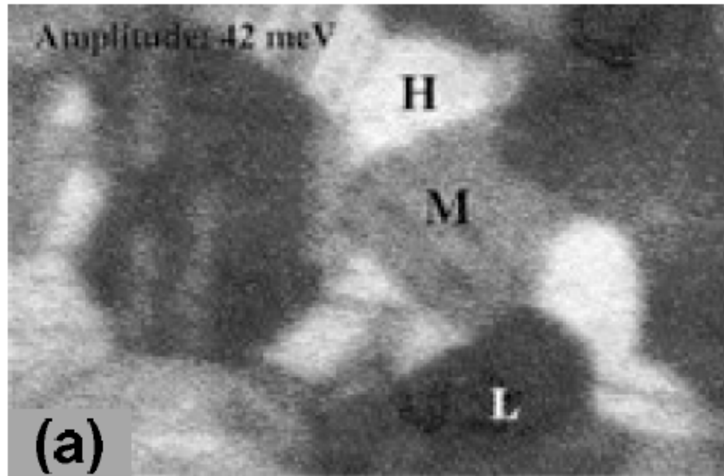


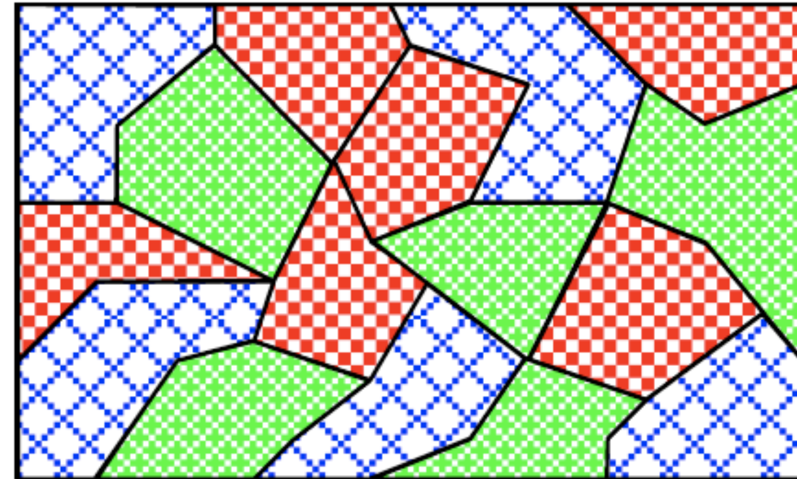
$$\sigma V_T \approx \frac{EOT \times N_D^{0.4}}{\sqrt{LW}}$$

H. Ivai

Metal gate granularity (MGG)

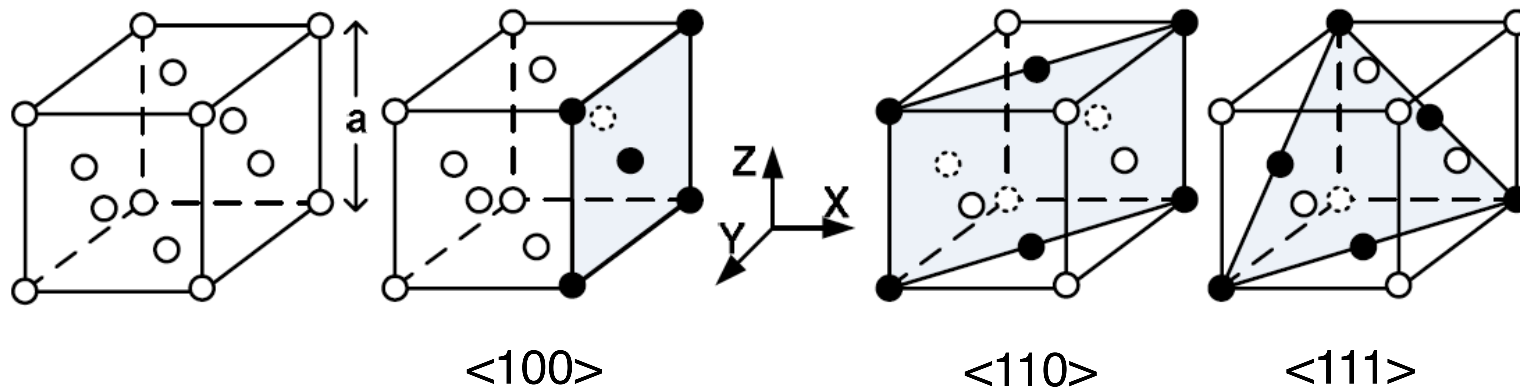
Cooper





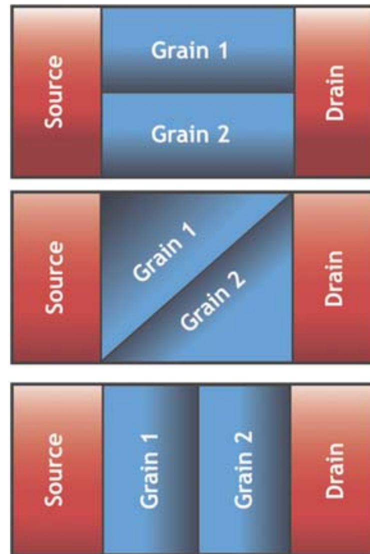
Φ_{111}(L)>Φ_{100}(M)>Φ_{110}(H)

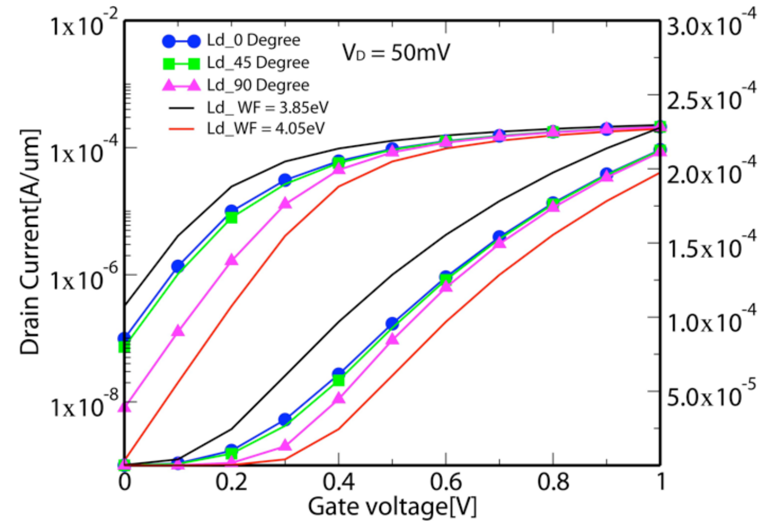
Different surface density at different orientations

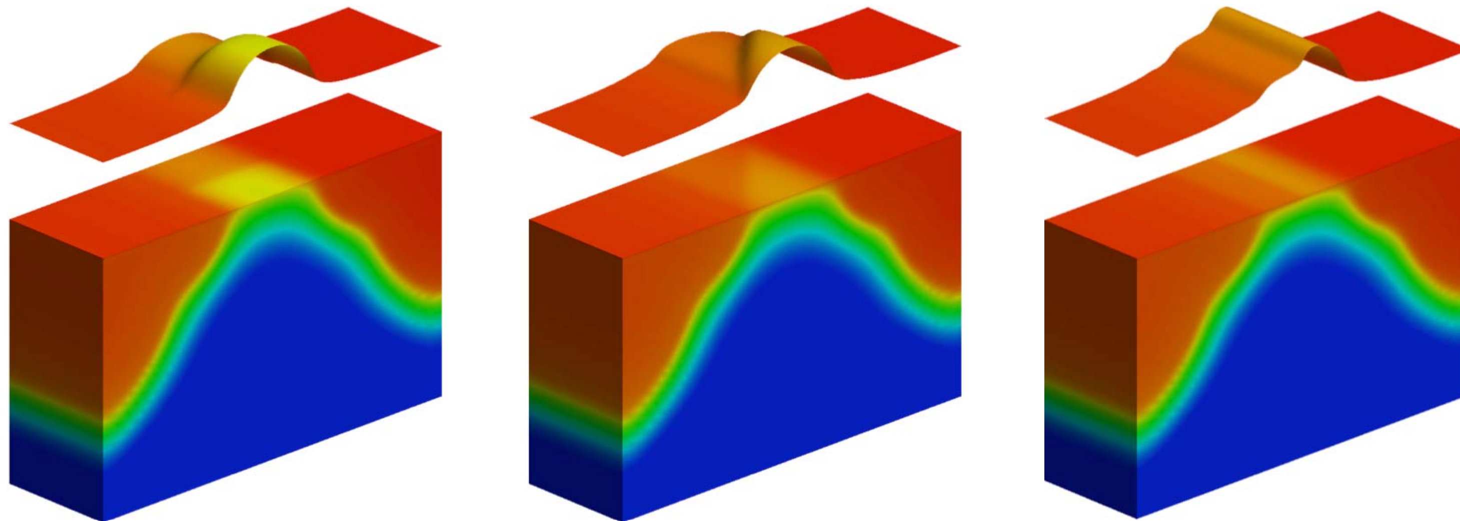


H. Dadgour et al.

Metal gate granularity (MGG)

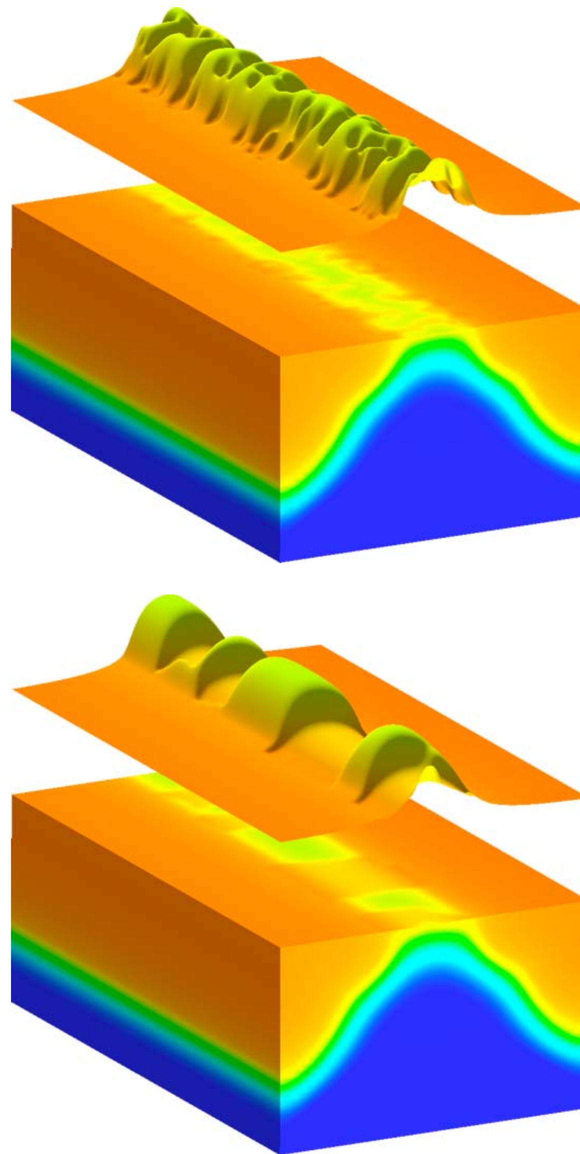


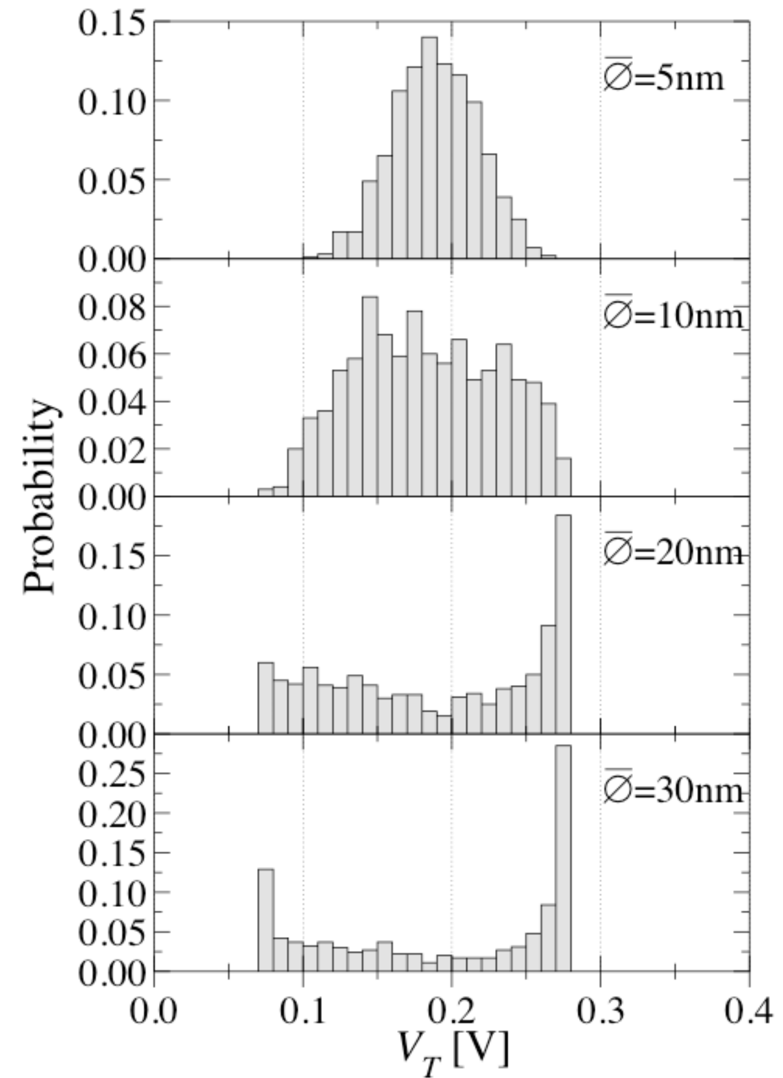




N. M. Idris et al.

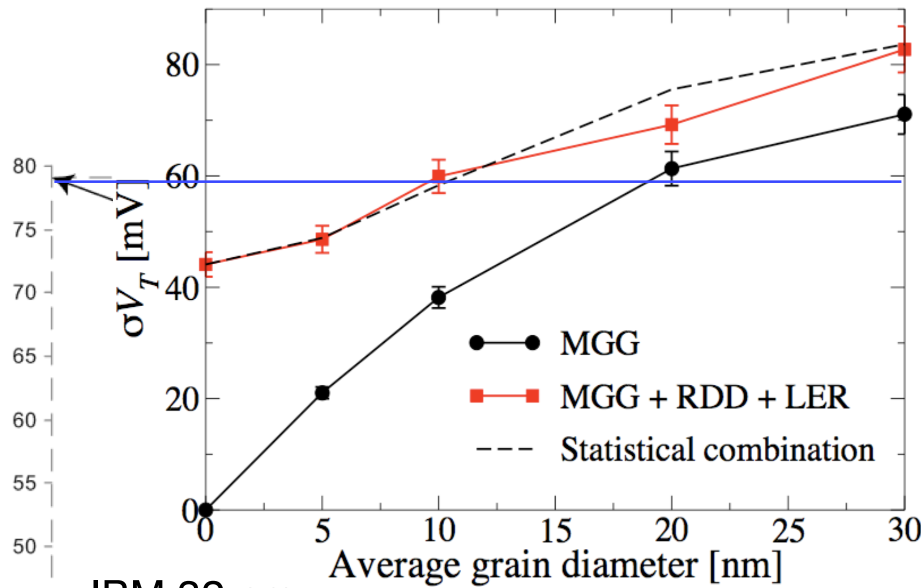
Metal gate granularity (MGG)



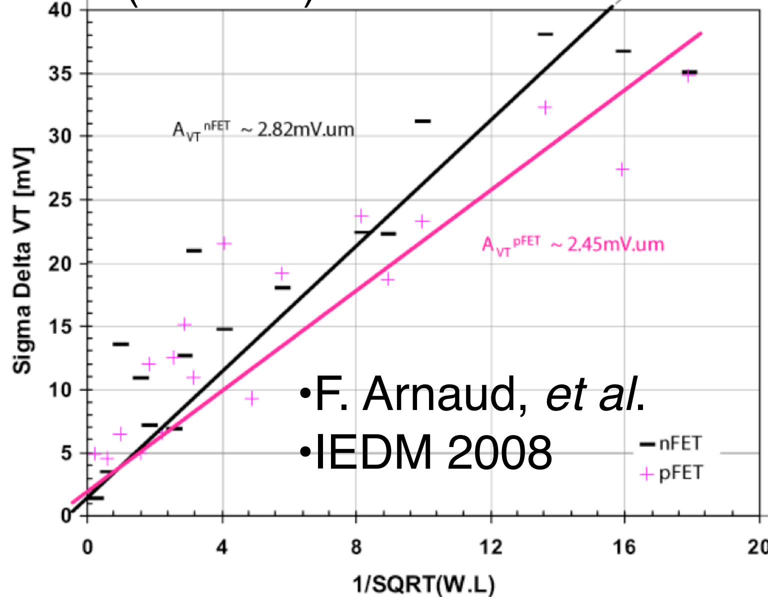


Brown et al.

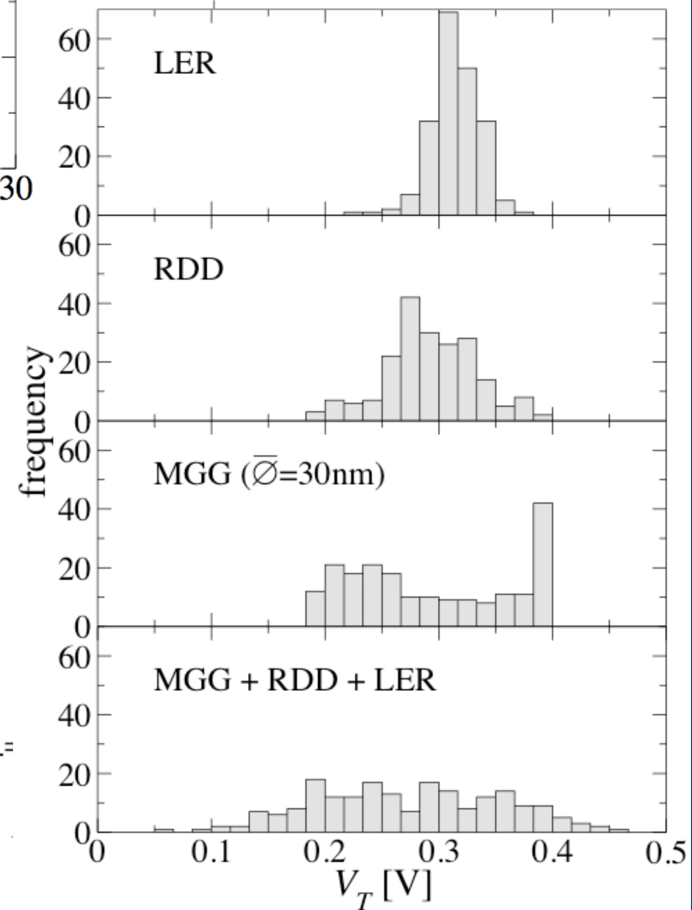
32 nm high-k/metal gate MOSFET



IBM 32 nm
(IEDM'09)

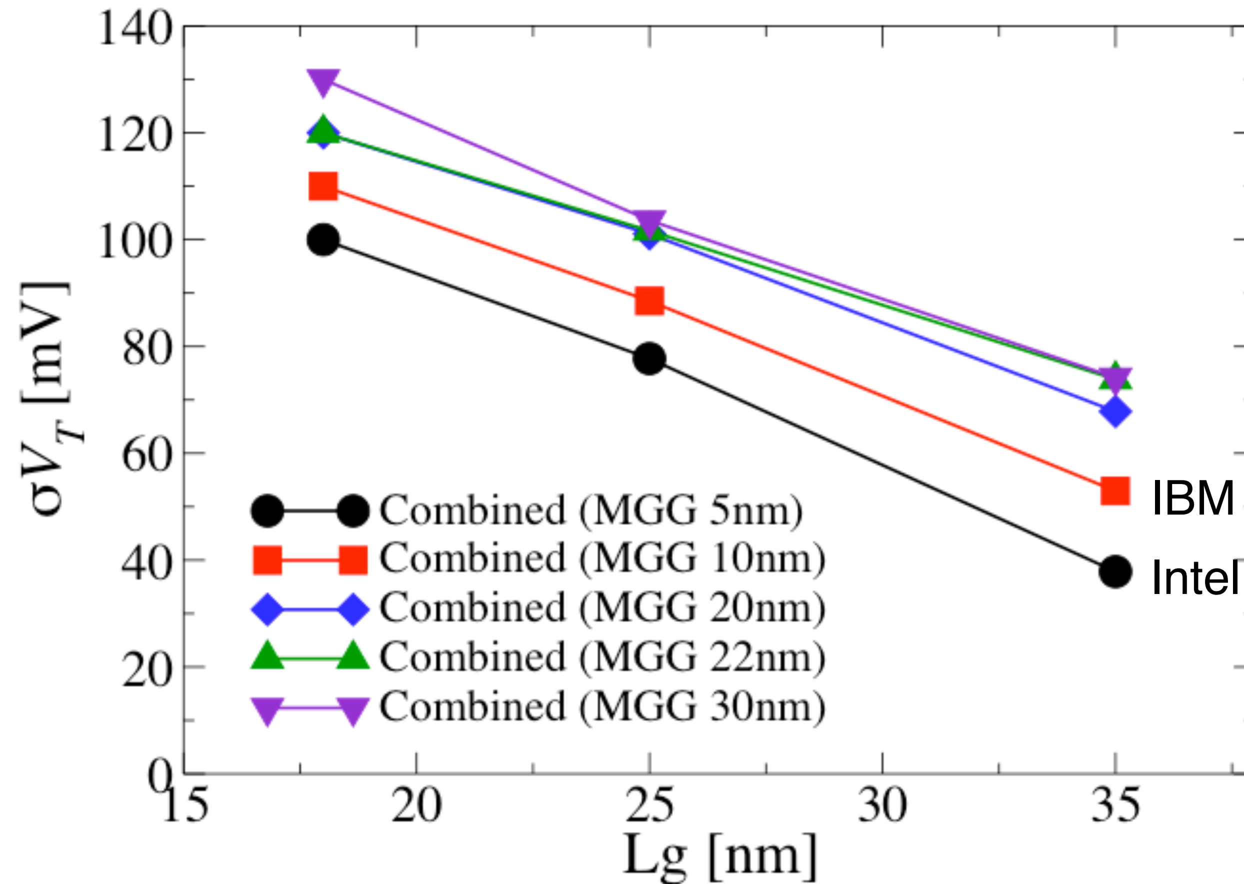


- F. Arnaud, *et al.*
- IEDM 2008



REALITY

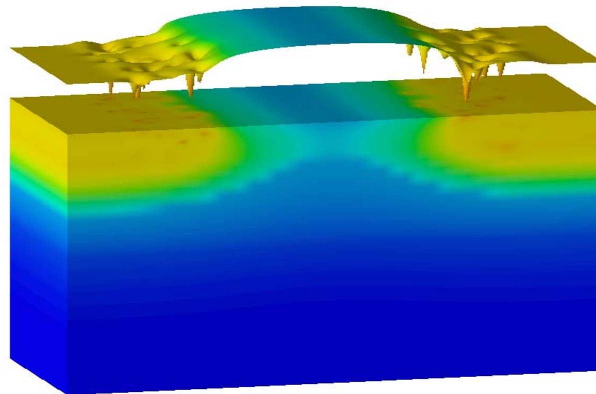
Variability in high-k/metal gate MOSFETs



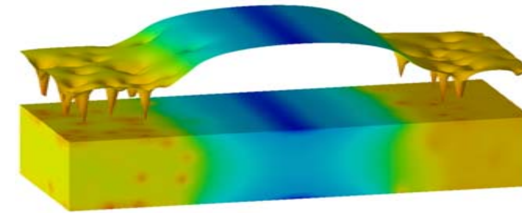
Combined with different MGG size

SOI and DG variability

32 nm FD SOI



22 nm DG



	32nm σV_T (mV)		22nm σV_T (mV)	
	V_{ds} (50mV)	V_{ds} (1.0V)	V_{ds} (50mV)	V_{ds} (1.0V)
RDD	5.3	6.1	6.4	8.1
LER	3.3	8.6	5.8	13
Trap (1e11)	11	11	5.1	4.8
Combined (1e11)	13	15	10	16

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Summary

- Background
- Statistical variability
- Statistical reliability
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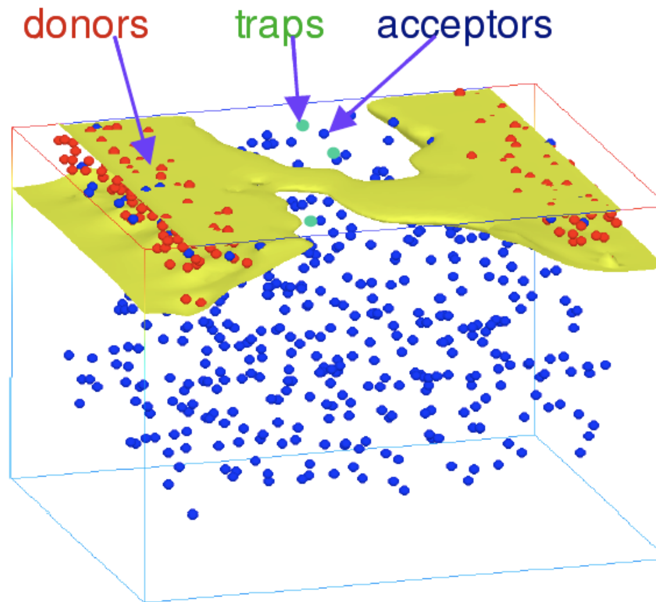
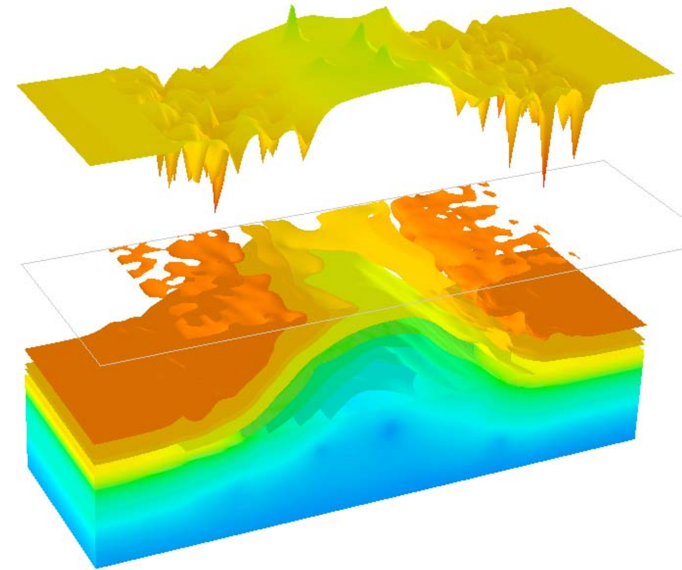
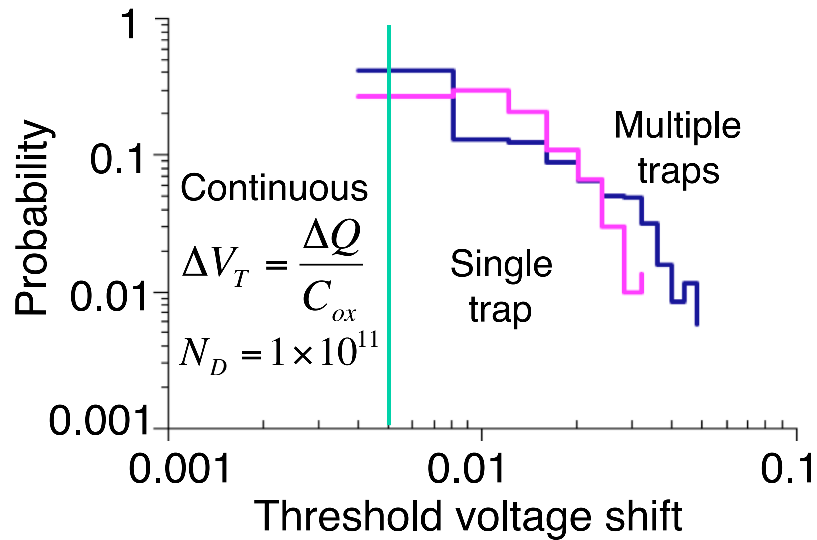
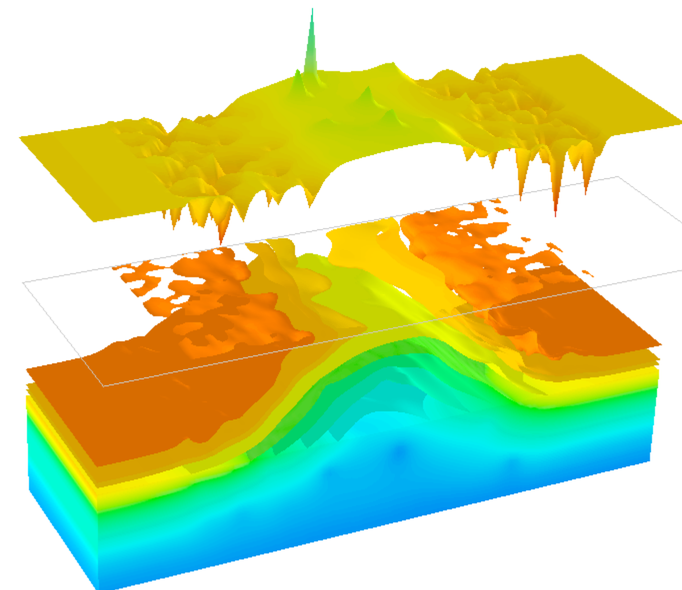
- Conclusions

Statistical reliability: electrostatics

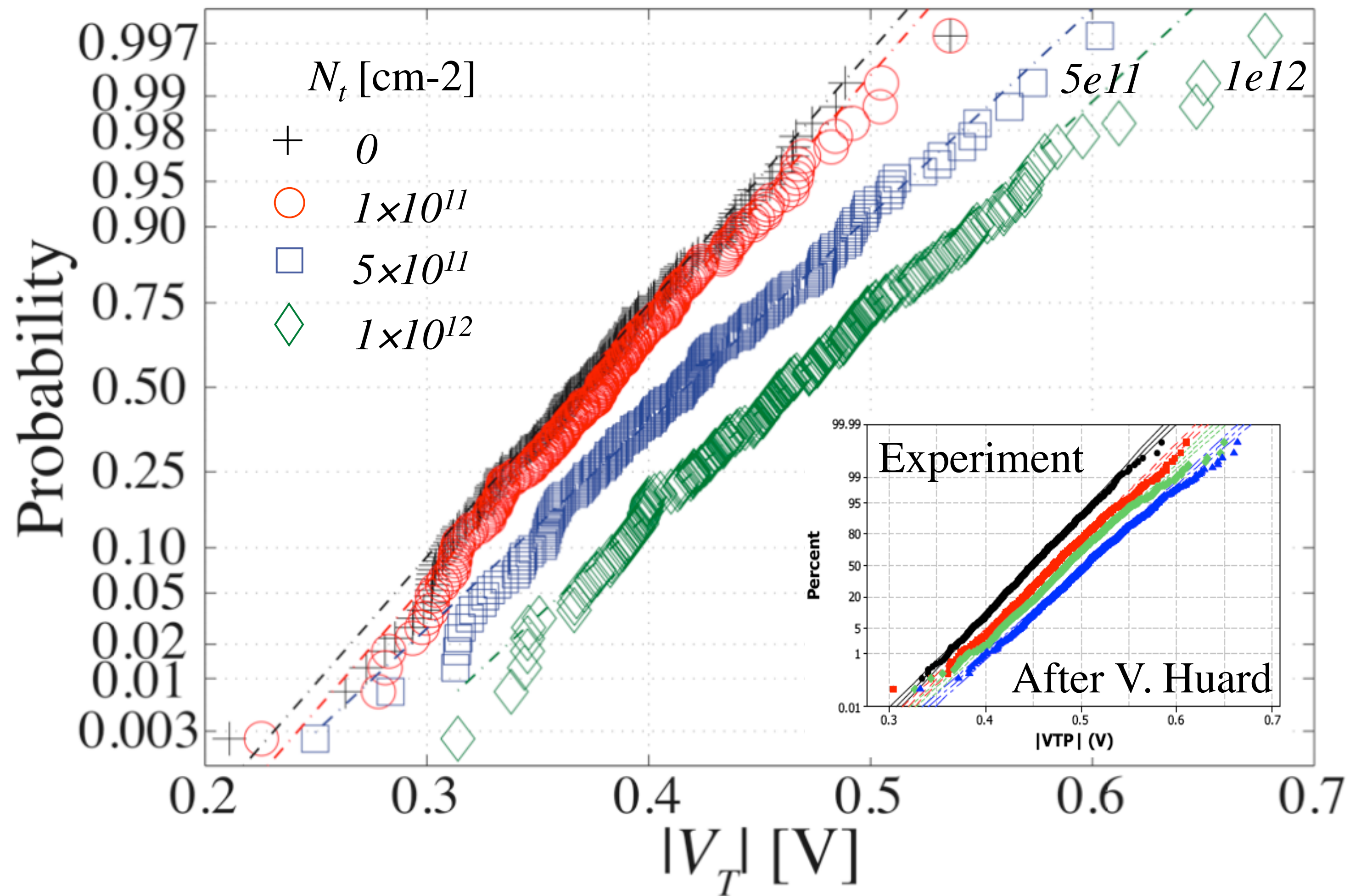








Threshold voltage variability increases with NBTI



Trapping produces ‘anomalously’ large Threshold voltage shifts

Probability

0.997
0.99
0.98
0.95
0.90
0.75
0.50
0.25
0.10
0.05
0.02
0.01
0.003

1×10^{11} 5×10^{11} 1×10^{12}

0 0.05 0.1 0.15 0.2

$|\Delta V_T|$ [V]

Experiment

Percent

99.99 99 95 80 50 20 5 1 0.01

-0.05 0.00 0.05 0.10 0.15

VTP shift (V)

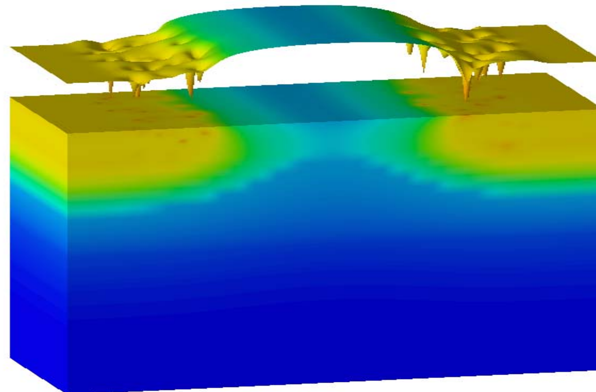
After V. Huard

The reason for 'anomalously' large threshold voltage shifts

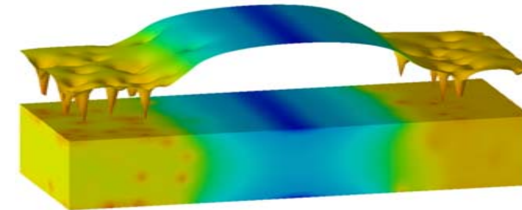
University of Glasgow

SOI and DG variability

32 nm FD SOI



22 nm DG



	32nm σV_T (mV)		22nm σV_T (mV)	
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RDD	5.3	6.1	6.4	8.1
LER	3.3	8.6	5.8	13
Trap (1e11)	11	11	5.1	4.8
Trap (5e11)	24	25	13	12
Trap (1e12)	36	37	18	17
Combined (1e11)	13	15	10	16
Combined (5e11)	25	27	16	19
Combined (1e12)	37	38	20	23

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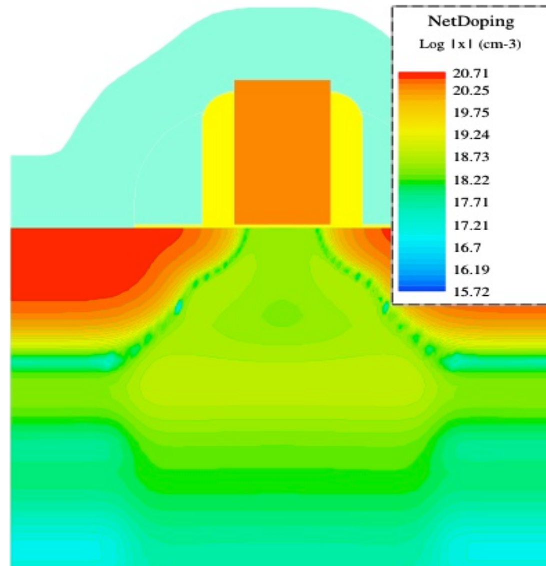
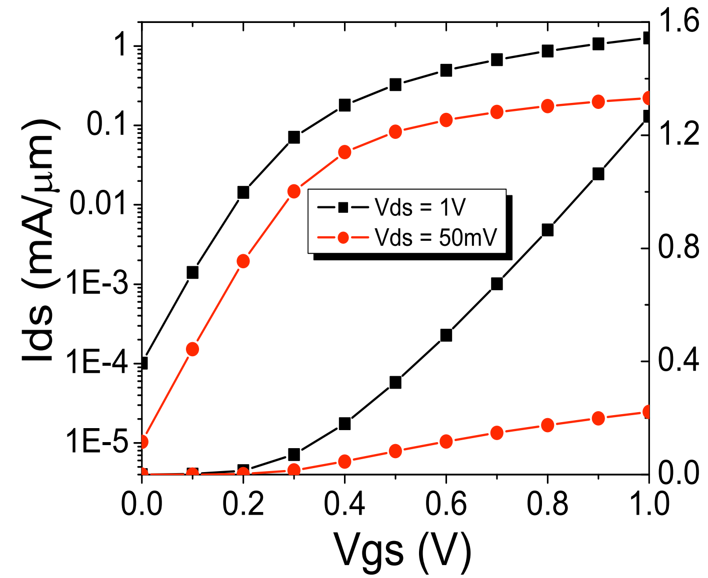
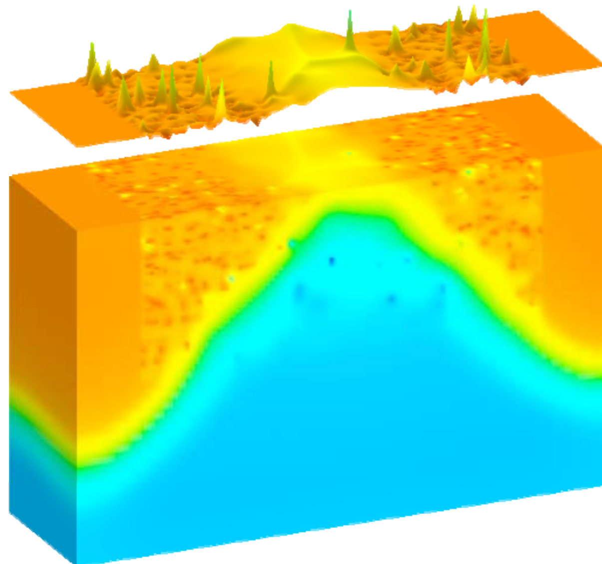
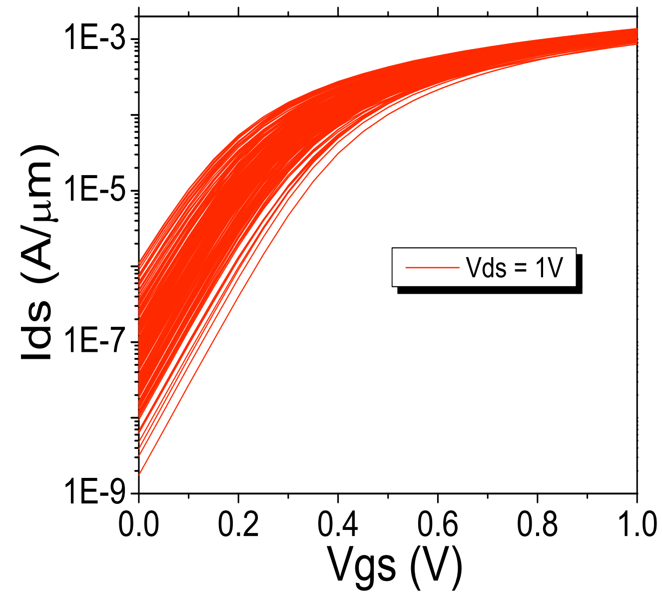
Test bed 35 nm MOSFET

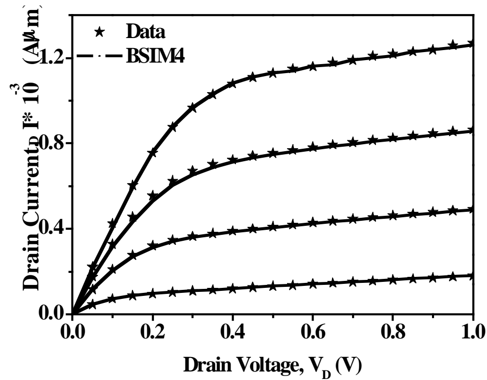


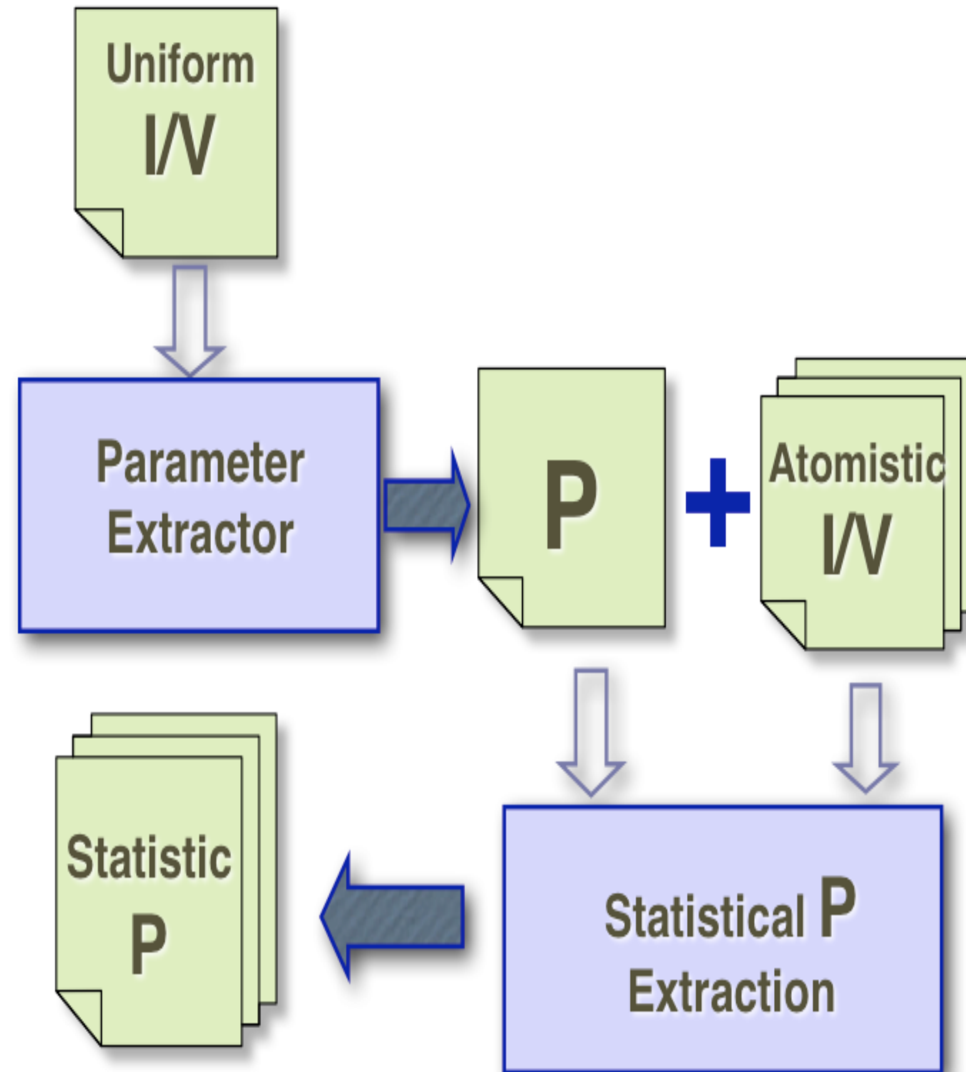


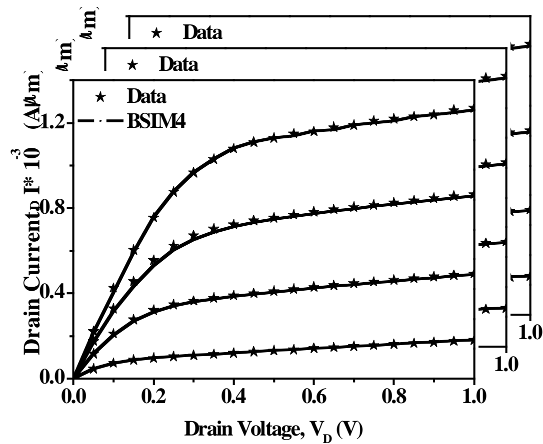




Two stage parameter extraction

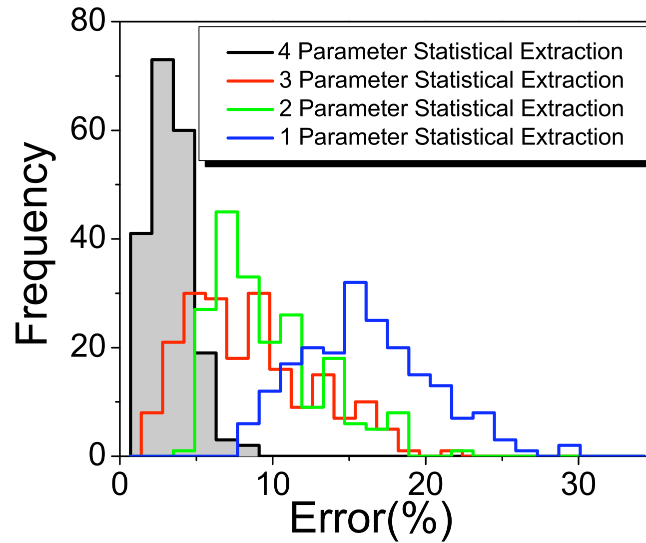


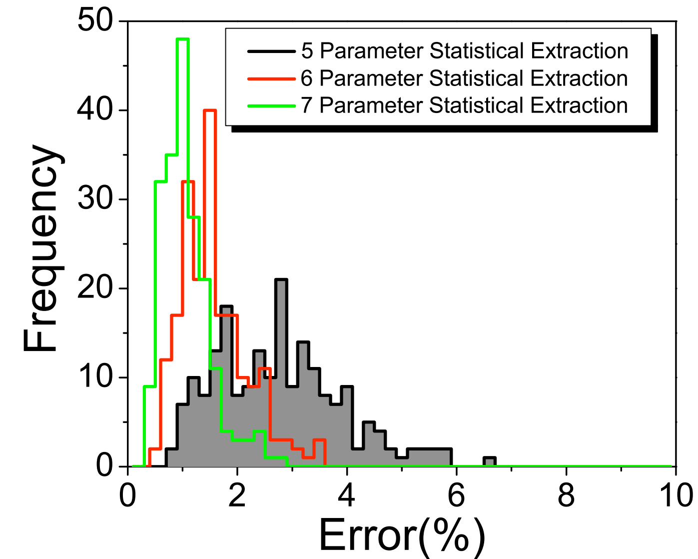




200 microscopically different transistors

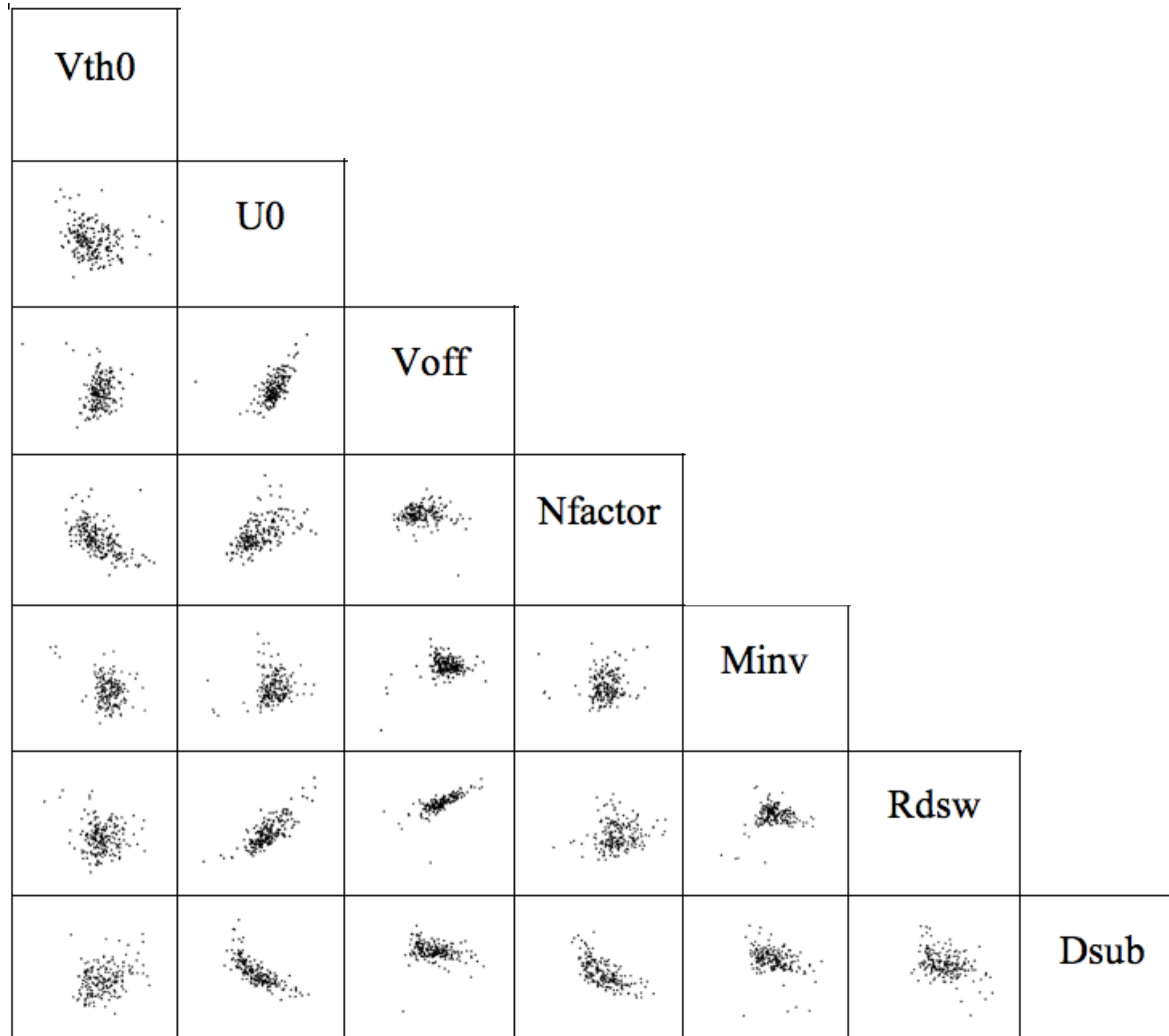
BSIM parameter selection



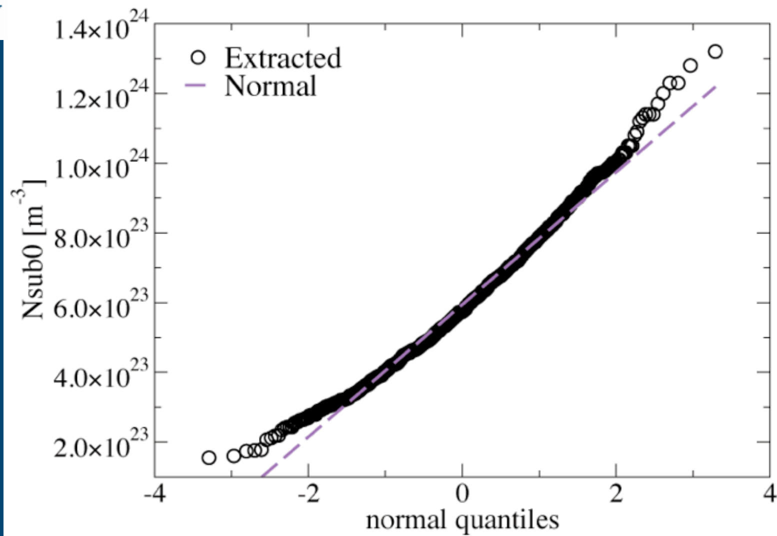


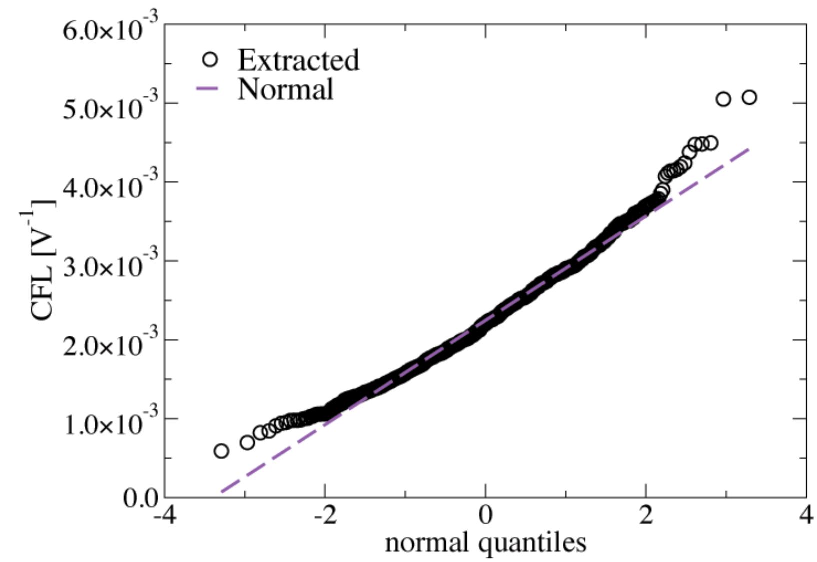
Number of parameters	Average RMS fitting error(%)		Maximum RMS fitting error(%)		Standard Deviation	
	BSIM	PSP	BSIM	PSP	BSIM	PSP
1	16.8	16.5	30.1	27.8	4.3	4.23
2	10.5	11.8	22.5	24.6	3.5	3.93
3	8.5	9.1	21.5	21.9	4.1	2.96
4	3.99	5.44	9.75	13.9	1.4	2.22
5	2.85	2.59	6.75	8.2	1.15	1.25
6	1.56	1.58	3.6	5.2	0.6	0.63
7	1.16	1.32	2.8	3.6	0.45	0.59

Statistical compact model parameter correlations

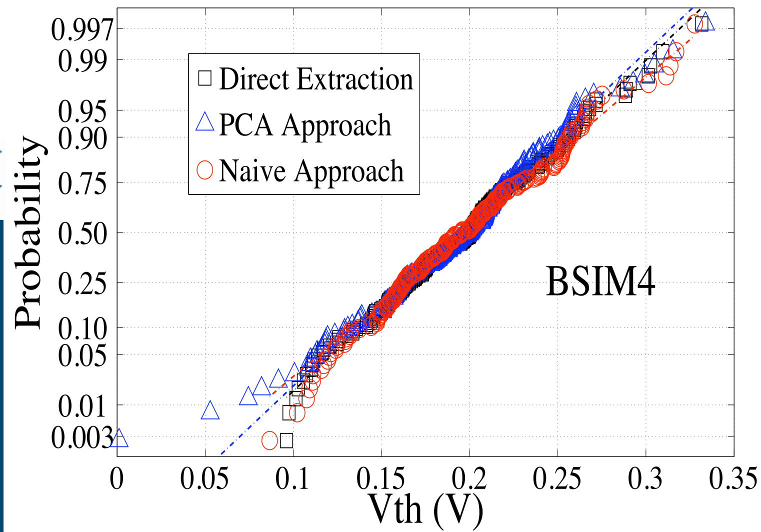


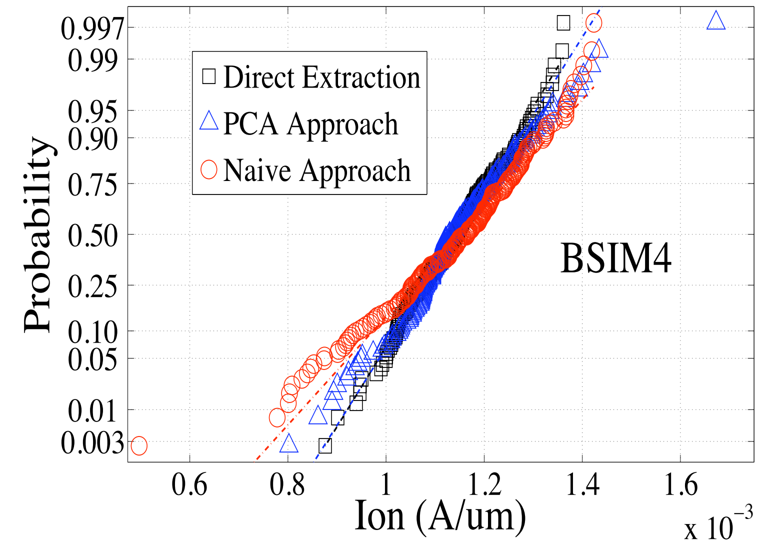
Deviation from Normal distribution

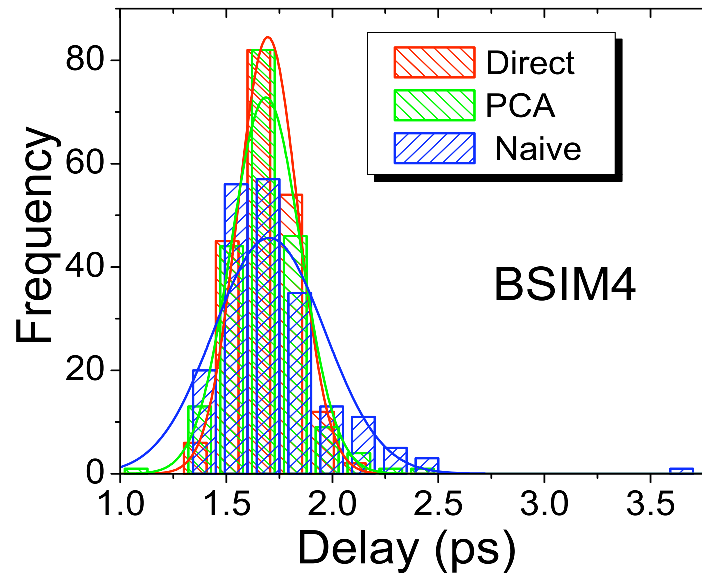




Naïve approach vs. PCA

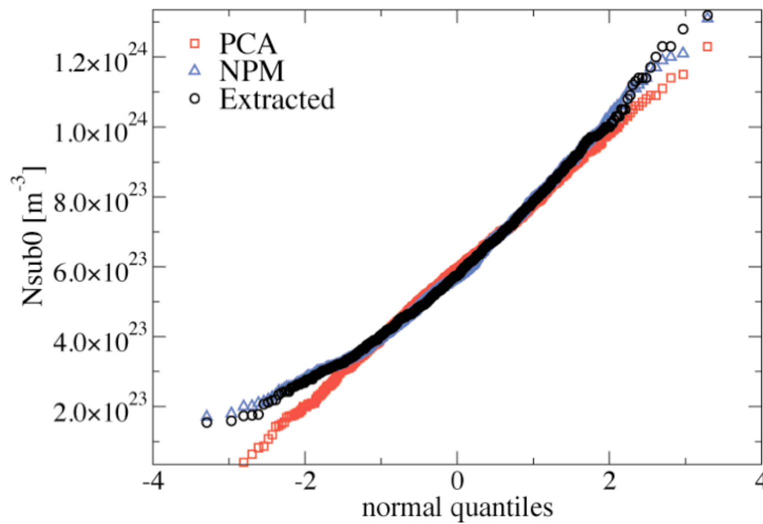


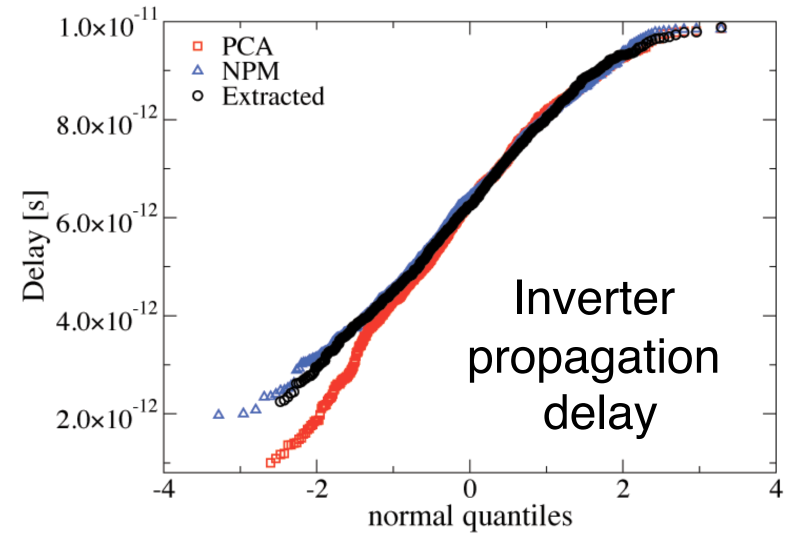


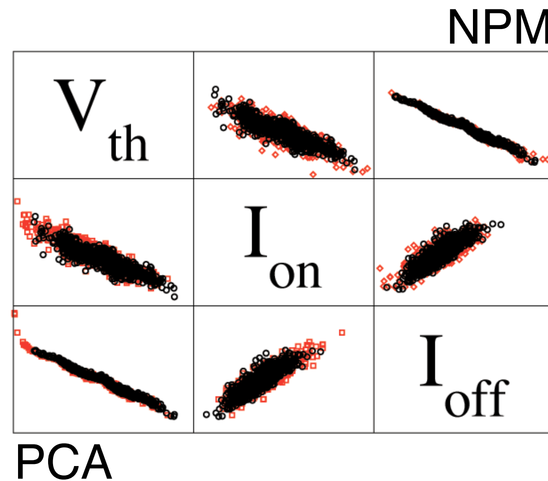


STDV error
PCI - 15%
Naïve - 85%

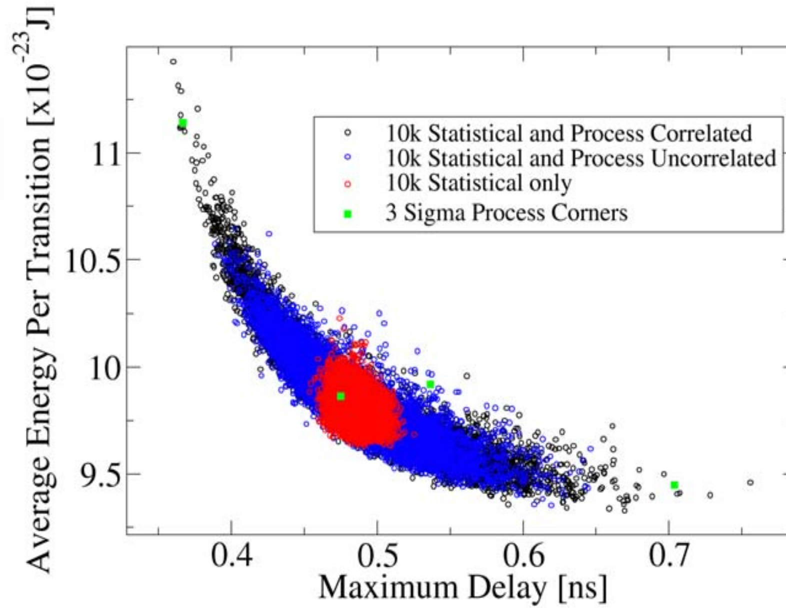
Statistical Nonlinear Power Method (NPM)

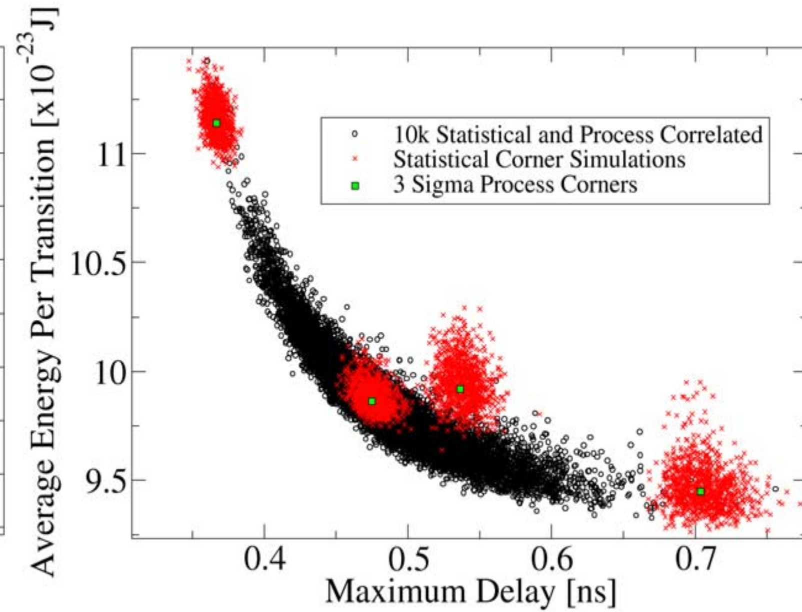


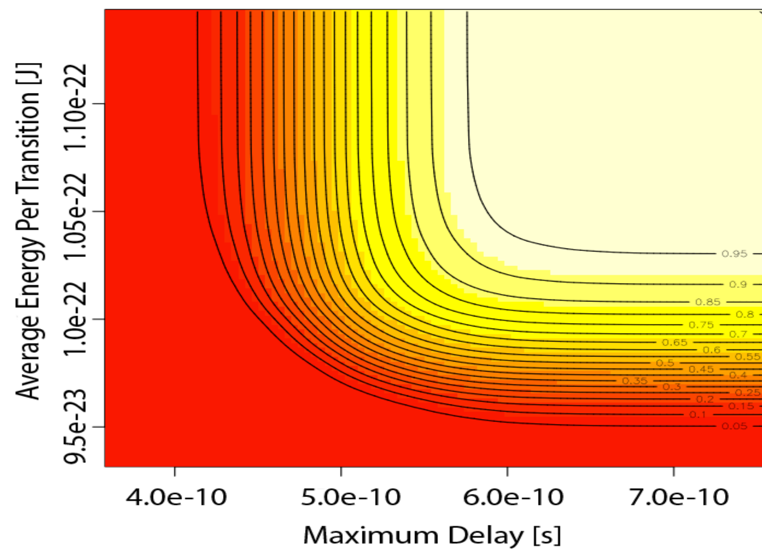


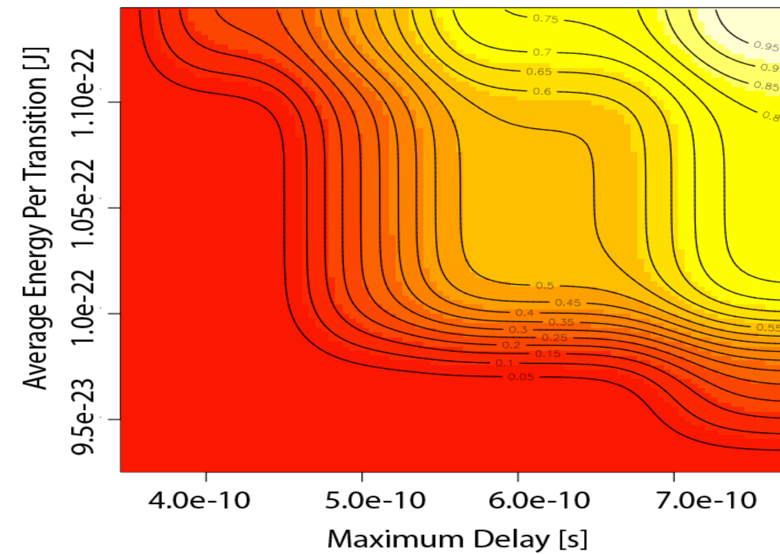


Statistical vs. Global Corners









Performance/power/yield trade off

Average Energy Per Transition [J]

Maximum Delay [s]

90% Yield

99% Yield

Correlated process variability +
3 different level of statistical variability

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Conclusions

- Statistical variability has to be taken very seriously at 32 nm technology generation.
- Statistical reliability, enhanced by statistical variability is becoming an important issue.
- Statistical compact model techniques are necessary to support statistical design.
- Best practices for statistical compact modeling need to be established.

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