Test Structures for Variability Characterization

Kevin Nowka
IBM Research – Austin
nowka@us.ibm.com

IBM Research Worldwide

Executive Summary

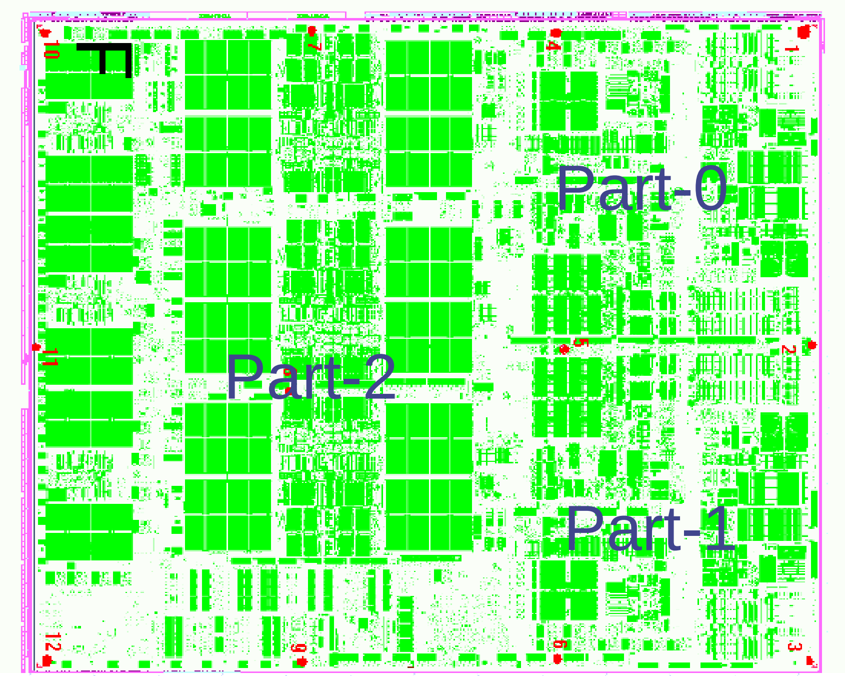
- Technology is getting more complex and harder to model/characterize.

- Meaningful modeling requires:
  - Sophisticated test structures to explore design implementation space (layout configurations).
  - High repetition counts to assess tolerances.
  - Efficient test to track technology learning.

- Net: numerous challenges.

An Example from IBM

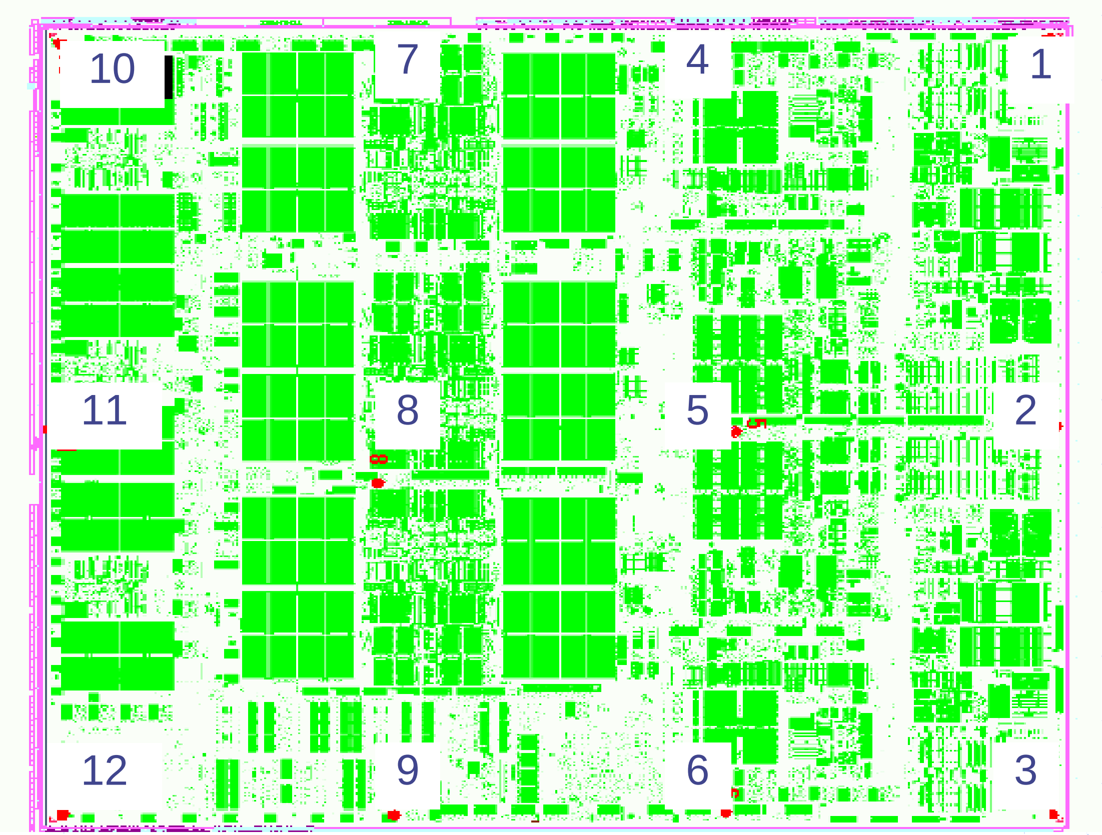
- One part of a 65nm design was found to be ~15% slower than other parts.
- Models predict all parts of design are identical.
- Model/hardware mismatch!
  - Slower block limits F_{MAX}.
  - Faster block wastes power.



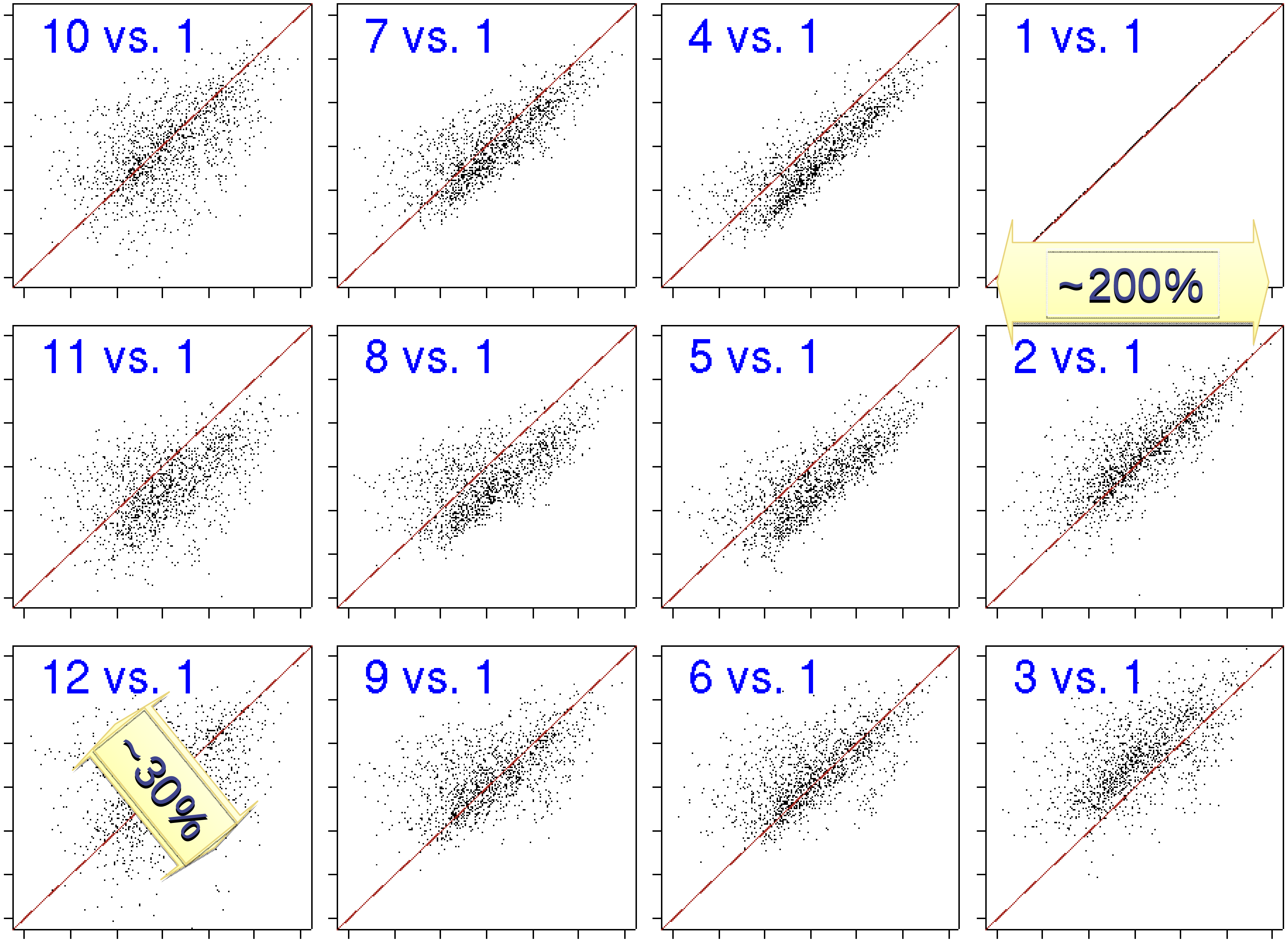
Case study performed by
Anne E. Gattiker

Model to Hardware Support

- Chip has 12 ring oscillators distributed across the die, and individually measurable.



Chip map with Ring Oscillator locations



10 vs. 1

7 vs. 1

4 vs. 1

1 vs. 1

11 vs. 1

8 vs. 1

5 vs. 1

2 vs. 1

12 vs. 1

9 vs. 1

6 vs. 1

3 vs. 1

~200%

~30%

Outcome and Observations

- Careful study of within-die and within-wafer patterns led to discovery of a systematic wafer processing problem (and its correction).

- Relying on models to find problems fails if models are not complete.
  - Obvious in retrospect!

Outline

- Model to Hardware Matching.

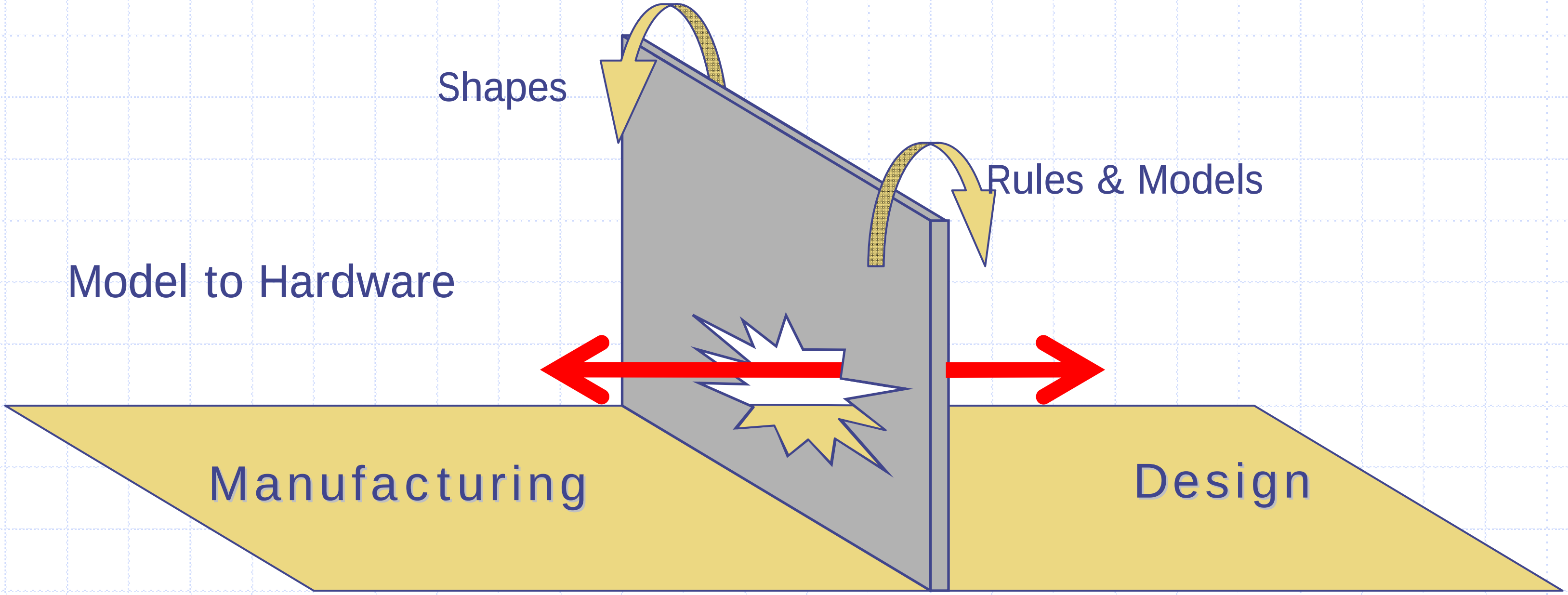
- General ideas about test structures.

- Structures for exploring random variability.
- Structures for exploring systematic variability.
- Structures for exploring spatial variability.

- Future trends and conclusions.

Model vs. Hardware for Semiconductors

- The semiconductor industry relies almost exclusively on "models" in order to predict performance.
- As features continue to shrink, the effectiveness of models becomes ever harder to maintain and check.
- There is a need for constant comparison and feedback between models and hardware!

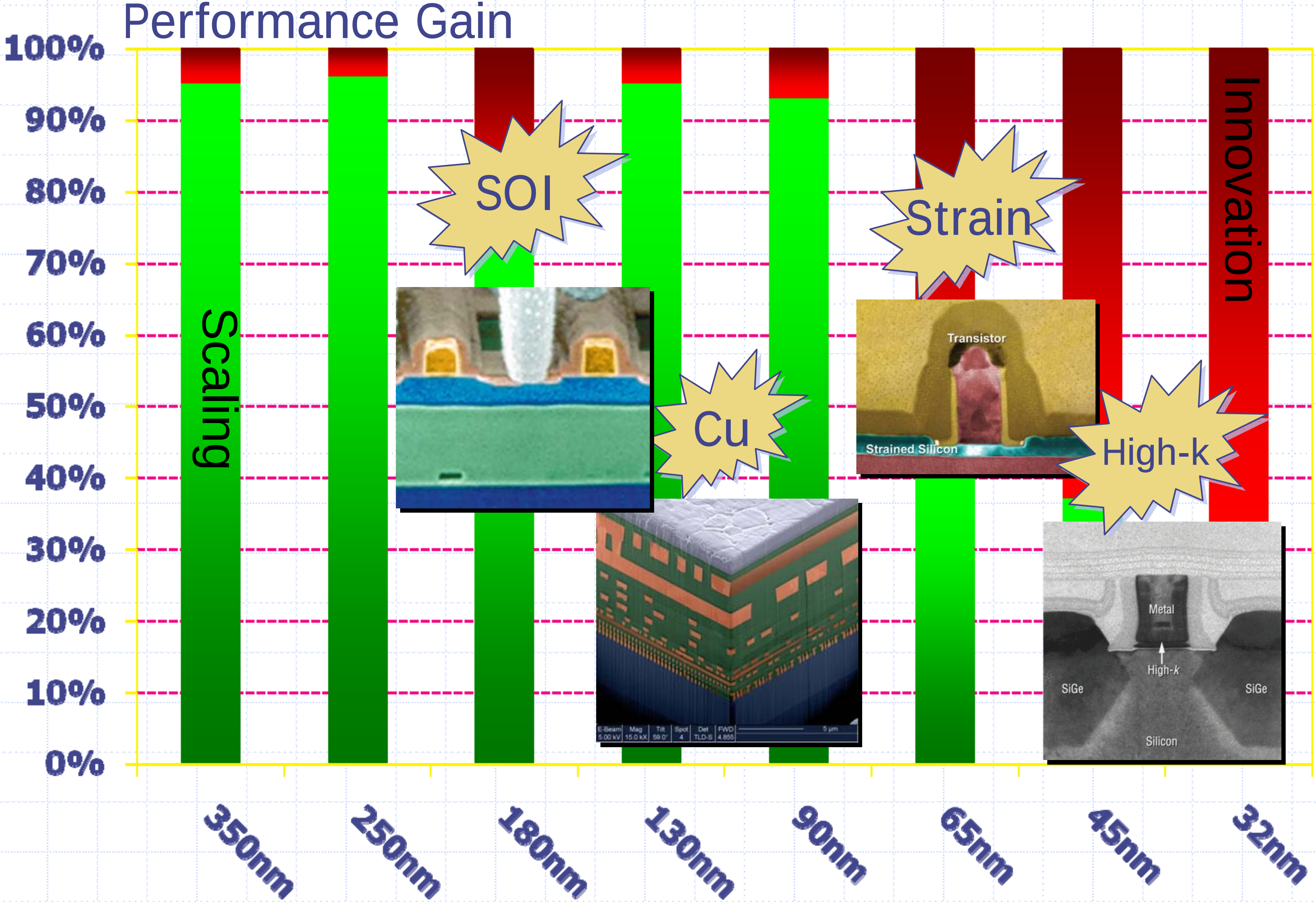


Why Added Complexity?

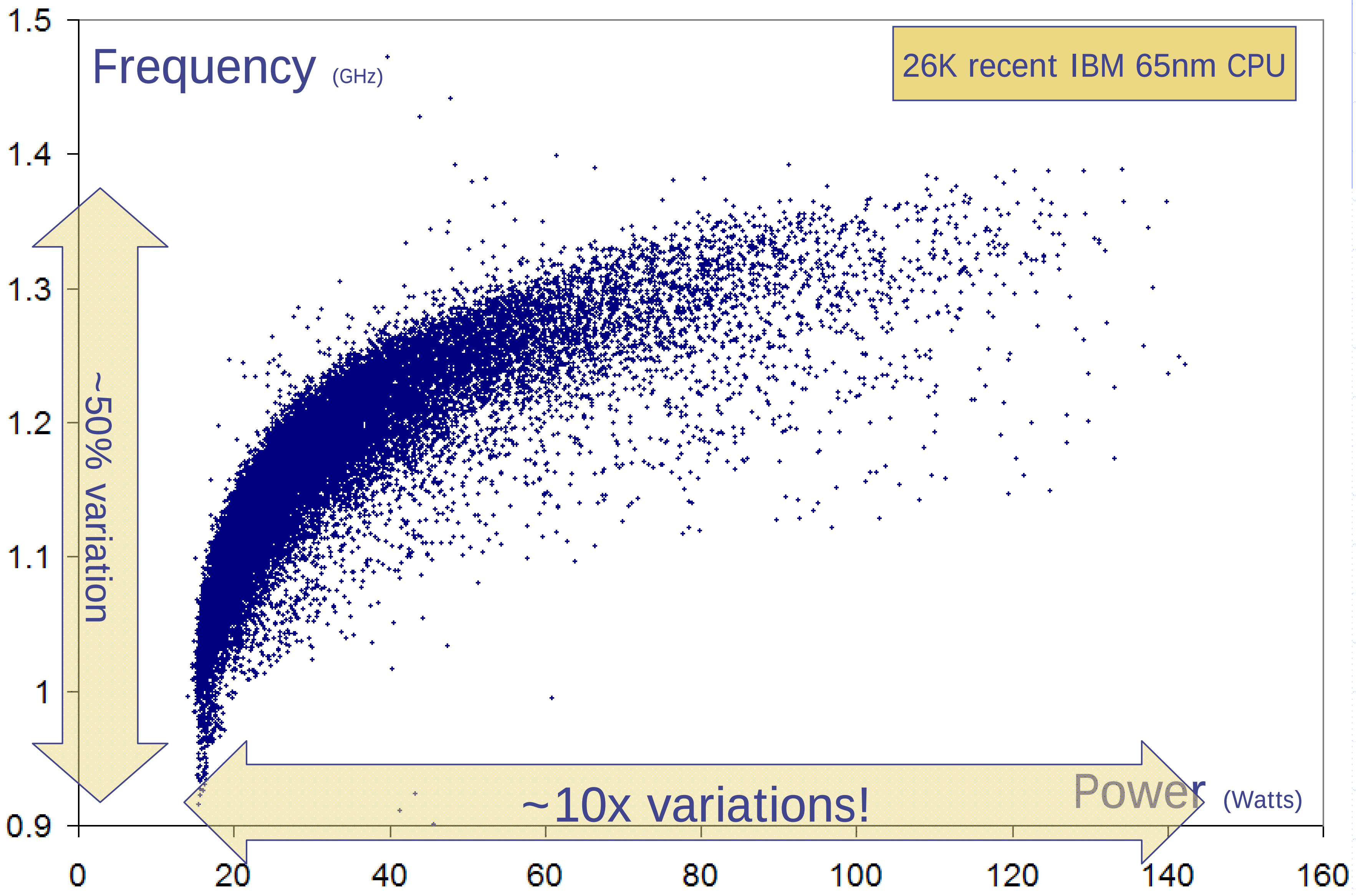
- Semiconductor manufacturing is getting harder as scaling fails to deliver performance.
  - Performance gain per technology generation is reducing.
- Gain coming from non-scaling innovations, Cu, SOI, Stress, Hi-K, etc...

- Technology R&D has become so expensive that few companies can afford to do it alone.
  - Hence the consolidation we see in our industry.

Scaling vs. Innovation



Result: Massive Variability



Variability vs. Knowledge

- Often, variability is simply “lack of knowledge”.
- This lack of knowledge can come about due to different factors:
    - I do not know where on the wafer this die will be.
    - I do not know how this wafer or lot will get processed.
    - I do not know what type of wiring will pass over this cell.
    - I do not know the exact load I am driving.
    - I do not know the exact value of V_{DD}.
    - I do not know how long this chip will need to operate.
    - ...
- Always, knowledge requires effort!

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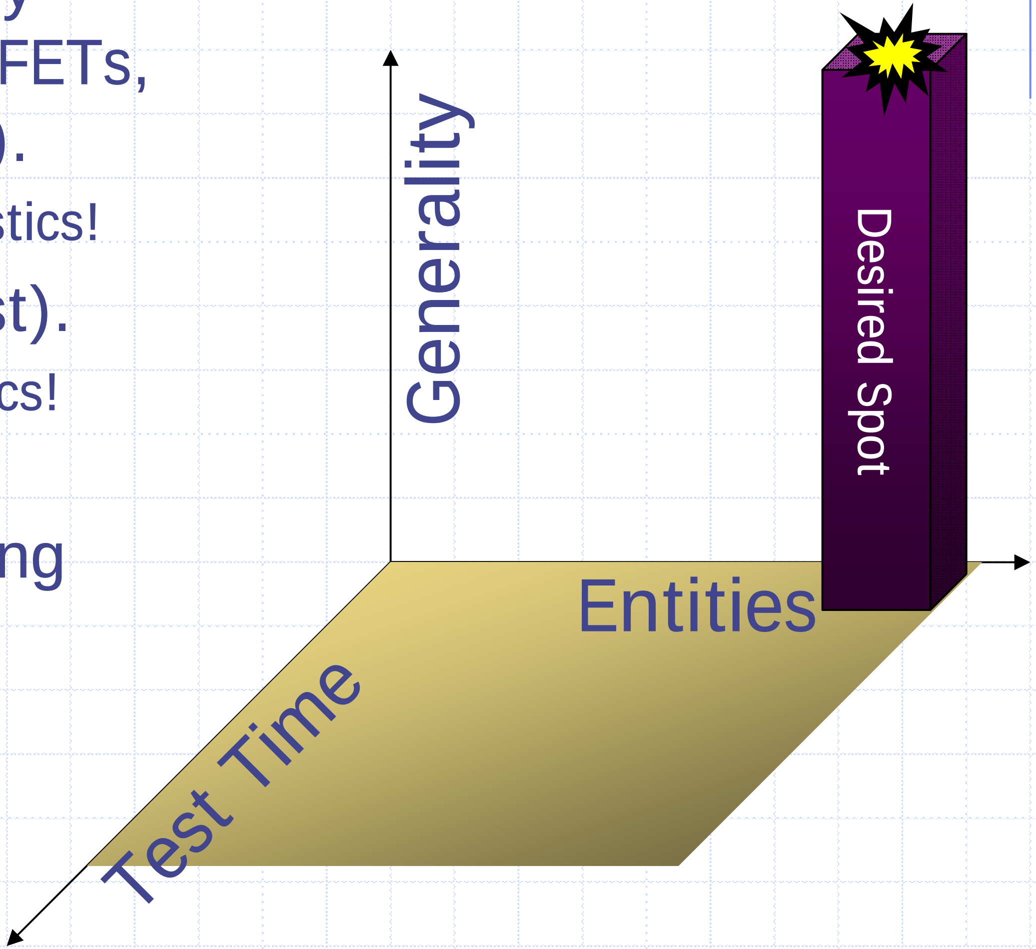
Silicon Information Density

- The efficiency with which we can perform precise variability characterization is going to become important.
  - No longer sufficient to do it once (technology bring up). Need to continually model and re-evaluate.
  - As EDA tools ramp up on understanding process, they will enable new methods of design optimization (e.g. during re-spins).

- Need vastly more information from scarce Si & test resources (increase density)!

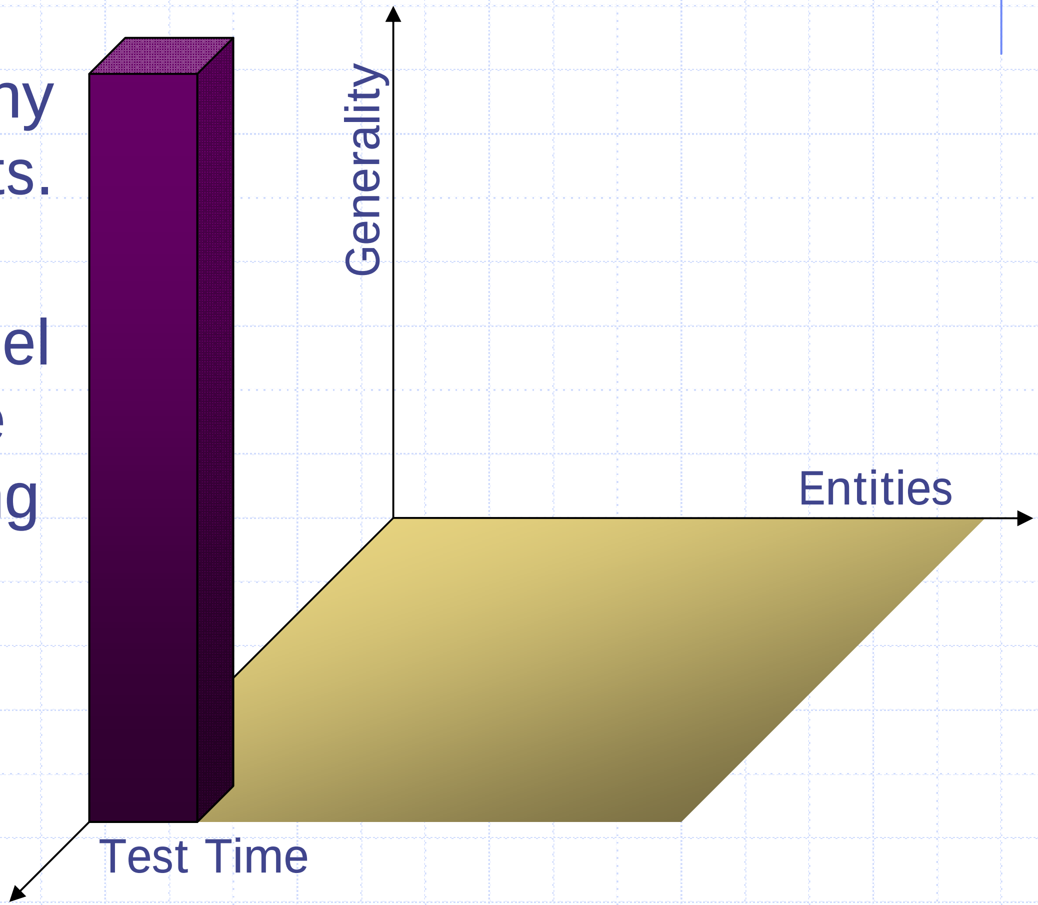
Test Structure Quality?

- Three relative measures:
- Number of individually measurable entities (FETs, ring oscillators, etc...).
  - Many entities ⇒ statistics!
- Test time (or test cost).
  - Lower cost ⇒ statistics!
- Generality of result: suitability for predicting design outcome.
  - Modeling & EDA.



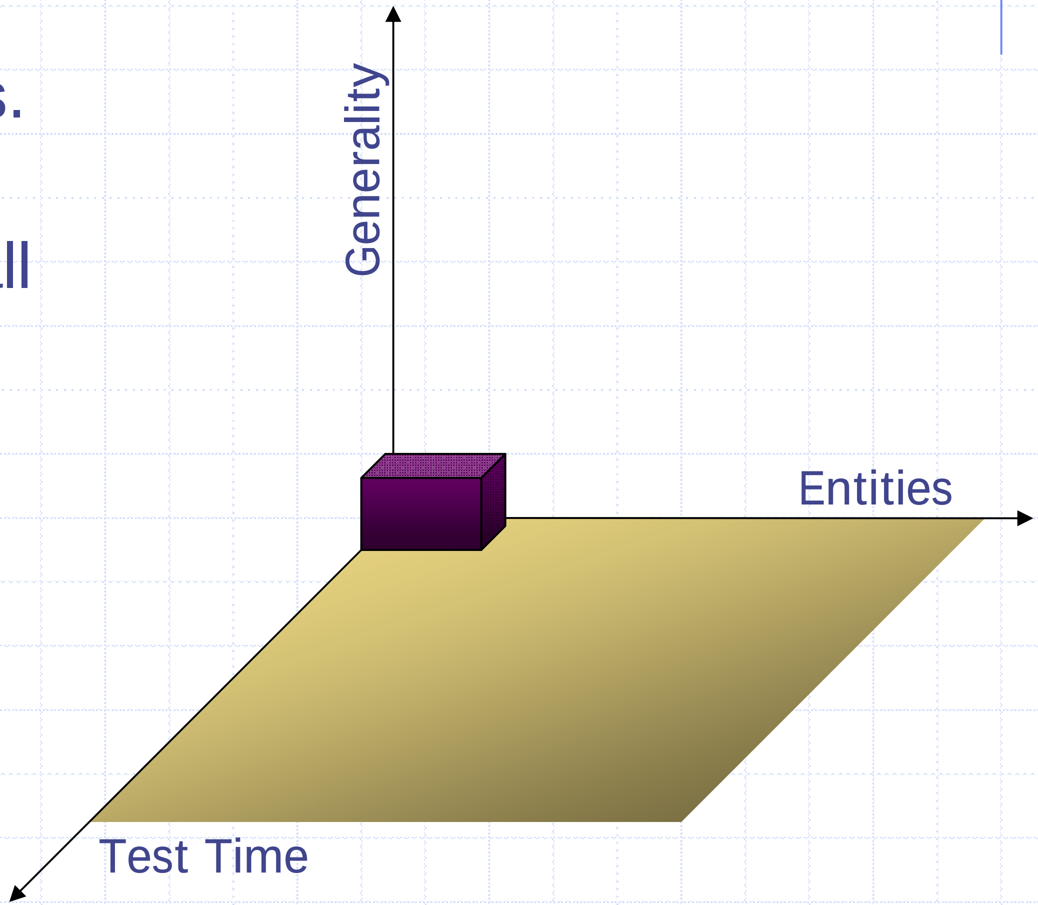
Example: Device Characterization

- Small number of devices with various dimensions.
  - Entities ↓.
- Typically measure many current / voltage points.
  - Analog test time ↑.
- Used to generate model parameters, which are the basis for everything else... (e.g. BSIM)
  - i.e. generality ↑↑.



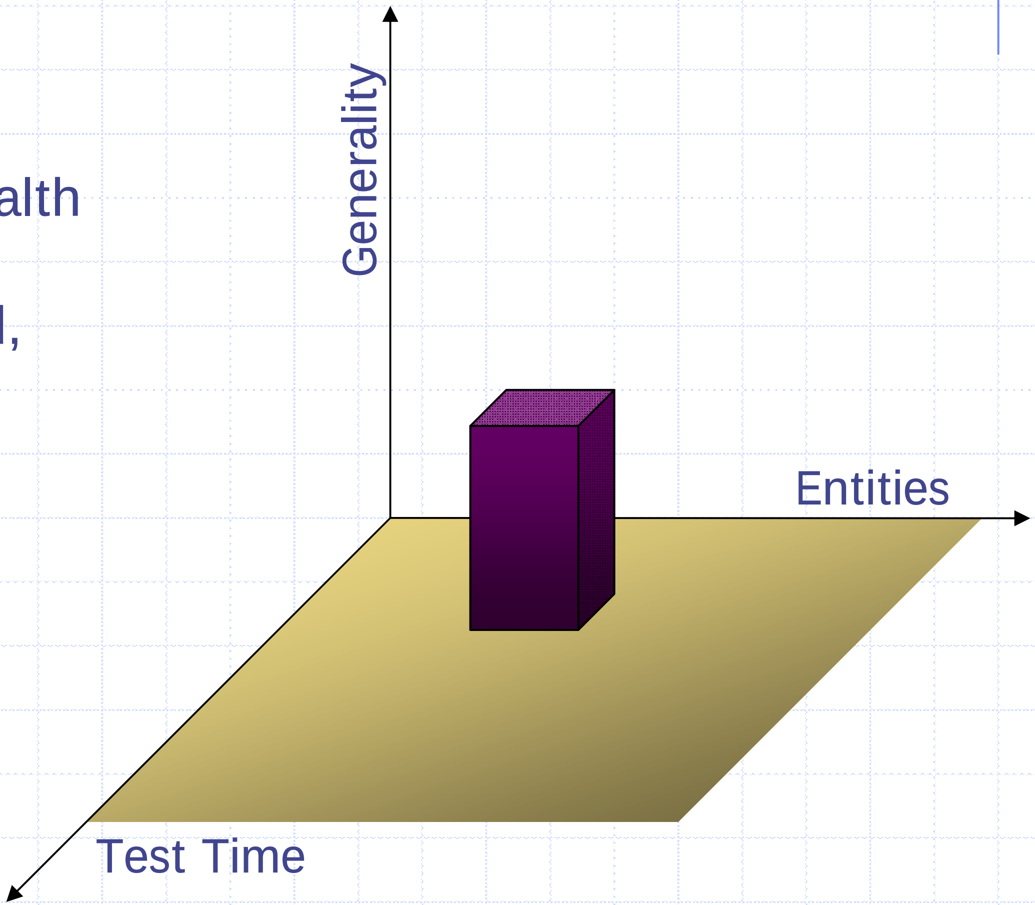
Example: Ring Oscillators (ROs)

- Few ROs per unit.
  - Entities ↓ .
- Typically measure few frequency & I_{DD} points.
  - Fast test ↓ .
- Useful to assess overall health of process, but result is unique to RO structure.
  - i.e. generality ↓ .

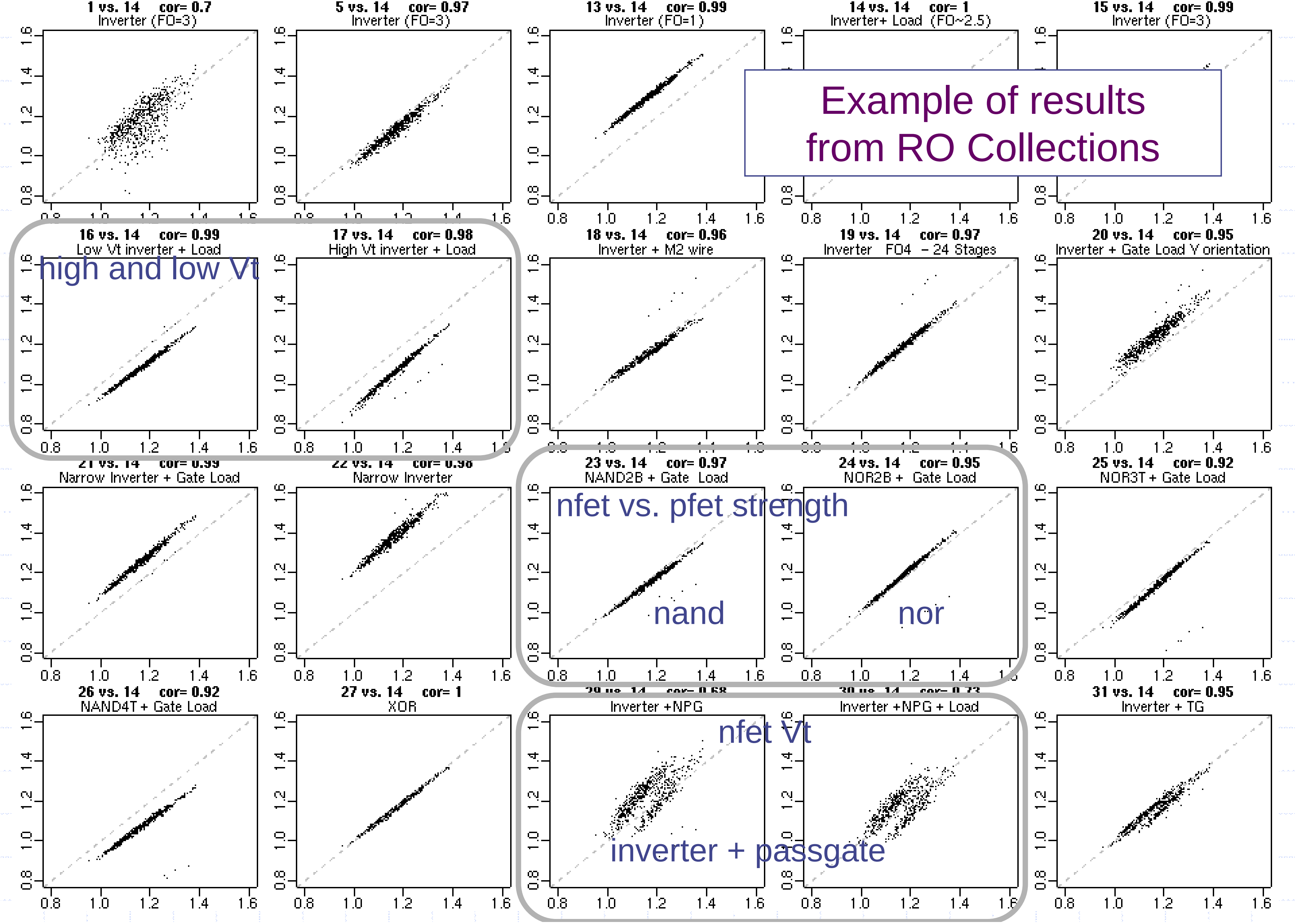


Example: RO Collections

- Variety of ROs per unit.
  - Entities ~.
- Typically measure few frequency & I_{DD} points.
  - Test ↓ .
- Useful to assess overall health of process, and since a variety of ROs are included, more can be learned.
  - i.e. generality ~.
- State of the art!!!



Example of results from RO Collections



high and low Vt

nfet vs. pfet strength

nand

nor

nfet Vt

inverter + passgate

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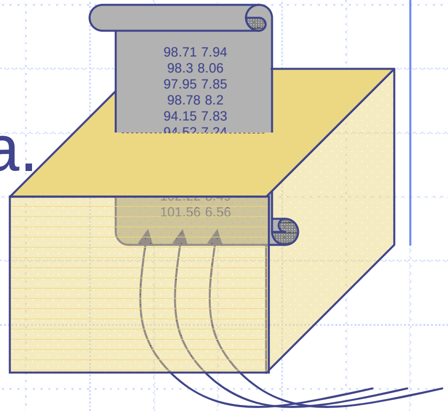
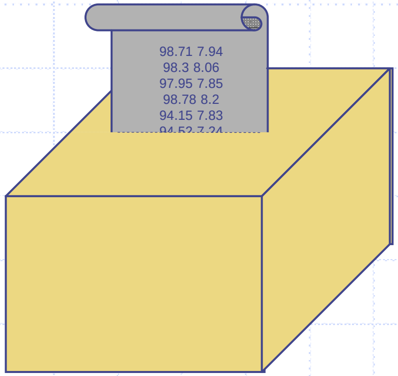
Systematic vs. Random?

- Systematic variability occurs when variation is caused by a known phenomena.
  - Wafer edge behaves differently from center!



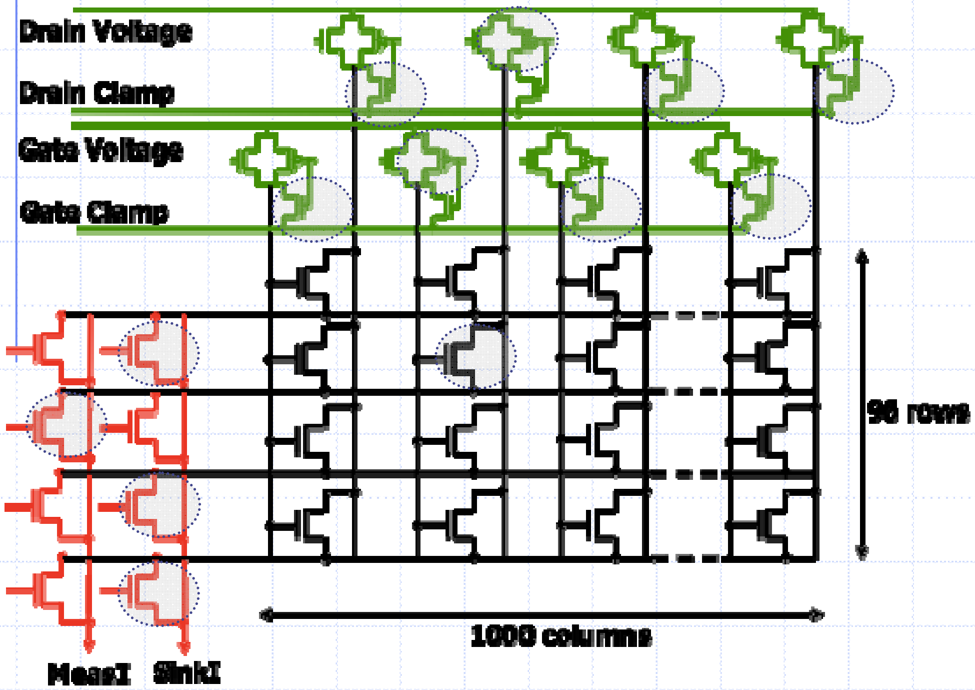
- Random variability occurs when the law of large numbers fails, e.g. for atomistic phenomena driven by scaling.
  - Random dopant fluctuations, line edge roughness.
  - Exacerbated for smaller devices.

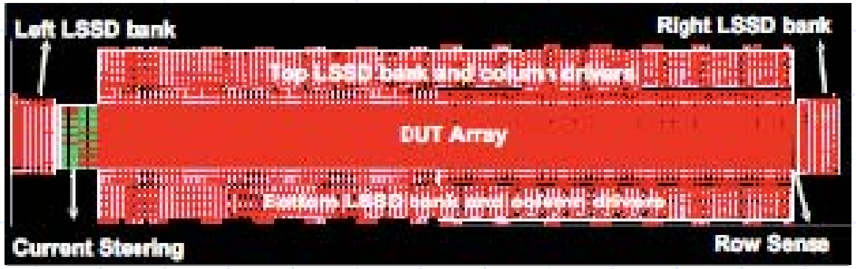


Random Variability Characterization

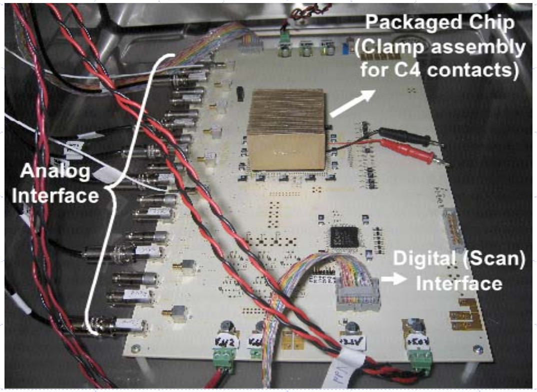
- Estimating statistics requires large numbers of samples.
  - Rule of thumb is ~50 for mean, ~300 for standard deviation, and even more for higher order statistics.
- Often, assumptions about the distribution type need to be verified.
  - Many parameters need not be normal.
- Care must be taken to ensure that the data is not polluted by other sources, e.g. spatial variability, or other sources of systematic change.

Random Variability Example

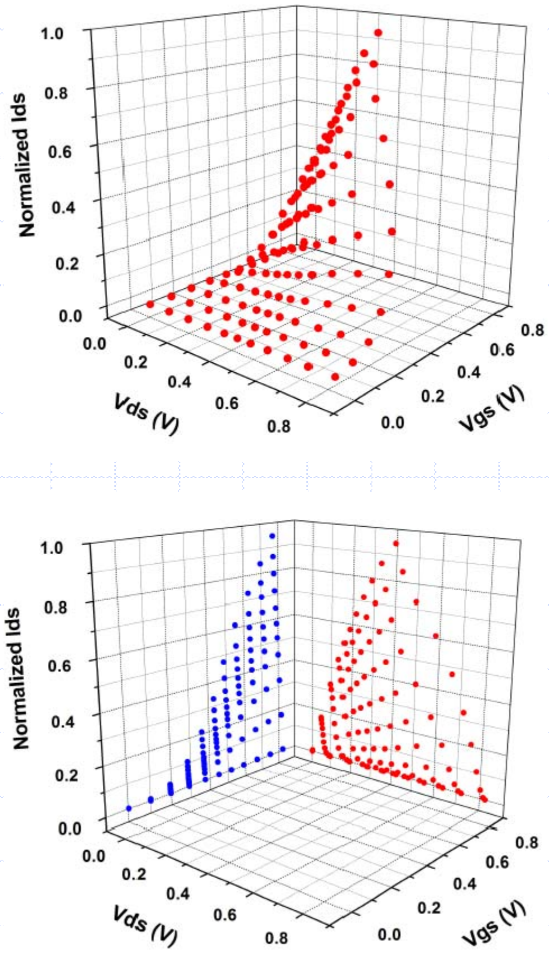




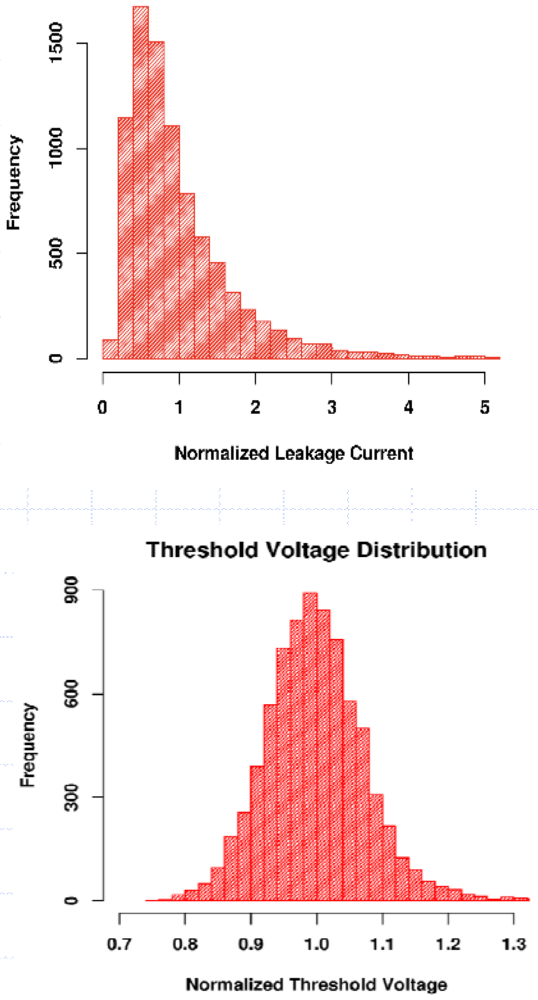
- Test structure to explore the limits of device variability.
- Small sized devices arranged in an addressable array.
- Current is “steered” in array to allow the measurement of individual devices.
- 96 rows, 1000 columns – 96,000 total devices.



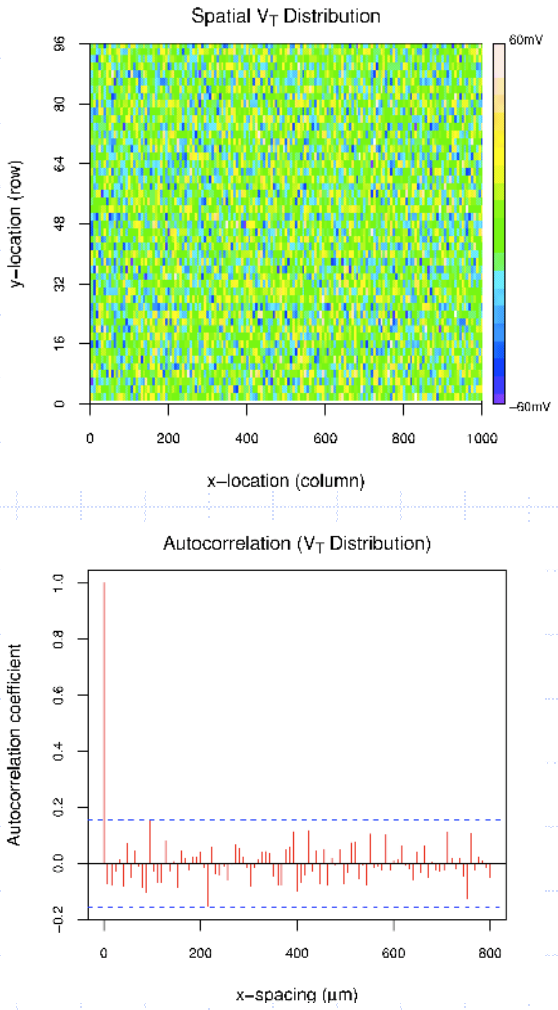
Random Variability Observation



Sample I-V curves



Parameter Distributions



Spatial Correlation

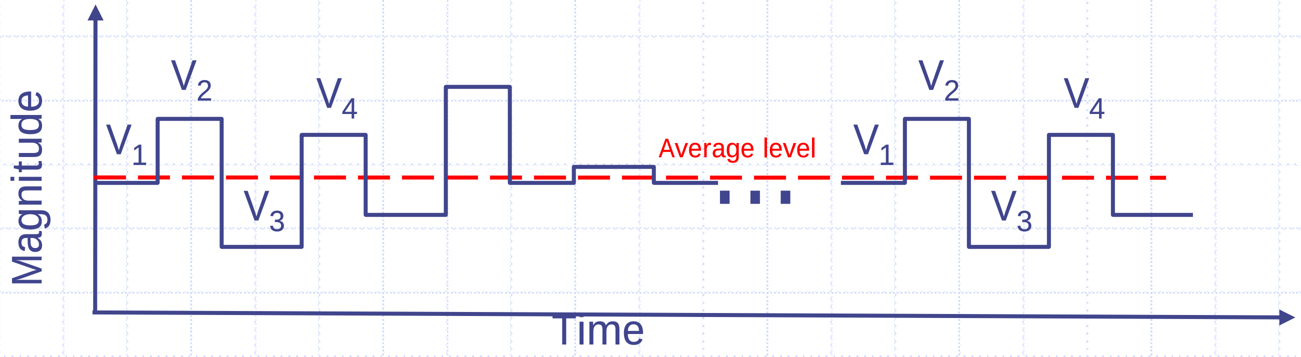
Deep Dive: VT Characterization

- Why is statistical characterization slow?
  - Because we typically need to measure many samples in order to get reliable estimates of distribution moments.

- This is especially true for VT because:
  - It is not a "direct" measurement, so it takes some significant time.
  - It needs to be characterized for a broad range (ideally, +/- 6 σ) so many samples are needed.

Observation

- Assume N measurements are produced as a periodic time domain waveform.
- Assume each measurement (magnitude of the waveform at a given time) corresponds to a parameter value of a single device.
- A simple low-pass filter will produce an average level that corresponds to the mean parameter value of the N devices.

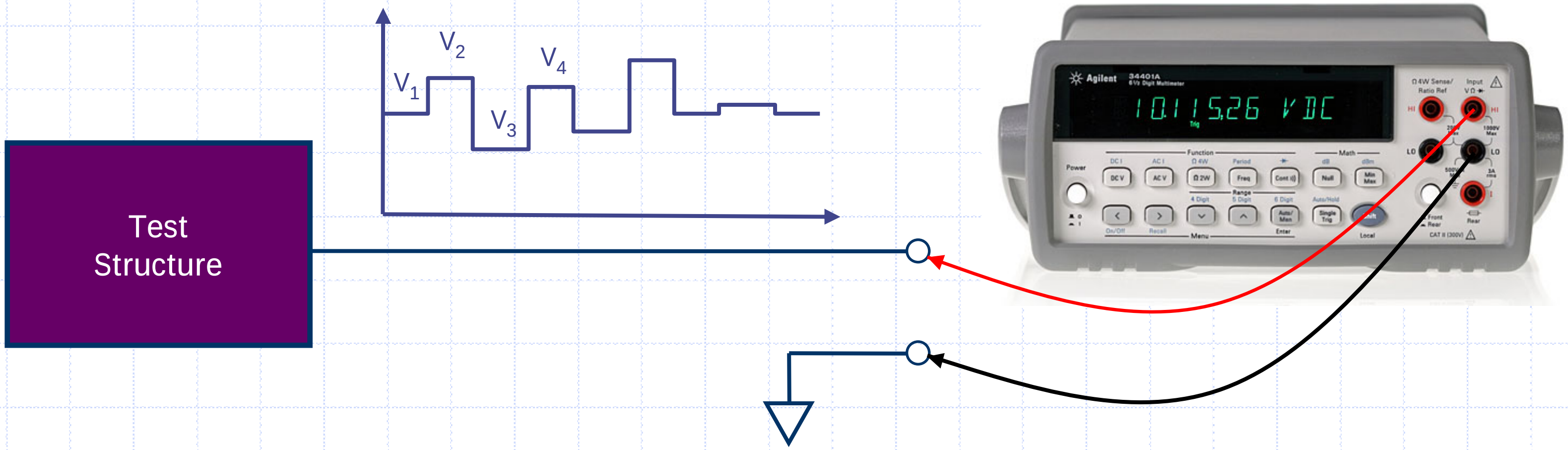


Standard Deviation Calculation

- Recall that the standard deviation of N samples is (with mean μ):
  - $\sigma = (1/N \sum (x_i - \mu)^2)^{½}$
- For the output waveform, centered at zero, the RMS value of the waveform is:
  - $V_{RMS} = (1/N \sum x_i^2)^{½}$
- So if the mean is zero, $V_{RMS} \sim \sigma$!

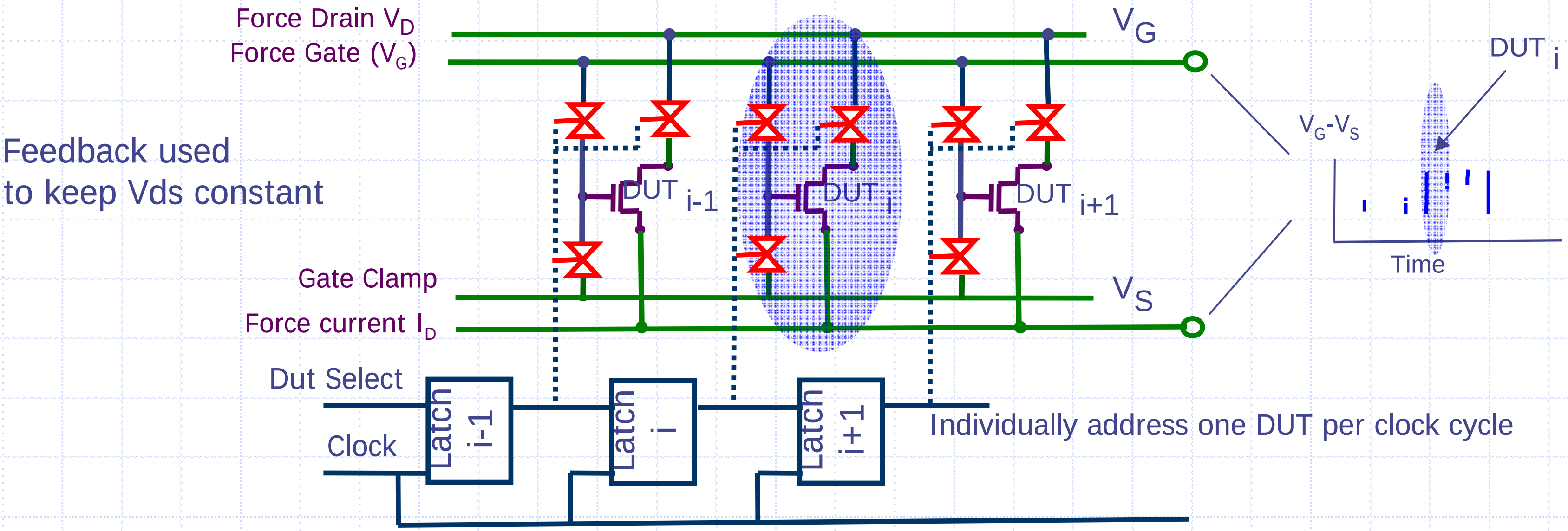
Standard Deviation Measurement

- The mean and sigma of the periodic waveform are obtained using a simple multimeter’s DC and AC modes respectively.
- The statistics of a parametric distribution is directly obtained from its equivalence to the mean and sigma of the waveform.



Test Structure for VT Statistics

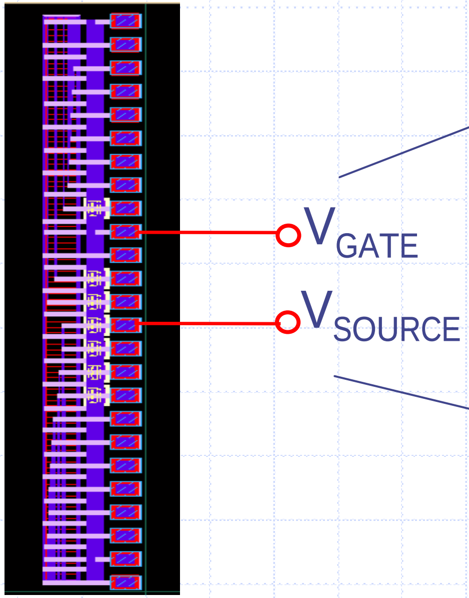
- A forced drain voltage, gate voltage, and source current is applied to the selected DUT using pass-gates.
- The source voltage adjusts itself such that (VGS – VTH) remains constant across all DUTS.
- The variation in VGS is a direct measurement of the variation in voltage threshold (VTH).



Implementation

- Implemented in a 65nm bulk technology
- Structure contains 1000 DUTs of identical layout that are serially accessed to create a periodic waveform representing VTH variations.
- Structure supports configurability of DUT IDS, VDS, VD, and VG for device parameter separation.

65nm Bulk Technology
V_{TH} test structure



Waveform illustrating V_{TH}
variation across multiple devices

```
Acquisition is stopped.
500 Sa/s
```

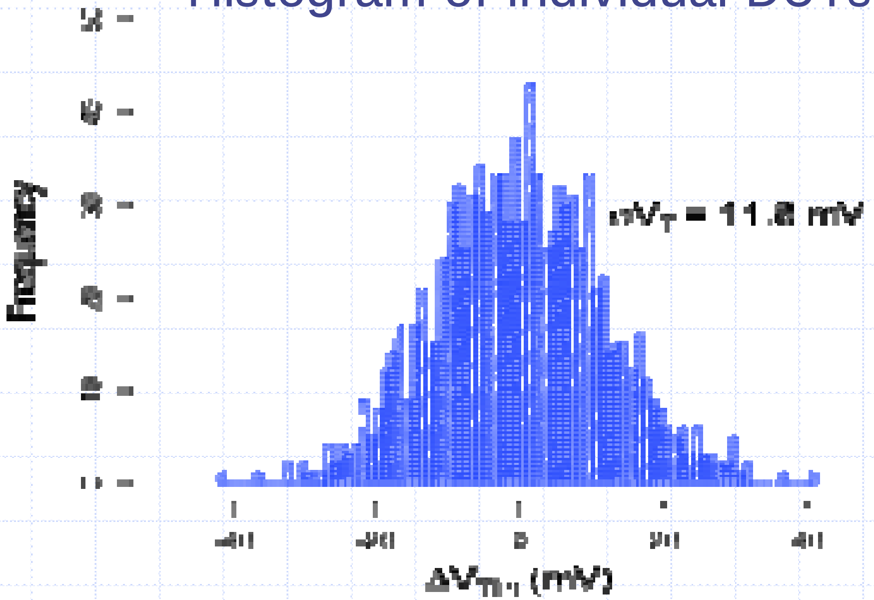
1 On ☑ 20 mV/div
2 On ☐
3 On ☑ 500 mV/div
4 On ☑ 500 mV/div
H 200 ms/div
-134.399000 ms
T 2.470 V

```
                    X                Y
A——(1) = -136.85 ms         45.4 mV
B---(3) = -126.71 ms        -7 mV
      Δ =   10.15 ms       -52.2 mV
   1/ΔX =   98.566246 Hz
```

Results

- A VTH histogram of the 1000 DUTs was obtained in 90 seconds using traditional gate sweeping techniques.
- The statistic's of the VTH distribution were directly obtained using two multi-meter measurements in less than a second!
- Need to extract litho variation from VTH variation to better understand process variability.

Histogram of individual DUTs



Measurement Results

Individual DUTs		Multi-meter	
Mean	Sigma	DC mode	AC mode
562mV	11.8mV	554mV	12.1mV

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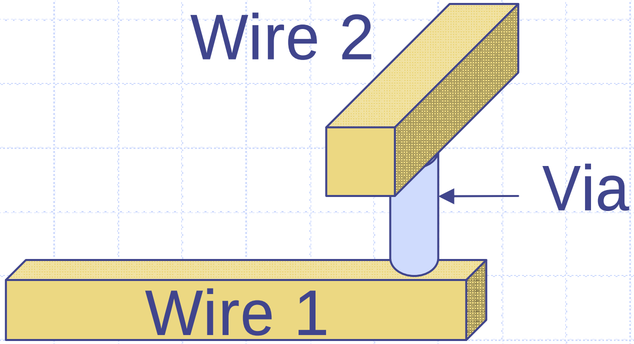
Systematic Variability Characterization

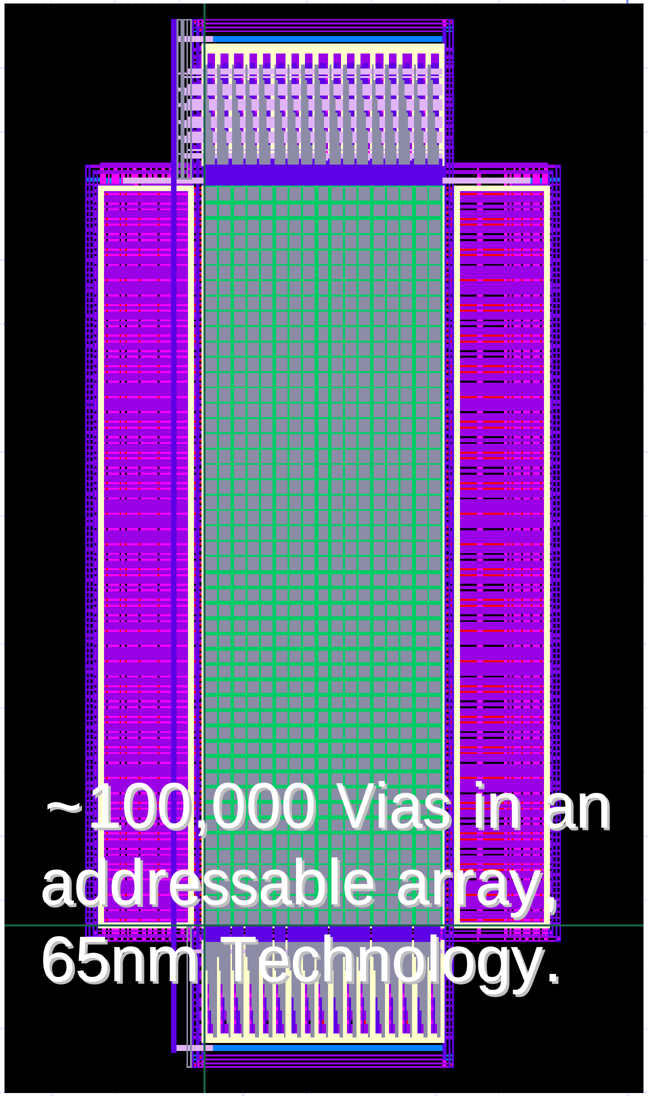
- Observing systematic variability requires careful attention to “experiment plans”.
    - One must define the test structures so that the appropriate insight can be gained.
    - Often that insight is in the form of models (for simulation or otherwise).

- One must be ready to accommodate other sources randomness! (so small numbers of repetitions are usually needed).
- One must also be ready for surprises, when the assumed model is not sufficient or accurate.

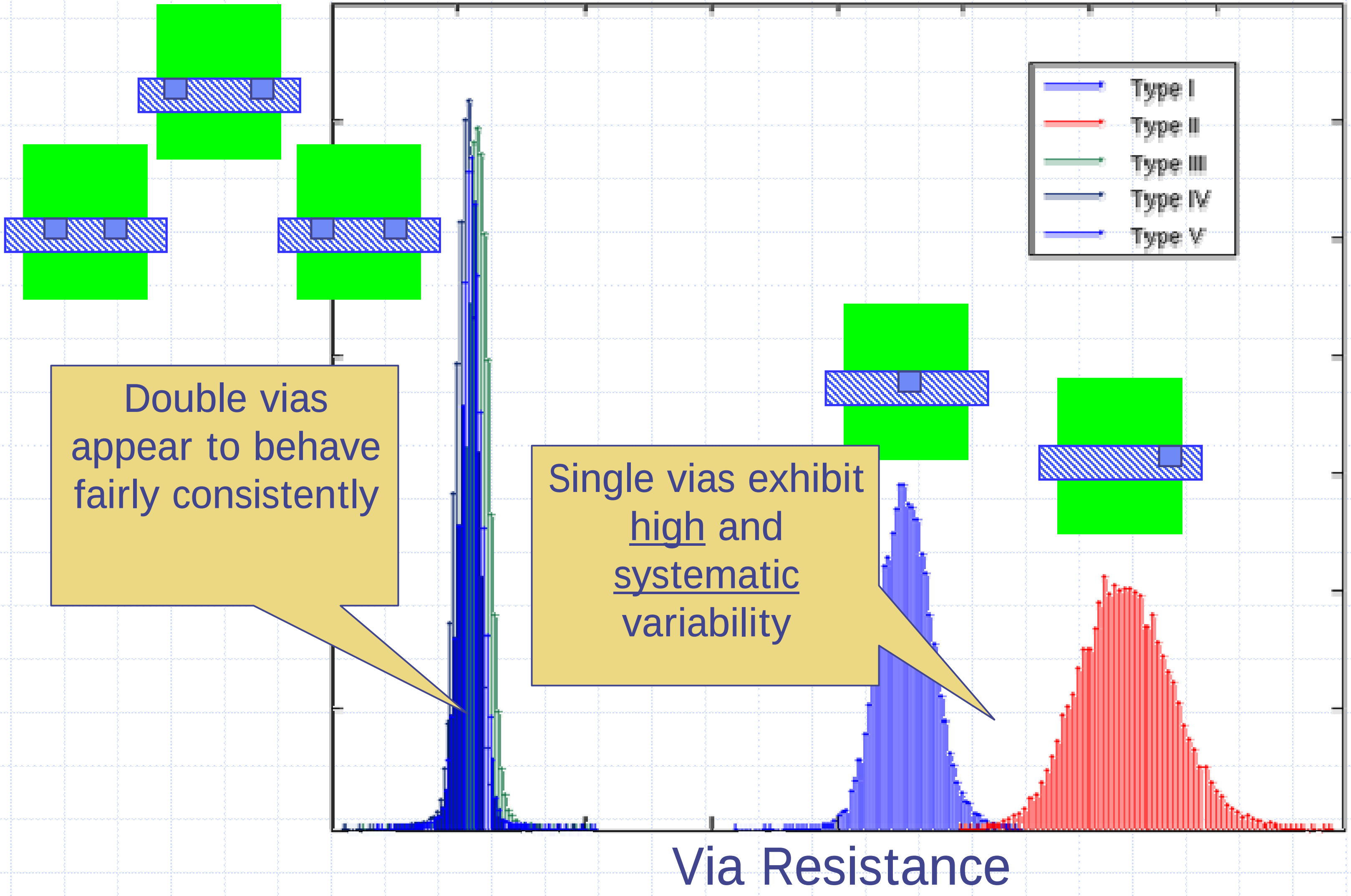
Systematic Variability Example

- Vias are the connections between different metal levels, and between metal and Si.
- Via resistance is a very important technology characteristic.
- We created a special structure to measure resistance of individual vias for various configurations.




~100,000 Vias in an addressable array, 65nm Technology.

Systematic Variability Results



Double vias appear to behave fairly consistently

Single vias exhibit high and systematic variability

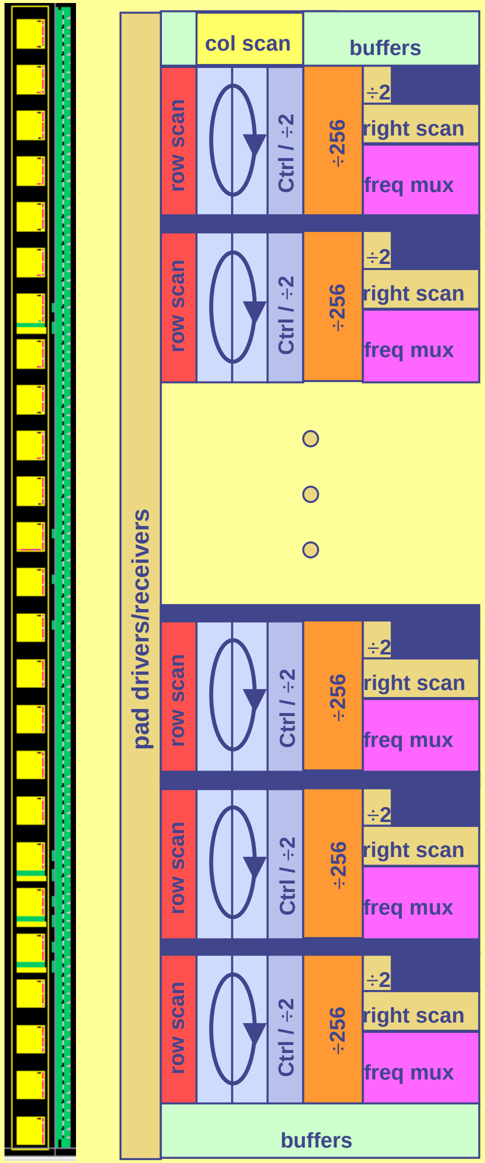
Deep Dive: Layout Systematics

- Wanted to explore the impact of layout on circuit performance in 65nm SOI CMOS.
- Developed a test structure with many ring oscillators with distinct layouts.
- Each layout was modified from a base layout according to a global “experiment plan”.

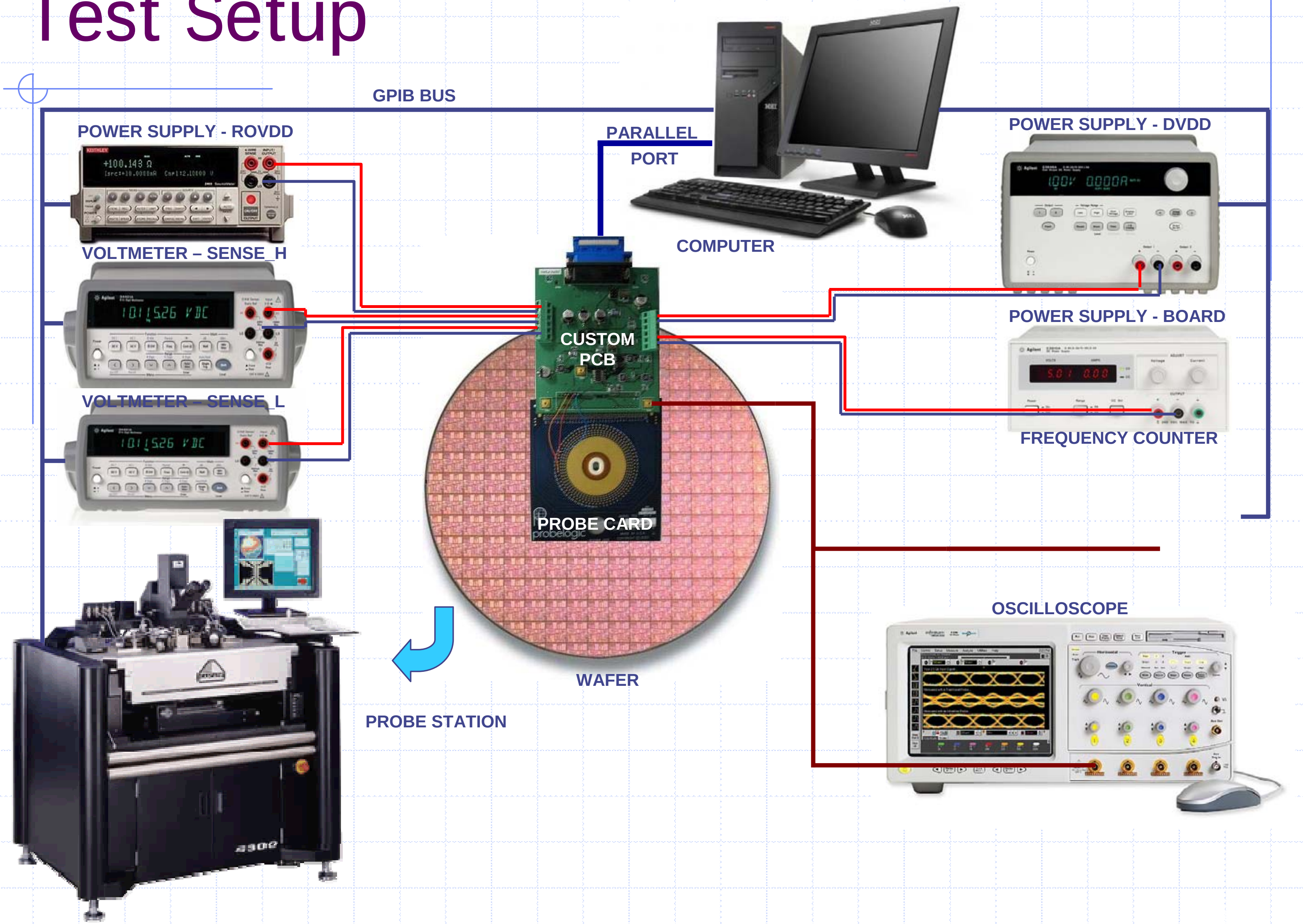
Test Structure Architecture

- Macro is 2500µm x 115µm (including 60µm x 60µm pads).
- Single column of 125 PSRO.
- All digital control through scan chain.
- Ensured good powering strategy
  - PSRO powered from a separate supply ROVDD and ROGND.
  - Digital support circuits supplied from DVDD and DGND.
  - Isolation of supplies aimed at keeping ROVDD as clean as possible.
- Power grid held up from 4 equally spaced pads.
  - Helps with IR drop.
- Has capability of measuring more than 1 PSRO at a time (for quicker measurements).
- Design is easily expandable.
- Most of the design (including DUT generation) done by SKILL code.

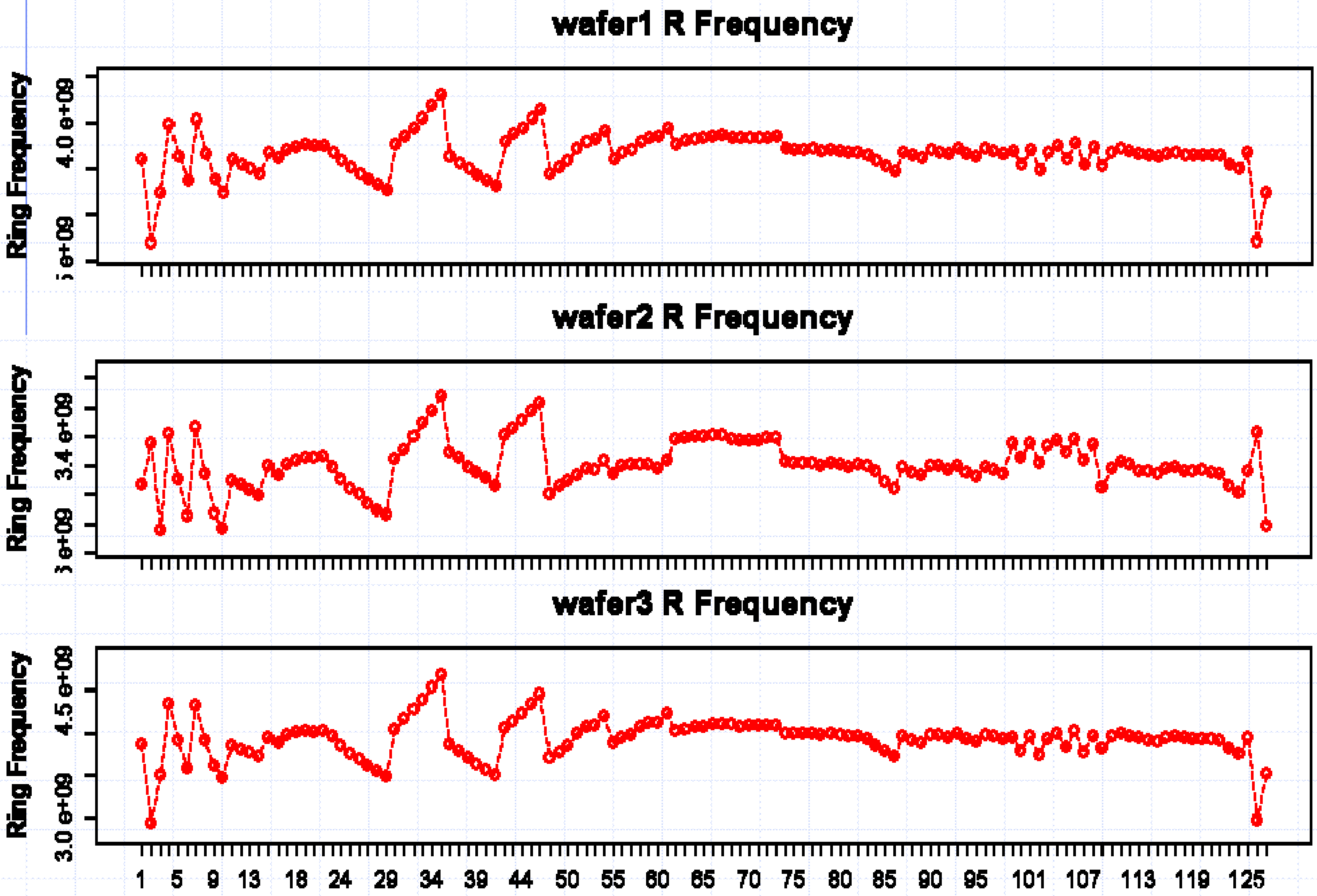
Pin	Signal
1	rovdd
2	rognd
3	dvdd
4	dgnd
5	sense_rovdd
6	sense_rognd
7	F_in
8	rovdd
9	rognd
10	dvdd
11	dgnd
12	F_out2
13	F_out1
14	scan_out
15	rovdd
16	rognd
17	dvdd
18	dgnd
19	clk_b
20	clk_a
21	scan_in
22	rovdd
23	rognd
24	dvdd
25	dgnd



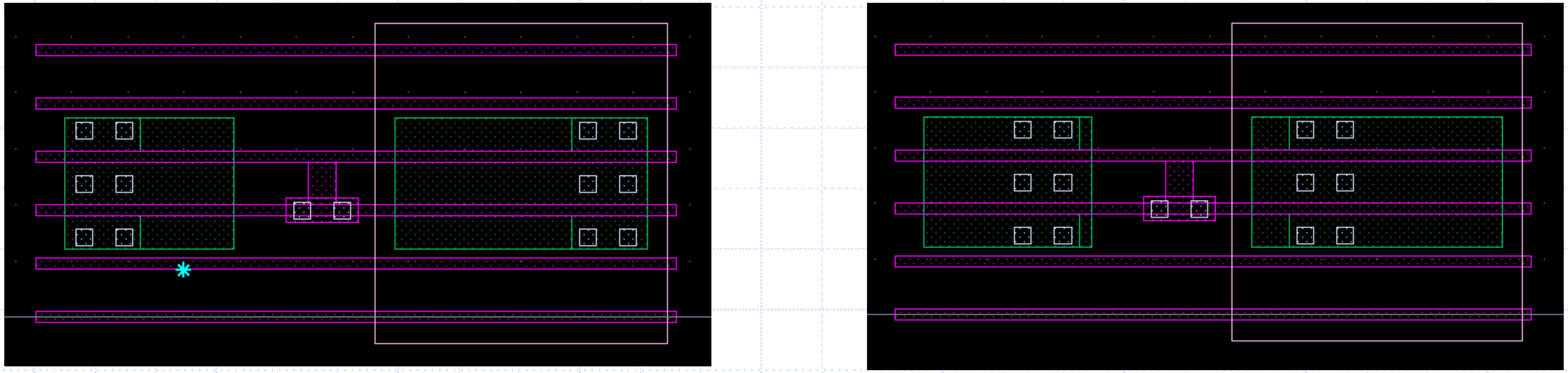
Test Setup

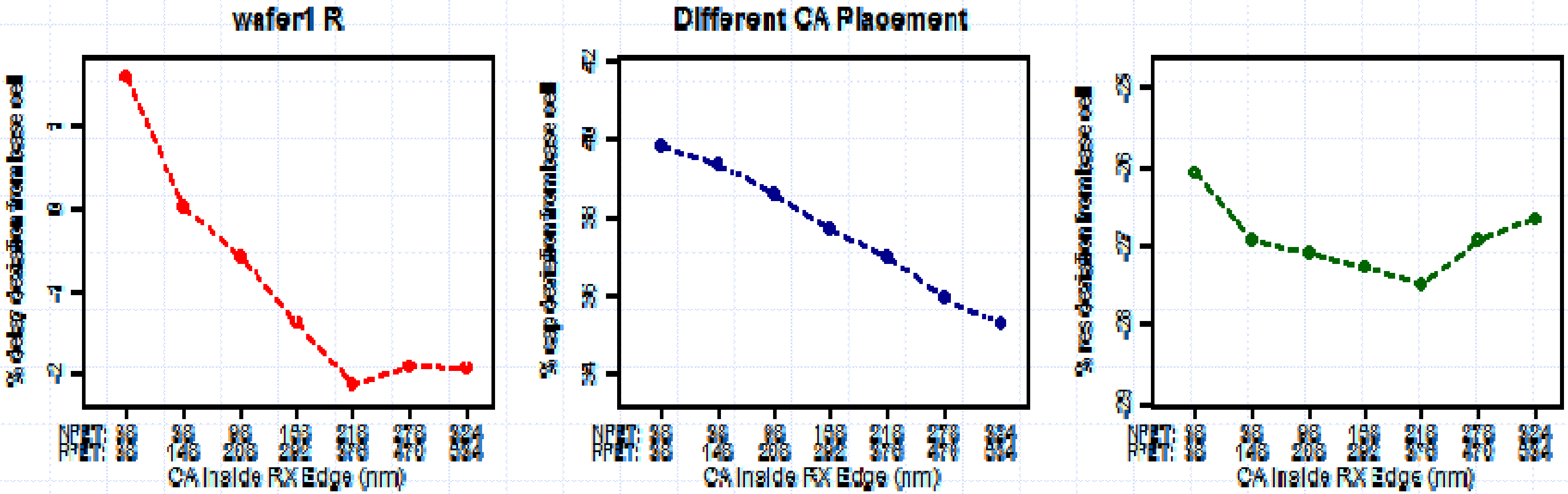

GPIB BUS
POWER SUPPLY - ROVDD
PARALLEL
PORT
COMPUTER
POWER SUPPLY - DVDD
VOLTMETER – SENSE_H
CUSTOM
PCB
POWER SUPPLY - BOARD
VOLTMETER – SENSE_L
FREQUENCY COUNTER
PROBE CARD
OSCILLOSCOPE
WAFER
PROBE STATION

Raw Frequencies: 125 Experiments

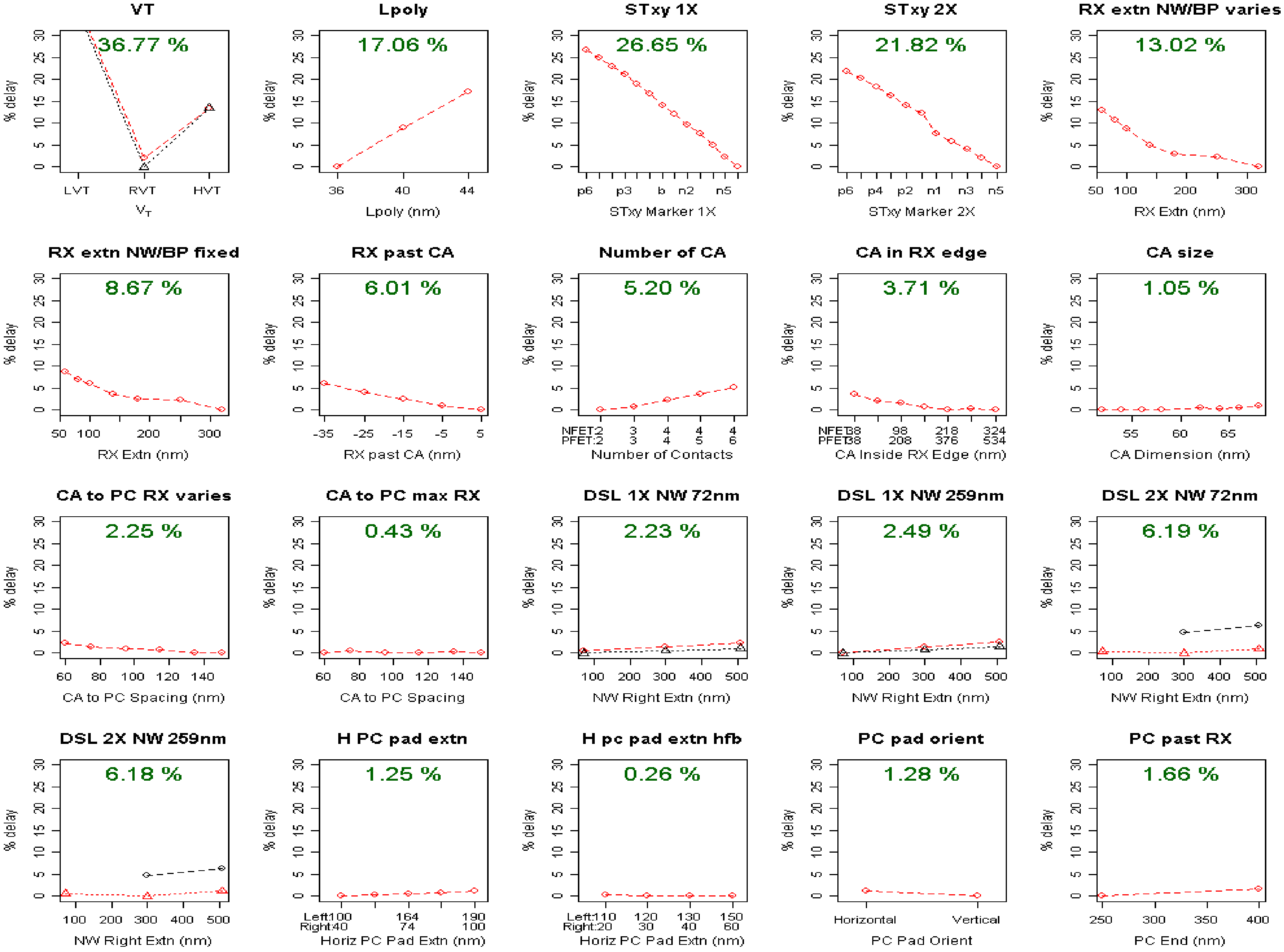


Example: Via Location Impact





Wafer 1 (R) Experiment Summary



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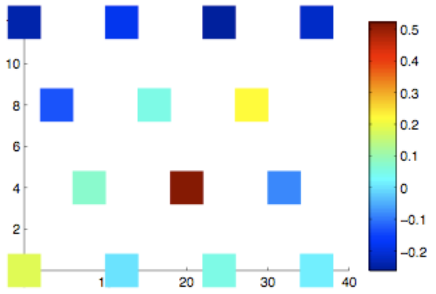
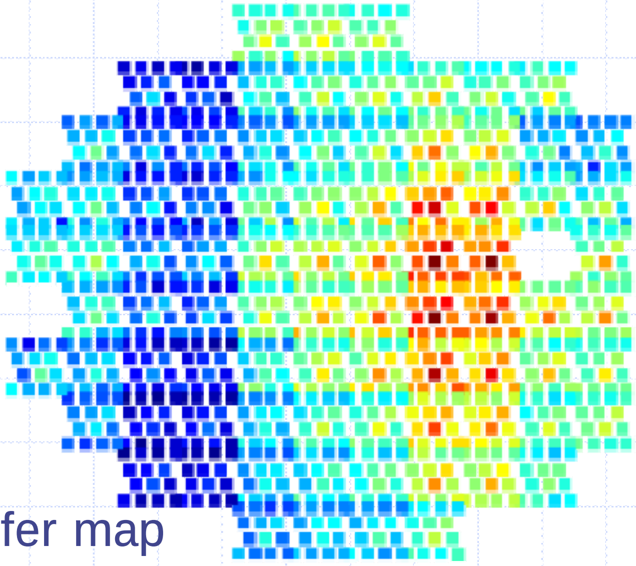
Spatial Variability Characterization

- Requires a “deep” sample of performance over all important levels of the chip manufacturing hierarchy.
- In IBM, performance-sensitive ring oscillators are embedded in each chip.
    - In this example, chip had 14 process rings.
    - Each ring is independently testable.
- Collected 348 wafers from 23 lots.
    - Each wafer contained 117 die.
    - Around 6% of the measurements are missing.
- Work done in partnership with Prof. Sherief Reda, Brown Univ.



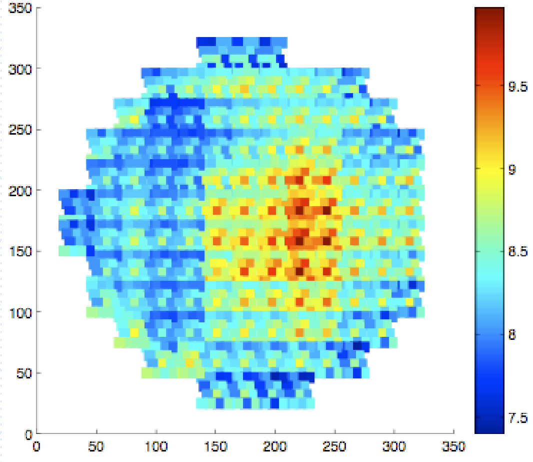
Rings within die



Typical wafer map

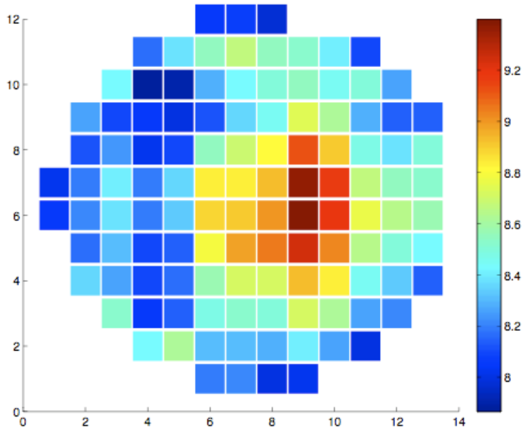
Systematic Spatial Variations

- Extract out “common” pattern across dies and wafers.
- Take the mean of the data, and separate out the wafer and die components.
    - Paper on algorithms used published in DATE 2009.



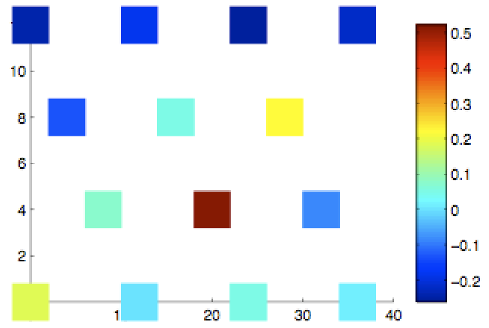
average wafer

=



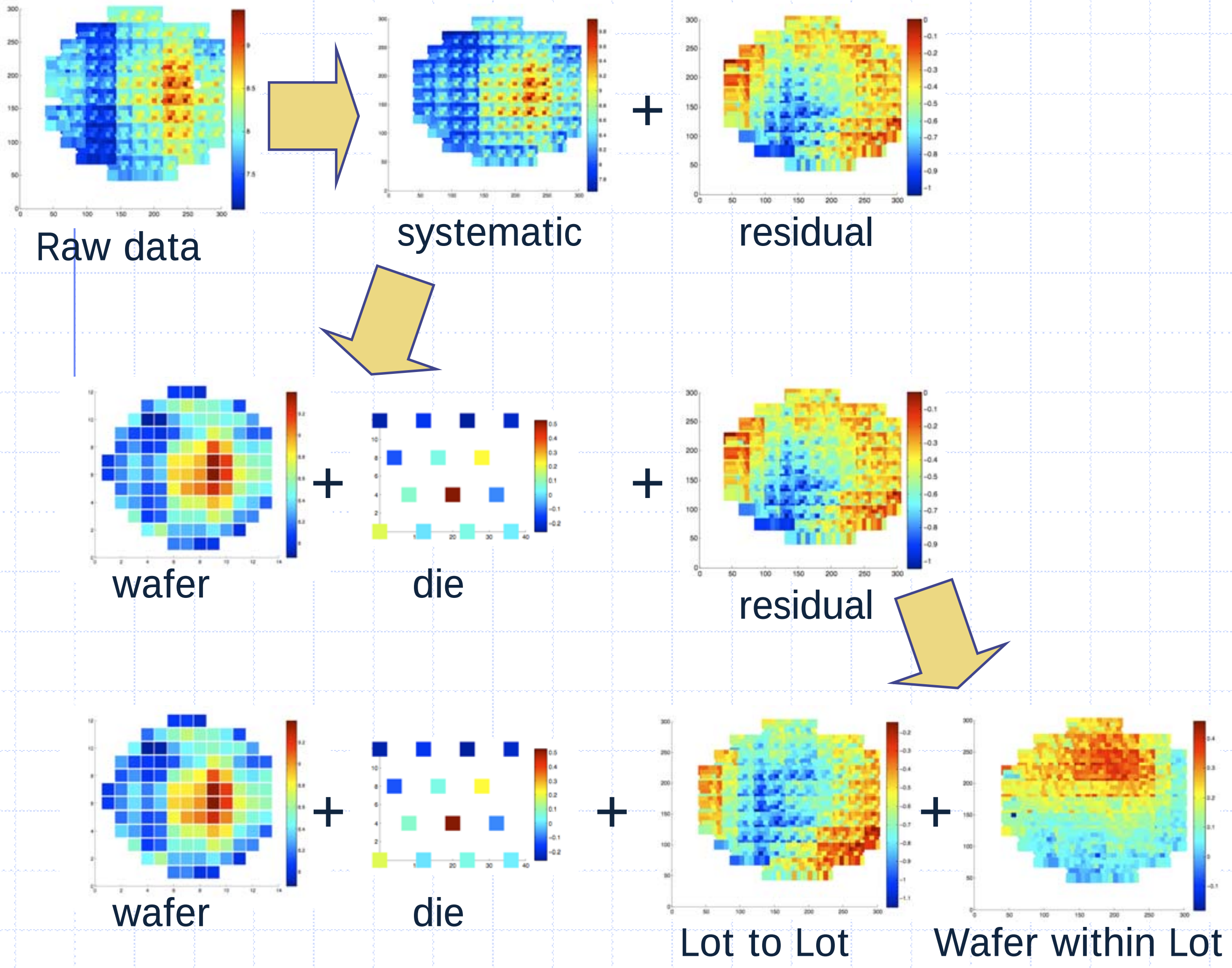
systematic within-wafer

+



systematic within-die

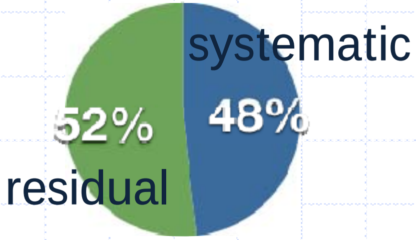
Overall Variability Breakdown

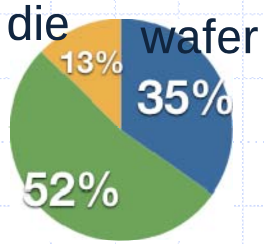

Raw data

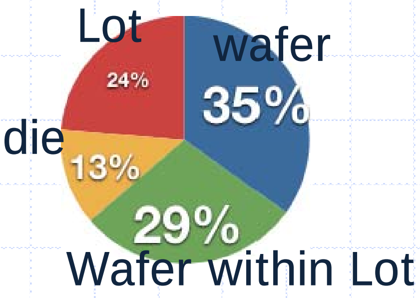
systematic + residual

wafer + die + residual

wafer + die + Lot to Lot + Wafer within Lot







Spatial Systematic vs. Random

- There are a number of systematic phenomena at various length scales:

Wafer-level phenomena	~3000 μ .
Chemical Mechanical Polishing	~300 μ .
Rapid Thermal Annealing	~30 μ .
Resist Etch Loading	~3 μ .
Lithography	~0.3 μ .

- From a design-level modeling point of view, these systematic phenomena have been a problem.

Conclusions

- Future technology development will need to rely on sophisticated modeling enablement.
- Increasing complexity and variability makes current characterization methods irrelevant.
- New characterization paradigms require innovations in test structures to enable rapid and accurate response to new phenomena.
  - IBM Research has developed a substantial amount of technology/circuit characterization structure IP for both internal development and licensing.

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